Fabrication of Electronically integrated, mass-manufactured, microscopic robots

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Abstract

We have developed a fabrication process that can be used to build millions of microscopic, electronically-integrated robots. Our procedure includes steps for building silicon microelectronics, building components for actuation, encapsulation steps, and a process for releasing the robots into aqueous environments. Each step is carried out massively in parallel, allowing us to build over a million robots on a single 4-inch wafer. Broadly, the new actuators and fabrication protocols presented here offer a generic platform and can be used to make a wide range of silicon-based, functional robotic systems that are too small to be resolved by the naked eye.

Introduction

After 50 years of Moore's law, it's now possible to pack nearly 1 million transistors in the space of a paramecium. This radical miniaturization of electronics has brought with it incredible opportunities for the field of microrobotics. In principle, electronic components could be appropriated to create tiny robots that sense their environment, communicate, or compute.

But a major roadblock exists: there is no micron-scale actuator system that seamlessly integrates with semiconductor processing and responds to standard electronic control signals. In a companion publication, we showed how to overcome this barrier with a new class of voltage-controllable electrochemical actuators that operate at low voltages (200 mV), low power (10 nW), and are completely compatible with silicon processing. To demonstrate their potential, we created lithographic fabrication and release protocols and prototyped sub-hundred micrometer walking robots.

This document provides a detailed description of the steps we used to build electronically integrated, microscopic robots. Every step is performed massively in parallel, allowing us to produce over one million robots per 4-inch wafer. Looking forward, these results can be built upon to incorporate more complex electronic components, taking a major step toward mass-manufactured, silicon-based, functional robots too small to be resolved by the naked eye.

Reagents

Commercially produced SOI wafers (Ultrasil Corporation). The device layer is p-type (boron doped), 2 µm thick and has a resistivity 0.1 Ohm-cm. The buried oxide layer is 500 nm thick and the handle layer is 500 µm thick.

Equipment

Procedure

Dope the wafers, forming p-n junctions:

1) deposit 550 nm of phosphosilicate glass (5% by weight PSG) at 350° C with PECVD using phosphine/helium plasma.

2) diffuse dopants into the device layer by annealing the substrate at 1000°C for 3 min in argon with a rapid thermal annealer, using a ramp rate of 75C°/s.

3) remove the phosphosilicate glass using 6:1 buffered oxide etch (BOE).

Selectively remove portions of the n-layer to provide contact points with the underlying p-silicon:

1) Prime wafers with HDMS.

2) Spin on Shipley 1813 photoresist at 3000 RPM for 45 seconds with a 1000 RPM/s ramp rate, bake the resist on a hotplate at 115°C for 1 minute.

3) Expose using a g-line 5x stepper.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spin dry (Hamatech HMP 900).

5) Etch the top layer of n-type silicon using inductively coupled HBr plasma, removing 1 μm of silicon.

6) Remove passivated resist via a 1 minute etch in oxygen plasma (150W).

7) Strip the photoresist by sonication in remover 1165, rinse with DI, blow dry with nitrogen and plasma ash any residuals in a reactive ion etch using oxygen plasma (150W).

Selectively remove the unwanted p-type silicon, defining the PV structure:

1) Prime the wafers with HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, and bake the resist on a hotplate at 115° C for 90 seconds.

3) Expose using a g-line 5x stepper.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spin dry (Hamatech HMP 900).

5) Etch away exposed silicon via HBr all the way to the underlying oxide.

6) Remove passivated resist via a 1 minute etch in oxygen plasma (150W).

7) Strip the photoresist by sonication in remover 1165, rinse with DI, blow dry with nitrogen and plasma ash any residuals in a reactive ion etch using oxygen plasma (150W).

Electrically isolate the p-n junction with a conformal dielectric layer:

1) Plasma clean the surface of the wafer via 5 minutes of oxygen plasma at 150W.

2) Deposit 50 nm of silicon dioxide via plasma enhanced atomic layer deposition at 110° C.

Make electrical contacts to the p-type and n-type silicon:

1) Prime the wafers via HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, and bake the resist on a hotplate at 115° C for 90 seconds.

3) Expose using a g-line 5x stepper defining regions where we want to form contacts.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spun dry (Hamatech HMP 900).

5) De-scum residual resist using a 1 minute oxygen plasma at 150W.

6) Bake the resist for 5 minutes at 115°C.

7) Etch the deposited oxide in 30:1 BOE, rinse the wafer in DI and blow dry.

8) Immediately load the wafer into a sputter deposition tool, deposit 20nm of Ti and 60 nm of platinum to form metal contacts.

9) Sonicate off resist and unwanted metal in 1165, rinse with DI and blow dry.

10) Anneal the metal contacts at 350°C for 5 minutes in vacuum.

Pattern the buried oxide layer:

1) Prime the wafers via HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, and bake the resist on a hotplate at 115° C for 90 seconds.

3) Expose using a g-line 5x stepper defining the bottom layer of oxide that will form the robot body.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spun dry (Hamatech HMP 900).

5) De-scum residual resist using a 1 minute oxygen plasma at 150W.

6) Etch the unwanted oxide using inductively coupled CHF_3/O_2 plasma.

7) Remove passivated resist via 1.5 minute oxygen plasma at 150W.

8) Strip the photoresist by sonication in remover 1165, rinse with DI, blow dry with nitrogen and plasma ash any residuals in a reactive ion etch using oxygen plasma (150W).

Deposit a platinum layer for use as a Surface Electrochemical Actuator (SEA):

1) Plasma clean the surface of the wafer via 3 minutes of oxygen plasma at 75W.

2) Use thermal atomic layer deposition to deposit 1 cycle of aluminum oxide, creating a seed layer for the deposition of platinum.

3) Deposit platinum with thermal atomic layer deposition (via Arradiance Gemstar 6) at 250°C using precursors of Trimethyl(methylcyclopentadienyl)platinum(IV) ($MeCpPtMe_3$) and O_2. We pulse these reactions for 70 cycles to produce our 7 nm platinum growth (see section on characterization for thickness vs cycle number).

Pattern the platinum layer for the SEAs:

1) Prime the wafers via HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, bake the resist at 115° C for 90 seconds.

3) Expose using a g-line 5x stepper defining open areas in the resist that will be filled with a chrome hard mask.

4) Develop in AZ 726 using an automated developer tool with a 1-minute single puddle recipe and spin dry (Hamatech HMP 900).

5) Sputter deposit 70 nm of chrome.

6) Lift off resist and unwanted metal via sonication in 1165, rinse in DI, blow dry in nitrogen.

7) Etch the exposed platinum via aqua regia (3 parts hydrochloric acid, 1 part nitric acid) at 55° C with mechanical stirring (100 RPM stir bar), checking to see when the platinum has cleared in 8 second intervals, rinse in DI, and blow dry with nitrogen.

8) Remove the chrome via wet etching (Cyantek CR-14), rinse with DI, and blow dry with nitrogen.

Pattern/deposit the capping layer of the SEAs:

1) Prime the wafers via HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, bake the resist at 115°C for 90 seconds.

3) Expose using a g-line 5x stepper defining open areas in the resist that will be filled with titanium.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spun dry (Hamatech HMP 900).

5) Sputter deposit 2 nm of titanium.

6) Lift off resist and unwanted metal via sonication in 1165, rinse in DI, blow dry in nitrogen.

Interconnect the SEAs to the silicon photovoltaics:

1) Prime the wafers via HMDS.

2) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, bake the resist at 115°C for 90 seconds.

3) Expose using a g-line 5x stepper defining open areas in the resist that will be filled with titanium platinum interconnects.

4) Develop in AZ 726 using an automated developer tool with a 1 minute single puddle recipe and spun dry (Hamatech HMP 900).

5) Sputter deposit 20 nm of Ti, then 60 nm of platinum to form metal interconnects.

6) Lift off resist and unwanted metal via sonication in 1165, rinse in DI, blow dry in nitrogen.

Dice the 4-inch wafer into 12 mm test die

1) Spin a protective layer of Shipley 1827 resist at 3000 RPM for 45 seconds with 1000RPM/s ramp, bake the resist at 115°C for 120 seconds.

2) Dice the wafer with a silicon specialized dicing blade (KNS S1235) spinning at 3000 RPM with a feed speed of 2 mm/s.

3) Rinse debris from the wafer with DI gun and blow dry with nitrogen.

4) Remove protective resist and residual debris by sonicating in 1165, rinse in DI, blow dry nitrogen.

Pattern an SU8 encapsulation layer and rigid panels:

1) Spin coat SU-5 epoxy on the diced chips at 3000 RPM for 30 seconds with a 1000RPM/s ramp rate.

2) Soft bake the chips for 1 minute at 65°C followed by 2 minutes at 95°C.

3) Manual strip the edge bead on each chip with acetone and alpha swabs, removing ~2 mm.

4) Expose SU8 on a contact aligner (ABM) with a 365 nm filter in place.

5) Bake the chip for 1 minute at 65°C followed by 3 minutes at 95°C.

6) Develop for 1 minute in SU8 developer with agitation, rinse in IPA, blow dry with nitrogen.

7) Bake chip at 65°C, transfer to 95°C hotplate and ramp to 150°C.

8) Hold the chip at 150°C for 5 minutes, turn off the hotplate and allow to cool to room temperature.

Mechanically support the devices with patterned aluminum prior to release:

1) Sputter coat 200 nm of aluminum everywhere on the chip.

2) Deposit a 2 nm thick layer of aluminum oxide via plasma enhanced atomic layer deposition to fill any pinholes in the film.

3) HMDS prime the chip.

4) Spin on Shipley 1827 resist at 3000 RPM for 45 seconds with 1000 RPM/s ramp, bake the resist at 115°C for 90 seconds.

5) Manual strip the edge bead on each chip with acetone and alpha swabs, removing ~2mm.

6) Expose resist on a contact aligner (ABM) to pattern openings where aluminum will be removed.

7) Manually develop resist with AZ 726 developer with a 1 minute emersion and agitation, DI rinse and nitrogen blow dry.

8) De-scum residual resist in oxygen plasma for 1 minute at 150 W.

9) Bake the resist for 1 minute at 115°C.

10) Wet etch unwanted aluminum with aluminum etchant (Transene A), rinse in DI, blow dry with nitrogen.

11) Strip the photoresist in acetone, rinse in IPA, rinse in DI, blow dry with nitrogen.

Release devices from the substrate:

1) Strip residual organics from the chip by plasma cleaning in oxygen at 150 W for 5 minutes.

2) Under etch the silicon using pulsed XeF2 vapor phase etching, 2.5T pressure, 12 second cycles. Typical etches are ~150 cycles long.

Stamp devices onto target substrates:

1) Press a PDMS stamp into contact with the released devices and rapidly peel it away.

2) Spin S1827 resist onto the “inked” surface of the PDMS stamp (3000 RPM spin speed, 1000 RPM/s ramp, 30 seconds).

3) Manually press the resist-robot side of the PDMS stamp into contact with the target substrate, let relax for 1 minute, peel away PDMS.

Release the devices into solution:

1) submerge the target substrate loaded with robots into a bath of diluted aluminum etchant (~100:1 dilution by volume with DI). All of the aluminum must be removed.

2) Dilute the aluminum etchant via solvent exchange with DI to pH neutral.

3) Add buffered NaOH (pH 13) to dissolve the resist into solution.

4) Solvent exchange to create desired solution chemistry (pH, salt concentration, etc.). We tested deployed robots in three different solutions: 1X phosphate buffer saline, 1M NaOH (pH 13), and dilute phosphoric acid (pH 2.4). In all three cases we were able to produce the desired actuation response when illuminated.

Troubleshooting

Time Taken

Anticipated Results

References

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