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Gyuho Myeong
Korea Advanced Institute of Science and Technology
Wongil Shin
Korea Advanced Institute of Science and Technology
Seungho Kim
Korea Advanced Institute of Science and Technology
Hongsik Lim
Korea Advanced Institute of Science and Technology
Boram Kim
Korea Advanced Institute of Science and Technology
Taehyeok Jin
Korea Advanced Institute of Science and Technology
Kyunghwan Sung
Korea Advanced Institute of Science and Technology
Jihoon Park
Korea Advanced Institute of Science and Technology
Michael Fuhrer
Monash University https://orcid.org/0000-0001-6183-2773
Kenji Watanabe
National Institute for Materials Science https://orcid.org/0000-0003-3701-8119
Takashi Taniguchi
National Institute for Materials Science, Tsukuba, Ibaraki https://orcid.org/0000-0002-1467-3105
Fei Liu
Peking University
Sungjae Cho (sungjae.cho@kaist.ac.kr)
Korea Advanced Institute of Science and Technology https://orcid.org/0000-0003-2547-095X

Article

Keywords: power consumption, low-power diode rectifier, density of states, low-power circuit technology

Posted Date: October 28th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-1008445/v1

Version of Record: A version of this preprint was published at Nature Communications on July 26th, 2022. See the published version at https://doi.org/10.1038/s41467-022-31849-5.

Dirac-Source Diode with Sub-unity Ideality Factor

Gyuho Myeong[1†], Wongil Shin[1†], Seungho Kim[1], Hongsik Lim[1], Boram Kim[1], Taehyeok Jin[1], Kyunghwan Sung[1], Jihoon Park[1], Michael S. Fuhrer[2], Kenji Watanabe[3], Takashi Taniguchi[3], Fei Liu[4**], Sungjae Cho[1*]

An increase in power consumption necessitates a low-power circuit technology to extend Moore's law. Low-power transistors, such as tunnel field-effect transistors (TFETs)[1-5], negative-capacitance field-effect transistors (NC-FETs)[6], and Dirac-source field-effect transistors (DS-FETs)[7-10], have been realised to break the thermionic limit of the subthreshold swing (SS). However, a low-power diode rectifier, which breaks the thermionic limit of an ideality factor (η) of 1 at room temperature, has not been proposed yet. In this study, we have realised a DS diode, which exhibits a steep-slope characteristic curve, by utilising the linear density of states (DOSs) of graphene[7]. For the developed DS diode, η < 1 for more than two decades of drain current with a minimum value of 0.8, and the rectifying ratio is large (> 10^5). The realisation of a DS diode paves the way for the development of low-power electronic circuits.

[1] Department of Physics, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea

[2] ARC Centre of Excellence in Future Low-Energy Electronics Technologies, and School of Physics and Astronomy, Monash University, Clayton, Victoria 3800, Australia

[3] National Institute for Materials Science, Namiki Tsukuba Ibaraki 305-0044, Japan

[4] Institute of Microelectronics, Peking University, Beijing, 100871, China

[†]These authors contributed equally to this work

* Corresponding author, S. C, Email: sungjae.cho@kaist.ac.kr

** Corresponding author, F. L, Email: feiliu@pku.edu.cn

Power consumption of integrated digital devices sets the ultimate limit to downscaling and Moore's Law[11]. Reducing power consumption has been thwarted by fundamental limits on the operating voltage set by thermionic emission[12]. For an ideal thermionic device the dependence of current I on voltage V is expressed through the subthreshold swing $SS = [d\log(I)/dV]^{-1} = (k_BT/q)\log(10) \approx 60$ mV/dec at room temperature, where k_BT is the thermal energy and q is the elemental charge.

Two-dimensional (2D) van der Waals (vdW) materials[13,14] have been proposed for various schemes to overcome the thermionic limit (SS = 60 mV/dec) of metal-oxide semiconductor field-effect transistors (MOSFETs) in nonconventional transistors such as TFETs, NC-FETs, and DS-FETs[1-10]. In particular, DS-FETs use the linear energy dispersion relationship of graphene, producing a super-exponential change in the DOS with energy[15]. As a result, DS-FETs have achieved a smaller SS than that of a MOSFET, with a large drive current[7-10].

Integration of heterogeneous electronic components on a single low power-consumption platform is highly desirable to enable application such as the Internet of Things. Schottky diodes are important electronic components with low operation voltage and high current[16], and have many useful applications such as rectifiers， mixers, selectors， switches， photo detectors and solar cells[16]. Although there has been considerable development of low-power transistors, steep slope diode (or diode) rectifiers that overcome the thermionic limit ($\eta < 1$) of conventional diodes have not been proposed yet, but will be necessary for device integration with low-power transistors. Herein, we propose a DS diode as an essential element for low-power circuits. The DS injects cold electrons without a long thermal tail above the potential barrier in the channel (Fig S1). Our proposed DS diode consists of a graphene/MoS_2/graphite heterojunction, where graphene acts as a cold electron injector, whereas the graphite/MoS_2 interface provides a Schottky barrier for rectification. The MoS_2 channel was chosen because of its high-gate tunability and mobility[17]. The minimum and average values of η for the DS

diode are 0.76 and less than 1 over more than two decades of current at room temperature, respectively, with a high rectifying ratio (> 10^5).

The proposed DS diode device (Fig. 1a) consists of four components: (i) an n-type monolayer MoS_2 channel, (ii) a graphene DS neutral at a zero gate-voltage, (iii) a graphite drain-contact to form a Schottky barrier between the graphite and monolayer MoS_2 for electrical rectification with a bias voltage, and (iv) metal (back and top) gate electrodes to tune the Fermi levels of 2D materials. Two-dimensional van der Waals epitaxy was performed inside an Ar-filled glovebox until the heterostructure was encapsulated by hexagonal boron nitride (hBN) to avoid any contamination through air exposure or chemicals (Fig. S2). Unlike a metal contact, a graphite contact with the monolayer MoS_2 forms a non-reactive clean interface[18], preventing Fermi-level pinning[19] (Fig. S3 and Fig. S4). The diode has a local top-gate and a global back-gate. The top gate only modulates the channel of the monolayer MoS_2 band, whereas the global back gate affects the graphene/MoS_2/graphite heterostructure. The gate-dependent electrical measurements (Fig. S5) indicate that the Dirac point of hBN-encapsulated graphene not on MoS_2 is located at $V_{BG} = 0$, whereas the Dirac point of graphene on MoS_2 is located at $V_{BG} \approx -18$ V because of the n-doping caused by the monolayer MoS_2[20].

Fig. 1b presents the characteristic drain current (I_D) versus bias voltage (V_{bias}) curve for the DS diode at $V_{BG} = -30$ V. At $V_{BG} = -30$ V, the G1 and G2 regions of graphene are p-type. When a bias voltage is applied to the graphene, electrons are injected from the p-type graphene source to the graphite drain. The electrical measurements reveal a nearly Ohmic graphene/MoS_2 contact and a Schottky barrier of the graphite/MoS_2 contact (Fig. S6). When a negative back-gate voltage is applied, the Schottky barrier height increases, and the device current is mainly modulated by the Schottky barrier at the interface between the graphite and monolayer MoS_2.

The performance of a Schottky diode is mainly characterised by two figures of merit. One is

the rectifying ratio, which refers to the ratio between the on and off currents ($R = \frac{I_{on}}{I_{off}}$), whereas the other is η, which is the slope representing the change in drain current with a bias voltage and can be obtained from the following Schottky diode equation:

$$I_D = I_S\left(1 - e^{qV_{bias}/\eta k_B T}\right), \qquad (1)$$

where q is the elementary charge, V_{bias} is the applied bias voltage, η is the ideality factor, k_B is the Boltzmann constant, T is the temperature, and I_D and I_S are the drain and leakage currents, respectively. Eqn (1) corresponds to $SS = (\eta k_B T/e)\log(10)$ hence values $\eta < 1$ correspond to SS below the thermionic limit. The characteristic curve at a negative gate voltage in Fig. 1b exhibits rectification behaviour with $\eta < 1$ observed over more than two decades of drain current, a minimum η of 0.76, and a large rectifying ratio ($> 10^5$).

To explore the switching mechanism of DS diode, we developed analytical formula for ideality factor and performed numerical device simulations (See supplementary materials 7). Both the two methods show that the ideality factor less than 1 is obtained in DS diode due to the linear density of states of graphene. The switching slope of a diode is determined by the energy-dependent current density injected from an electrode, which is related to DOS and the distribution function. Graphene has a linear energy-dependent electronic DOS near the Dirac point, which is different from conventional metals with a constant DOS around the Fermi level. Therefore, the thermal tail of the Boltzmann distribution function is suppressed by the Dirac point tuned to the off-state region by doping. Namely, as the bias voltage is decreased on the graphene electrode as shown in Fig. 1c, the part of current density related to the distribution function is increased exponentially similar as conventional metals, which results in the ideal factor limit of 1. While, the injected DOS over the top of channel barrier is also increased linearly from off-state to on-state, as shown in Fig. 1c. Therefore, current is increased super-exponentially and the ideal factor below 1 is obtained in the diode with graphene electrode as the injection source.

Therefore, the switching slope of a diode, i.e., $\eta < 1$, is obtained in the diode with a graphene electrode as the cold electron injection source because of the linear DOS of the DS. Detailed simulation results are presented in Fig. S7. Quantum transport simulations show that DS diode has promising device performance. The ideality factor as small as 0.69 is obtained in the simulated DS diode and is less in 1 in more than five decades of current at room temperature. The on-state current is larger than 10^3 μA/μm and the rectifying ratio is over 10^7.

Fig. 2a presents the I_D-V_{bias} characteristic curve of the DS diode at different back-gate voltages. For the proposed DS diode to work as a diode, an asymmetric Schottky barrier height between the source and drain is necessary[21-24]. To satisfy this condition, we placed asymmetric graphene and graphite contacts with the monolayer MoS_2 channel with gates. Without gate modulation, graphene has a work function of 4.3–4.7 eV from a monolayer to a few layers[25-27]. Because the work function of graphene (~4.3 eV) does not differ significantly from the electron affinity of MoS_2 (~4.2 eV)[28-31], the Schottky barrier height at the graphene/MoS_2 interface is negligible, compared to the Schottky barrier height at the graphite/MoS_2 interface. This also indicates that the Dirac point of pristine graphene is located near the conduction band edge of MoS_2. Fig. S8 indicates that the graphene/MoS_2 device shows an almost Ohmic IV curve, whereas graphite/MoS_2 does not show an Ohmic IV curve at room temperature. Fig. 2a shows that as the gate voltage decreases, the rectification behaviour becomes dominant at negative gate voltages. As the back-gate voltage exceeds $V_{BG} > 0$, non-diode I_D-V_{bias} characteristic curves appear.

To clarify the origin of the gate-dependent modulation of the I_D-V_{bias} characteristic curves, we measured the modulation of the Schottky barrier height with back-gate voltages from the activation energy in the reverse bias regime. The Schottky diode equation (Eq. 1) can be rewritten as

$$I_D = AA^*T^{\alpha}e^{-q\Phi_B/k_BT}\left(1 - e^{\frac{qV_{bias}}{\eta k_BT}}\right), \quad (2)$$

where A is the area of the Schottky junction, A^* is the Richardson constant, $\alpha = 3/2$ is an exponent for a two-dimensional semiconducting system[32], k_B is the Boltzmann constant, q is the elementary charge, T is the temperature, and Φ_B is the Schottky barrier height. When a large negative bias in absolute value is applied, i.e., $e^{qV_{bias}/k_BT} \approx 0$, the saturated drain current is proportional to $T^{3/2}e^{-q\Phi_B/k_BT}$. The inset of Fig. S4a shows a plot of $\ln(I_{sat}/T^{3/2})$ versus $1/k_BT$ in the reverse bias saturation regime (V_{bias} = +1 V). We extract Φ_B for a given V_{BG} from the slope of each curve. Fig. S4a shows the Schottky barrier height obtained from the slope of each curve in the inset of Fig. S4a. As shown in Fig. S4b, in the highly positive V_{BG} regime, the device shows an almost linear I_D-V_{bias} curve, exhibiting nearly Ohmic contact behaviour (negligible Schottky barriers on both sides of the contacts, graphene and graphite with MoS_2). The adjustable Schottky barrier height with gate voltage indicates that Fermi-level pinning does not exist at the interface between graphite and monolayer MoS_2. This absence of Fermi-level pinning is owing to the defect- and disorder-free interface between two-dimensional materials, graphite and monolayer MoS_2[18,19].

To prove that the proposed diode is operated via cold carrier injection from a graphene DS at negative back-gate voltages, we measured the SS to determine if it showed sub-thermionic values. Fig. S8a shows the characteristic I_D versus top-gate voltage (V_{TG}) transfer curve under the working conditions of the DS-FET, i.e., $V_{BG} < -18$ V, where both the G1 and G2 regions of graphene are p-type. When we apply $V_{BG} = -20$ V, graphene regions G1 and G2 become heavy and slightly p-type, respectively. When the top gate placed on the MoS_2 channel is swept from the off state to the on state, the DOS of the graphene increases according to the band diagram presented in Fig. S8c, thereby operating as a DS-FET. As shown in Fig. S8b, the SS value of the device is less than 60 mV/dec, which indicates that the proposed diode acts as a DS-FET owing to the linear energy dispersion relationship of the graphene-source electrode, resulting in a super-exponential change in the DOS. Both DS-FET and DS diode have the same origin

for SS < 60 mV/dec and $\eta < 1$.

Fig. 3 shows the I_D-V_{bias} characteristic curve in the steep-slope diode regime at $V_{BG} = -15$, –30, and –45 V, where the graphene is p-doped. At $V_{BG} = -15$ V, region G1 is p-type and region G2 is slightly n-type doped. However, as the negative bias voltage is applied, the top of the Schottky barrier is located at a valence band of graphene region G2. At $V_{BG} < -15$ V, both regions G1 and G2 are p-type. In all the regimes at $V_{BG} = -15$, –30, and –45 V, where the top of the Schottky barrier is located below the Dirac point of graphene regions G1 and G2, η of the device is less than 1 in more than two decades of current owing to the cold charge injection from the DS at a forward bias ($V_{bias} < 0$). The minimum η that we measured in one decade of current is 0.76. The red dotted line in Fig. 3 is an ideal diode curve ($\eta = 1$) in the forward bias direction. The DS diodes in these gate-voltage regions show rectification ratios exceeding 10^5 at $V_{BG} = -15$ V (more than 10^4 when $V_{BG} = -30$ V and more than 10^3 when $V_{BG} = -45$ V). We note that the device leakage current level is limited by the leakage currents (~ 50 pA) from the measurement equipment (Fig. S9b). Therefore, the reverse bias leakage current level from the diode should be lower than the measured values.

In conclusion, we successfully demonstrated the first DS diode that operates based on cold charge injection from a graphene source owing to the linear DOS and a Schottky barrier at the interface between graphite and monolayer MoS_2. As the linear DOS of the injected charges from p-type graphene over the top of the Schottky barrier between graphite and n-type monolayer MoS_2 increases linearly from reverse to forward bias, an ideal factor below 1 is obtained in the diode with a graphene electrode as the injection source. Using gate modulation of the Schottky barrier height of the graphite/MoS_2 junction, gradual switching between the diode and non-diode behaviours was also observed. The fabricated DS diode presents a minimum η as low as 0.76 in one decade of current, and it remains less than 1 for more than two decades of current at room temperature, with a high rectifying ratio exceeding 10^5.

Additionally, the device shows SS < 60 mV/dec for the same origin as that for $\eta < 1$. The realisation of a steep-slope DS diode paves the way for the development of low-power circuit elements and energy-efficient circuit technology.

Methods

Device fabrication

We first prepared monolayer MoS_2, graphene, graphite, and hBN flakes on a 90 nm Si/SiO_2 wafer via mechanical exfoliation from bulk crystals in an Ar-filled glove box (< 0.1 ppm of H_2O and O_2) to maintain clean surfaces and prevent contamination from air exposure. Monolayer MoS_2 and graphene were identified using the optical contrast and Raman spectroscopy. Each piece was picked up using a standard dry transfer method with a polydimethylsiloxane (PDMS) stamp covered with a polycarbonate (PC) film and transferred onto a 285-nm wafer. The PC film was washed with chloroform, acetone, and isopropyl alcohol (IPA). Then, standard e-beam lithography and CF_4/O_2 plasma etching, followed by e-beam deposition, were used to place electrical contacts on the vdW layers. Additional e-beam lithography and deposition were performed to place the gate electrode (Fig. S2).

Measurement

To obtain a transfer curve, we performed DC measurements from room temperature to high temperatures in a home-built measurement vacuum chamber. Yokogawa 7651 and Keithley 2400 were used to bias the DC voltages to the source and gate electrodes. A DDPCA-300 preamplifier was used to amplify the drain current ($\times 10^6$) and convert it to a voltage, and this signal was measured using a Keithley 2182a nanovoltmeter (Fig. S8a).

Acknowledgments

We thank J. Lee for helpful discussions. S. C. acknowledges support from Korea NRF (Grant Nos. 2019M3F3A1A03079760, 2020M3F3A2A01081899, and 2020R1A2C2100258).F.L acknowledges support from NSFC (Grant No. 61974003) and the 111 Project (Grant No. B18001). M.S.F. acknowledge support from the ARC (CE17010039).

Author contributions

S. C. conceived and supervised the project. G.M and W.S. fabricated devices and performed measurements. K.W. and T.T. grew high-quality hBN single crystals. S.K., J. P., K. S., H.L., B.K., and T.J. assisted high-temperature transport measurements. F.L. developed the theoretical model and performed device simulations. S. C., G.M., W.S., M.S.F., and F.L. analyzed the data. S.C. and G.M. wrote the manuscript. All the authors contribute to editing the manuscript.

Competing interests

The authors declare no competing financial interests.

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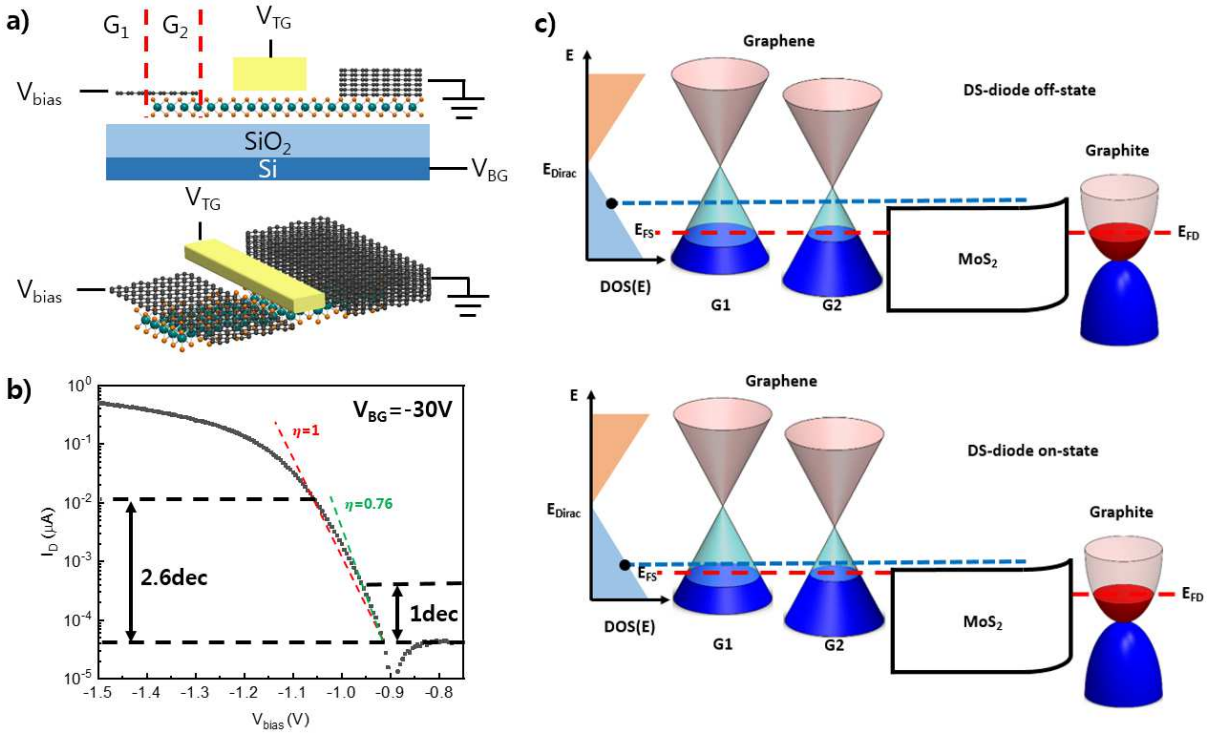

Figure 1. a Schematic image of graphene/MoS_2/graphite heterojunction diode. We used graphene as a source and graphite as a drain. The graphene source can be divided into two regions, G1, which is outside MoS_2, and G2, which is on MoS_2. **b** Characteristic I_D-V_{bias} curve in our device, which exhibits $\eta = 0.76$ in 1 decade of current and an average $\eta < 1$ in more than two decades of current. The rectifying ratio of our device is larger than 10^5. **c** Band diagram of DS Schottky diode, which explains the working principle of cold electron injection from graphene.

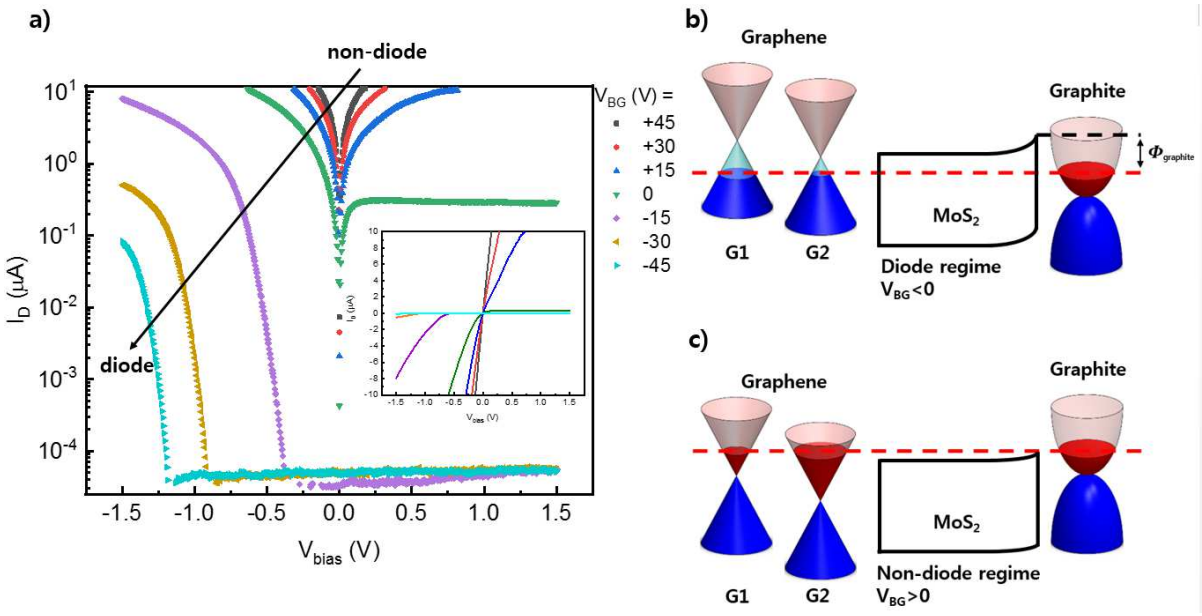

Figure 2. Characteristic I_D-V_{bias} curve for various V_{BG} and its band diagram. a Characteristic I_D-V_{bias} curve in the range of V_{BG} = –45 ~ +45 V. As V_{BG} decreases, change from non-diode to diode behaviour is observed. **b** Band diagram when V_{BG} < 0 (diode regime). Owing to the larger work function of graphite than that of graphene, the device becomes a graphite/MoS_2-interface Schottky barrier-dominant Schottky diode. **c** Band diagram when V_{BG} > 0 (non-diode regime). Owing to the weak Fermi-level pinning between the 2D metal and MoS_2, the Schottky barrier height of the graphite/MoS_2 interface can be modulated. As V_{BG} increases, the work function of graphite decreases, and the Schottky barrier height of the graphite/MoS_2 interface decreases.

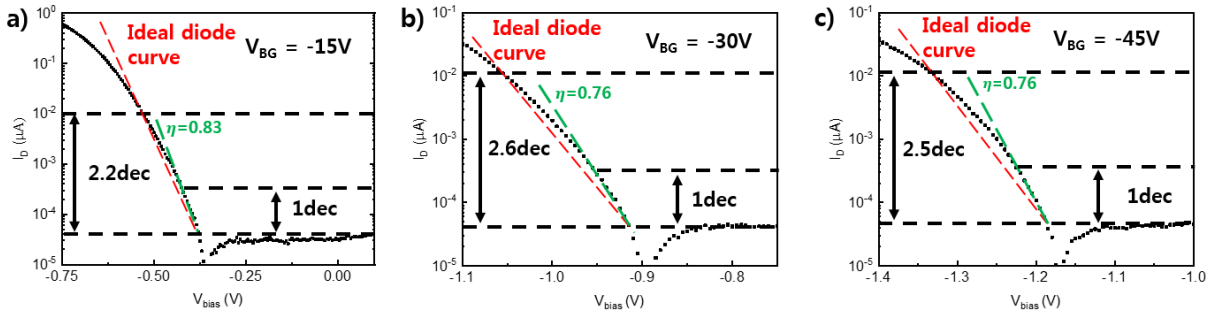

Figure 3. Slopes of DS Schottky diode versus ideal diode and recorded ideality factor in 2D vdW material-based diode. Comparison of slopes between the proposed DS Schottky diode and an ideal diode. Black and red dotted data represent those of the DS Schottky diode and an ideal diode, respectively. The DS Schottky diode exhibits an average η of 1 for 2.2, 2.6, and 2.5 decades when V_{BG} = –15, –30, and –45 V, respectively.

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