A Novel Design of Heterojunction Double Ferroelectric MOSFET (HDF-MOSFET) with Steep Subthreshold Slope and High Ion/Ioff Current Ratio

MOJTABA HOSSEIN ZADEH SANI (mojtabasani69@gmail.com)
Tianjin University https://orcid.org/0000-0002-4723-5013
Shujuan Li
University of Jinan

Research Article

Keywords: SF-MOSFET, DF-MOSFET, HDF-MOSFET, Ion/Ioff Ratio, Memory Windows (MW)

Posted Date: February 11th, 2022

DOI: https://doi.org/10.21203/rs.3.rs-1015278/v1

Abstract

In this work, three novel structures using ferroelectric material are designed and simulated. The proposed structures are Improved Priority, Single Ferro (SF-MOSFET), Double Ferro (DF-MOSFET), and Heterojunction Double Ferro (HDF-MOSFET), respectively. Unlike other structures, these structures have a contact gate and two ferroelectric layers, and an insulation layer between these layers. HfO_2 is used instead of the common perovskite ferroelectric layers such as zirconium lead titanate ($PbZrTiO_3$) and strontium bismuth tantalum ($SrBi_2Ta_2O_9$), which makes it compatible with the CMOS process as well as the scalability of the device. Ferroelectric layers, Insulation and Ferroelectric layers are stacked (F-I-F). Placing double ferro layers in the form of a stack increases the polarization effects and improves the application of the structure in memory. The memory performance can be saved even after the power is turned off and the readout properties are not destructive for double ferroelectric stack. perovskite Lead Zirconium Titan ate (PZT) is chosen as the ferroelectric materials. The DF-MOSFET structure, value of on-state current $I_{on}=10^{-2}$, off-state current $I_{off}=10^{-15}$, and memory Windows MW=0.9V for memory applications. In the barrier layer of HDF-MOSFET structure, from composite materials that have used TiO_2=60% and HfO_2=40%, the amount of $I_{on}=10^{-4.8}$, $I_{off}=10^{-35.2}$ and $I_{on}/I_{off} = 2.51\times10^{35}$ is obtained, which is a suitable application for high frequency.

1. Introduction

Field effect transistors are a group of transistors in which the current is controlled by an electric field. Due to the fact that in these transistors only one type of charge carrier (free electron or hole) is involved in creating electric current, they can be considered as unipolar transistors as opposed to bipolar transistors (in which the majority and minority carriers simultaneously play a role). Are placed. [1] Field effect transistors have source, drain and gate tripods. These transistors are divided into two groups: MOSFET and J_{ift}. In this type of transistors, unlike connecting bipolar transistors, which control the current of the emitter and collector with the input current to the base, the control of the source and drain current is done by applying voltage to the gate [2, 3].

Ferroelectric is a property in materials that causes permanent electric dipoles to form on the surface of a single cell due to the regular arrangement of atoms / molecules, so that their direction can be adjusted by applying an external electric field. Ferroelectric is a nonlinear dielectric with properties such that a certain range is independent of permeability in the intensity of the applied electric field. Dielectric displacement is the sensing electric field applied using the hysteresis loop profile. The dielectric constant of these materials is very high independently and is in the threshold of 1000 to 10,000. The dielectric parameters specifically depend on the temperature and the ferroelectric properties and are only within the defined temperature range. Dielectric polarization occurs in the absence of an external electric field, and this polarization can be coupled to apply an electric field. Scientists have developed a silicon oxide that could create a state of ferroelectricity to pave the way for the production of low-consumption, efficient electronic memory. Ferroelectricity is a property by which materials can be electrically polarized. The

polarity of the material can be rotated by applying an external electric field, which is used in long-term storage of data. In a research, the ferroelectric phenomenon and its properties are studied. Crystals with constant dipole moment are known as polar crystals. The permanent dipole moment is defined as M = eiri, where ri is the paraelectric distance ei from the origin and summation is performed on all the loads present in the single cell. Ferroelectric crystals are a special type of polar crystals in which the direction of spontaneous polarization can be reversed by applying an electric field. This switching is known and is associated with hysteresis. In most cases, these objects are similar to ferromagnetic bodies in which the direction of the magnet is reversed by changing the direction of the magnetic field, and this is the reason for choosing the name ferroelectric for these objects. Ferroelectrics are a subset of piezoelectric materials and have extensive properties such as high electrical polarization, strong piezoelectric capability, nonlinear optical activity, and remarkable nonlinear dielectric behavior. These features are used for various applications in electronic devices such as sensors, actuators, IR detectors, memories that are stored after a power outage [4.-10].

One of the major advantages of ferroelectric materials is their ability to be stored in memory. In fact, a ferroelectric material has spontaneous and reversible polarization, even in the part without electric field, and the memory program is based on the hysterical behavior of polarization with electric field [11–13]. The description curve of the first polarization of a ferroelectric device is called the first polarization curve. When an alternating electric field is applied to a ferroelectric, a hysterical behavior is created according to the intensity of the applied field. At zero field strength, there are two equally stable polarization modes, + Pr or -Pr, depending on the polarization time. This behavior of ferroelectric materials allows the design of a binary device in the form of a ferroelectric capacitor with a metal-ferroelectric-metal structure that can be reversed. Either of these two modes can be encrypted as —0‖ or —1‖ in the computer memory, and is non-volatile, and even when the electric field is cut off, information is stored in the device because no electric field is required to maintain the state of the device. To change the status of the device, a threshold part (mandatory field) greater than + Ec or –Ec is required. A strong ferroelectric material has a high Pr value and a low Ec value. In order to determine a ferroelectric device, it is necessary to determine the waste behavior and the value of Pr. In addition, because ferroelectric materials have piezoelectricity, spontaneous polarization, and high dielectric constants, they are useful for numerous other applications due to the inherent anisotropy of dielectric properties. For example, the high nonlinear polarization of ferroelectric materials has made these devices promising for electrical and optical devices [14, 15].

To simulate the effects of polarization and hysteresis of ferroelectric materials, the ferroelectric model in the atlas in the simulation code must be used. This model can be activated by setting the "FERRO" parameter in the phrase "MODELS" [16]. Permissibility, used in the Poisson equation, is expressed in Equation (1) as follows:

$$\epsilon(E) = ferro.\,epsp + \frac{ferro.\,ps}{2\delta} \bullet sech^2\left[\frac{E - ferro.\,ec}{2\delta}\right] (1)$$

Where, E is the electric field, *ferro.epsf* is the allowable value of ferro.pr, the residual polarization is in C/cm^2, ferro.ps is spontaneous polarization in C/cm^2 and ferro.ec is the forced field in V/cm. δ can be expressed mathematically as Equation (2).

$$\delta = ferro.ec\left[log\left[\frac{1+\frac{ferro.pr}{ferro.ps}}{1-\frac{ferro.pr}{ferro.ps}}\right]\right]^{-1} \quad (2)$$

There are two main models of ferroelectric materials which are PZT and SBT, in this paper the PZT model is used. In principle, each of the above ferroelectric materials is suitable for memory applications and is also intended for applications by ferroelectric field (FeFETs). These two substances differ in the values of polarization and forced field [17]. Table 1 shows the parameters of these two materials and Figure 1 shows a comparison of the polarization behavior of these two ferroelectric materials.

Table 1
Comparison of Ferroelectric materials of PZT and SBT.

Parameters	Unit	PZT	SBT
P_R	$\mu C/cm^2$	32	8
P_S	$\mu C/cm^2$	40	10
E_C	KV/cm^2	70	30
ε_r	-	250	250

In this paper, we integrate the ferroelectric material into a MOSFET transistor, which has already been done by scientists. But a new work that has been done in this article is to introduce the new double ferroelectric MOSFET (DF-MOSFET) and Heterojunction double ferroelectric (HDF-MOSFET) method, which aims to improve memory applications, performance speed, sub-threshold slope, on and off current and off current. This proposed new method, in addition to being used in MOSFET transistors, can also be tested in TFET transistors and other field effect transistors.

2. Proposed Devices

The proposed devices are designed and simulated in Figure 2 using Atlas section of the Silvaco software. In section (a), the structure is designed with a channel length of L_{ch} =20 nm and a single ferroelectric MOSFET (SF-MOSFET). Instead of the ferroelectric layer, material HfO_2 with a thickness of t_{ferro} = 10 nm has been used and the barrier layer has used oxide insulation with a thickness of $t_{barrier}$ = 40 nm. The substrate layer is made of silicon material with a thickness of 200 nm. Drain and source metals is made

of Ti/Al/Ni/Au materials with thicknesses of 5/20/5/10 nm. The gate is also made of Mo/Au with thicknesses of 5/5 nm. The length of the Schottky gate is L_G = 60 nm and the distance between the gate and the source is L_{GD} = 10 nm. Also, the distance between gate and source is L_{GS} = 10 nm. The total length of the device is L_T = 100 nm and total thicknesses is t_T = 240 nm. Figure 2 (b) shows the proposed double ferroelectric structure (DF-MOSFET), witch a ferro layer below the barrier layer and from TiO_2 material is used instead of Ferreroelectric. The thickness of this layer is t_{ferro2} = 10 nm. The concentration of p^+ doping in the channel layer is 1×10^{16} cm^{-3} and the concentration of n^+ doping is equal to or 1×10^{19} cm^{-3}. The Si_3N_4 material has been used as a passive layer on the device due to its high heat transfer.

The parameters used in the properties of ferroelectric material are *ferro.epsf* = 35, *ferro.ps* = 4.9×10^{-6} C/cm^2, *ferro.pr* = 4.8×10^{-6} C/cm^2 and *ferro.ec* =1.1×10^{6} V/cm, respectively. Figure 2 Overvoltage (VGS-VTH, where VTH is the threshold voltage) Dependent drain current (I_{DS}) for SF-MOSFET with L_{ch} = 20 nm channel length in V_{DS} = 1 V. In order to analyze and compare performance parameters much better, the sub-threshold slope was defined as the average slope between the off-state current and the threshold.

3. Single Ferroelectric Mosfet (Sf-mosfet)

3.1. I-V Curve of Single Ferroelectric Transistor (Linear & dB Scale)

As shown in Figure 2 (a), this structure used a ferroelectric layer that actually does the memory work and a Barrier layer (barrier below the gate metal) to transfer the field electric into the channel layer with length of L_C = 40nm and a gate length of L_G = 60nm. The Barrier layer material is made of HfO_2 and the bottom layer is made of S_iO_2. As can be seen, the yellow area of the silicon is of type p+, that two n+ wells have been created in this area. When positive voltage is applied to the gate metal, the ferroelectric layer does nothing, and in fact the barrier layer does its job and transfers the field electric to the channel layer. The ferroelectric layer has polarization properties that store electron and hole residues in itself. and this residue creates a window called Memory Window (MW). The smaller it is, the better for us. As shown in Figure 3, the transistor is turned off before the V_{th} = -1.8 V, after this voltage (V_{th}), the transistor starts to turn on. By increasing the voltage, we increase the current. We have the maximum current at V = 6V.

According to Figure 4 the amount of on current is I_{on} = 2^{-10} (dB scale) and the amount of off current is I_{off} = 10^{-15} (dB scale) and the amount of memory window is MW = 1.1V. According to the figure, with the gate voltage increasing from V_G = -6V to V_G = 3V, the amount of drain current is increasing and at the same time the electron and hole waste are collected in the ferroelectric layer. When we reduce the gate voltage, we see that the drain current decreases from another path, which the same difference in the return path creates a memory window.

3.2. Effects of Thickness and Materials on SD-MOSFET

In this section (Figure 5), the effects of changing the thickness of the Barrier layer ($t_{barrier}$) and the ferroelectric layer (t_{ferro}) on the I_{on}, I_{off} and MW parameters are investigated. As can be seen in the figure, with thickness changes, it has no effect on the I_{on} and I_{off} parameters. But there are changes in the Windows window that increase the thickness of the stored waste effects. From this figure we conclude that when the ferroelectric thickness is t_{ferro} = 15nm, it has the best memory windows (MW=0.9V) state.

In addition, the effects of the materials type used in the barrier layer on the important parameters are investigated (Figure 7). Here we used three types of materials that have different physical properties and do not have problems in terms of stress and adhesion to barrier layers. The materials used in the barrier layer are HfO_2, Al_2O_3, and Si_3N_4. As shown in the figure 6, all parameters change with the change of the barrier layer material.

4. Double Ferroelectric Mosfet (Df-mosfet)

In the SF-MOSFET structure, the I_{on}/I_{off} current ratio increased slightly. In order to increase the I_{on}/I_{off} current ratio and decrease the amount of memory window, the DF-MOSFET structure is designed and presented. As can be seen in Figure (2b), in this structure, a double ferroelectric material is used, one under the gate and one under the barrier layer. A barrier layer material is HfO_2. In double collapse, the two layers of residue electrical are added together algebraically, so the amount of residue must be doubled. This causes the Ion current to increase and the Ioff current to decrease, resulting in a smaller memory window.

As shown in Figure 6, they are compared in an equal manner, in the double ferro structure the value of the memory window is reduced by 0.1V, the amount of on current is increased by $I_{on}=10^{-0.2}$, and the amount of off current is reduced by $I_{off}=10^{-0.2}$.

4.1. Effects of Materials and Thickness on DF-MOSFET

To determine the best material, the change of material in the barrier layer in the double ferro state is investigated. According to Figure 7, TiO_2 has the best performance compared to HfO_2 and ZrO_2. These parameter improvements include on and off current and memory windows. The amount of on current in the case of the barrier layer is made of TiO_2 is $10^{-1.8}$ amps and the amount of off current is $10^{-15.4}$ and the amount of memory window is 0.6 V.

In this section, we want to investigate the effects of thicknesses of ferroelectric layers (F1, F2) and barrier layer (B) on the parameters of on and off current and memory windows. As can be seen in Figure 8, the thicknesses of the ferroelectric layer and the dam layer are investigated for the two states [(F1=10, B=25, F2=5) & (F1=5, B=30, F2=5)]. Here the ferroelectric material is HfO_2 and the dam material is SiO_2. At first glance, we see that with changes in the thickness of F1, F2, and B layers, the off current has decreased significantly and has reached 10^{-35}. It can be concluded that the leakage current in this type of structure

has been very low, and that prevents power leakage losses. The value of the memory window for F1+F2 = 15nm, and B = 25nm is MW = 0.7V. And for F1+F2=10nm, B=30 memory window equal to MW = 1V. Therefore, as the total F1, F2 decreases and B increases, the amount of memory window decreases. The amount of current in the thickness state B> F2, F2 increases and its value is equal to $I_{on} = 10^{-4.9}$.

Figure 9 shows the others thicknesses of F1, F2 and B layer. As can be seen from the results of Figure 9, it can be concluded that the thicker the ferroelectric layer, the larger the memory window. On the other hand, the off current decreases and as a result the leakage current decreases.

Next, we want to check the linear value of the on current for both HfO_2 and TiO_2 materials. As can be seen in Figure 10, it can be concluded that changes of up to one epsilon in the dB state cause large changes in the linear state. According to the material, material TiO_2 performs better than material HfO_2, and the amount of light current when material TiO_2 is used in ferroelectric layers is equal to $I_D = 0.0125$ A.

4.2. Heterojunction the Barrier Layer in DF-MOSFET (HDF-MOSFET)

After the double ferroelectric idea, we briefly consider another idea. Next idea in addition to examining the effects on the thickness and type of material, we want to divide the barrier layer into two parts and use two different materials. With the transverse changes of the barrier layer, we calculate the values of different important parameters. Figure 11 also shows the best case of the proposed HDF-MOSFET, which is drawn in 3D to have a better understanding of the structure.

As can be seen in Figure 12, the barrier layer has been transformed into two equal parts in the form of heterojunction, and in one part material (HfO_2=50%) and in the other part material (ZrO_2=50%). In this case, the amount of on-state current is $I_{on} = 10^{-4.8}$ and the amount of off-state current is $I_{off} = 10^{-34}$ and the memory window is equal to MW = 0.9 V. The ratio of on-state current to off-state current is equal to $I_{on}/I_{off} = 1.584\times10^{29}$.

In the next case, the barrier layer has been transformed into two unequal parts (HfO_2=80% and TiO_2=20%) in the form of heterojunction, and in one part material HfO_2 and in the other part material TiO_2 is placed. In this case, the amount of on-state current is $I_{on} = 10^{-5}$, the amount of off-state current is $I_{off} = 10^{-34}$ and the memory window is equal to MW = 1 V. The ratio of on-state current to off-state current is equal to $I_{on}/I_{off} = 1\times10^{29}$.

Finally, the barrier layer has been transformed into two unequal parts (TiO_2=40% and TiO_2=60%) in the form of heterogeneity, and in one part material HfO_2 and in the other part material TiO_2.

In this case, the amount of on current is $I_{on} = 10^{-4.8}$, the amount of off current is $I_{off} = 10^{-35.2}$ and the memory window is equal to MW = 0.5 V. The ratio of on-off-state current is equal to $I_{on}/I_{off} = 2.5\times10^{30}$.

According to the obtained results, it can be concluded that when 40% of the barrier layer is made of material HfO_2 and 60% of material TiO_2 is used, it is the best case that the ratio of on-off current reaches its maximum value of $I_{on}/I_{off} = 2.51\times10^{30}$.

Finally, we want to present the process of improving the MOSFET structure using ferroelectric material in the form of a table. Table 2 shows a comparison of important structure parameters such as I_{on}, I_{off}, on/off current ratio, and MW for SF-MOSFET, DF-MOSFET, and HDF-MOSFET structures.

Table 2
Measurement of important parameters in the proposed structures

Proposed	Materials	I_{on} (A/μm^2)	I_{off} (A/μm^2)	MW (V)	I_{on}/I_{off}
SF-MOSFET	HfO_2	10^{-2}	10^{-15}	1.1	1×10^{13}
DF-MOSFET	HfO_2	$10^{-1.5}$	$10^{-15.2}$	0.9	5.01×10^{13}
HDF-MOSFET	HfO_2 & TiO_2	$10^{-4.8}$	$10^{-35.2}$	0.5	2.51×10^{30}

5. Conclusion

In the MOSFET structure, the important parameters are I_{on} and I_{off}, I_{on}/I_{off} ratio and memory window (MW). To have an ideal structure, we need to increase the amount of I_{on} current and decrease the amount of I_{off} current and the memory window. The higher the I_{on}/I_{off} ratio, the performance structure is better. In this paper, we designed and proposed three new structures, in each of which an improvement in the structural parameters was observed. Among the proposed structures, the best HDF-MOSFET structure was introduced, which has an extremely low I_{off} current and minimizes leakage losses ($10^{-35.2}$). On the other hand, the I_{on}/I_{off} current ratio increased significantly and reached 2.51×10^{30}. Finally, the memory window value was reduced to 0.5V. In general, the proposed structure is very suitable for memory applications and work at high power and frequency.

Declarations

Acknowledgements:

Science and Technology Foundation of University of Jinan (XKY1619), Education Research Foundation of University of Jinan (JZ2002).

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Figures

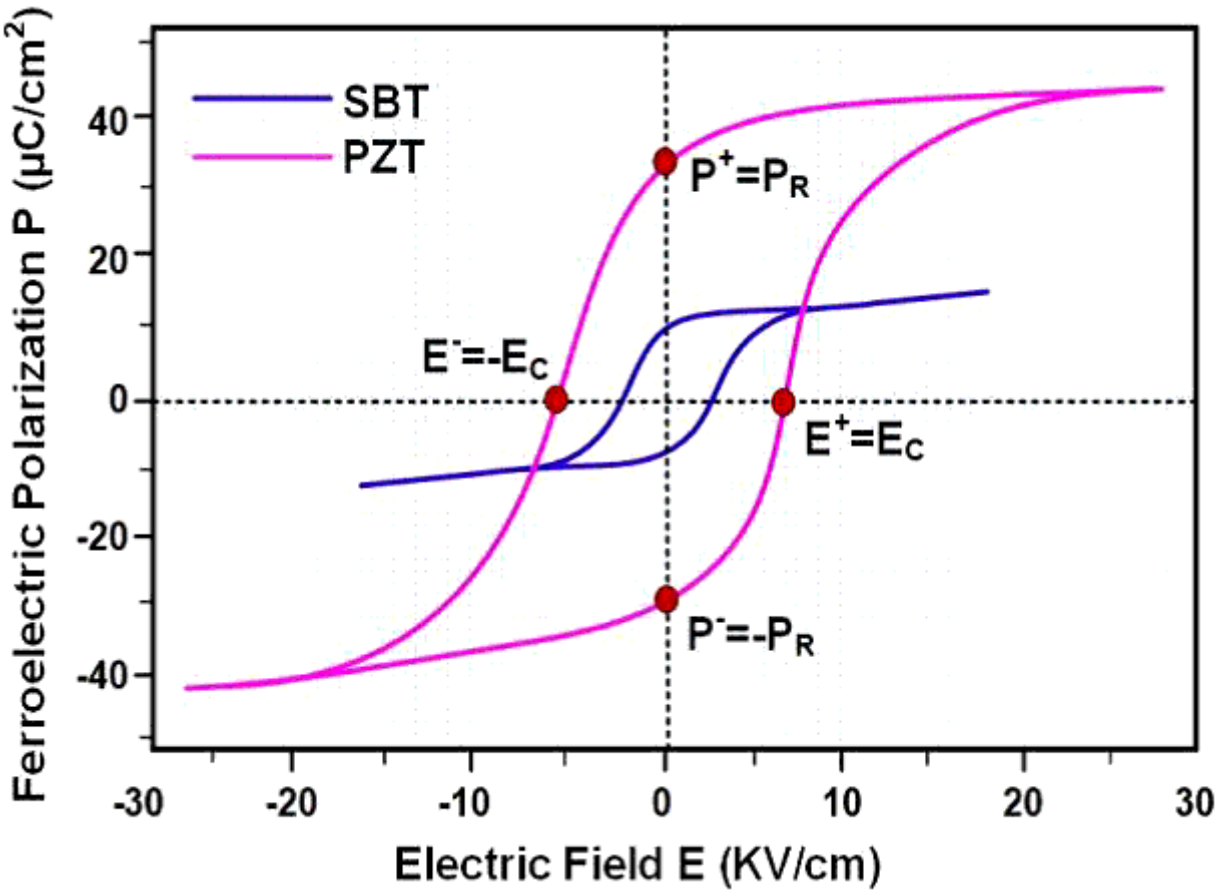

Figure 1

The polarization hysteresis loops of the two main models of ferroelectric materials PZT and SBT.

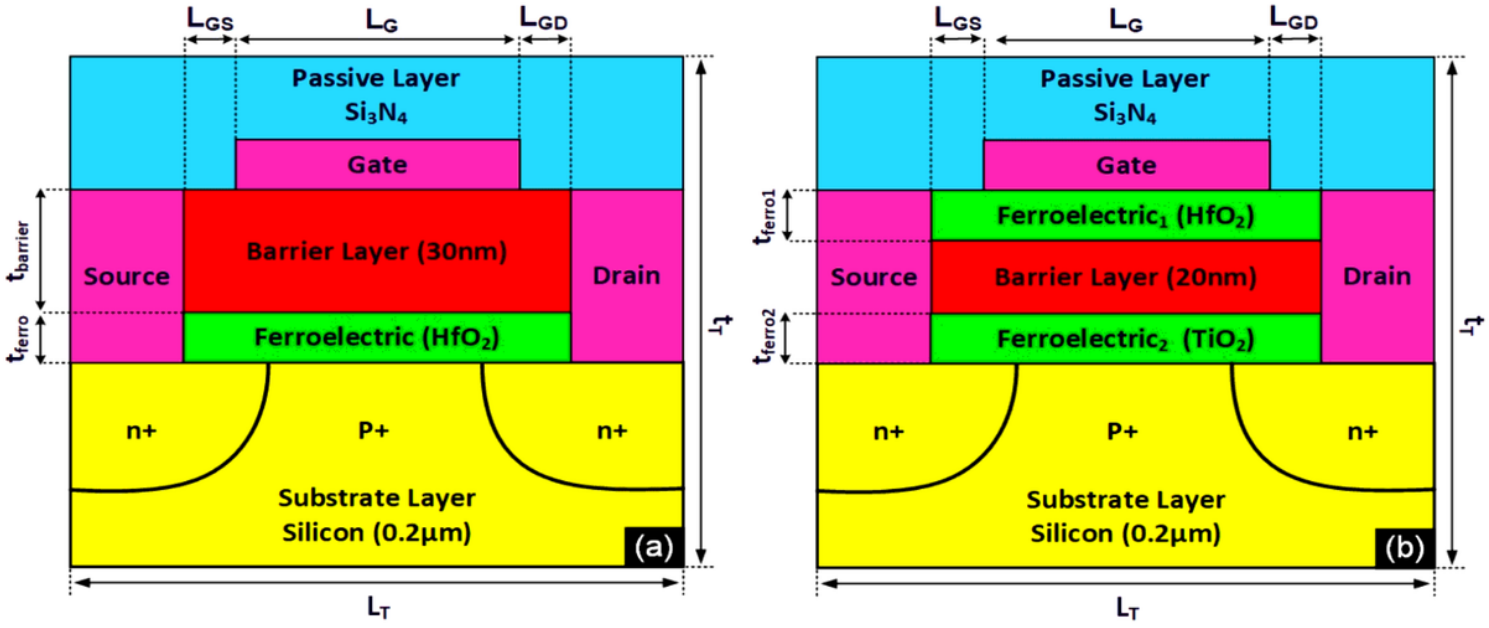

Figure 2

Poroposed Device (a) Single ferroelectric (SF-MOSFET), (b) Double ferroelectric (DF-MOSFET).

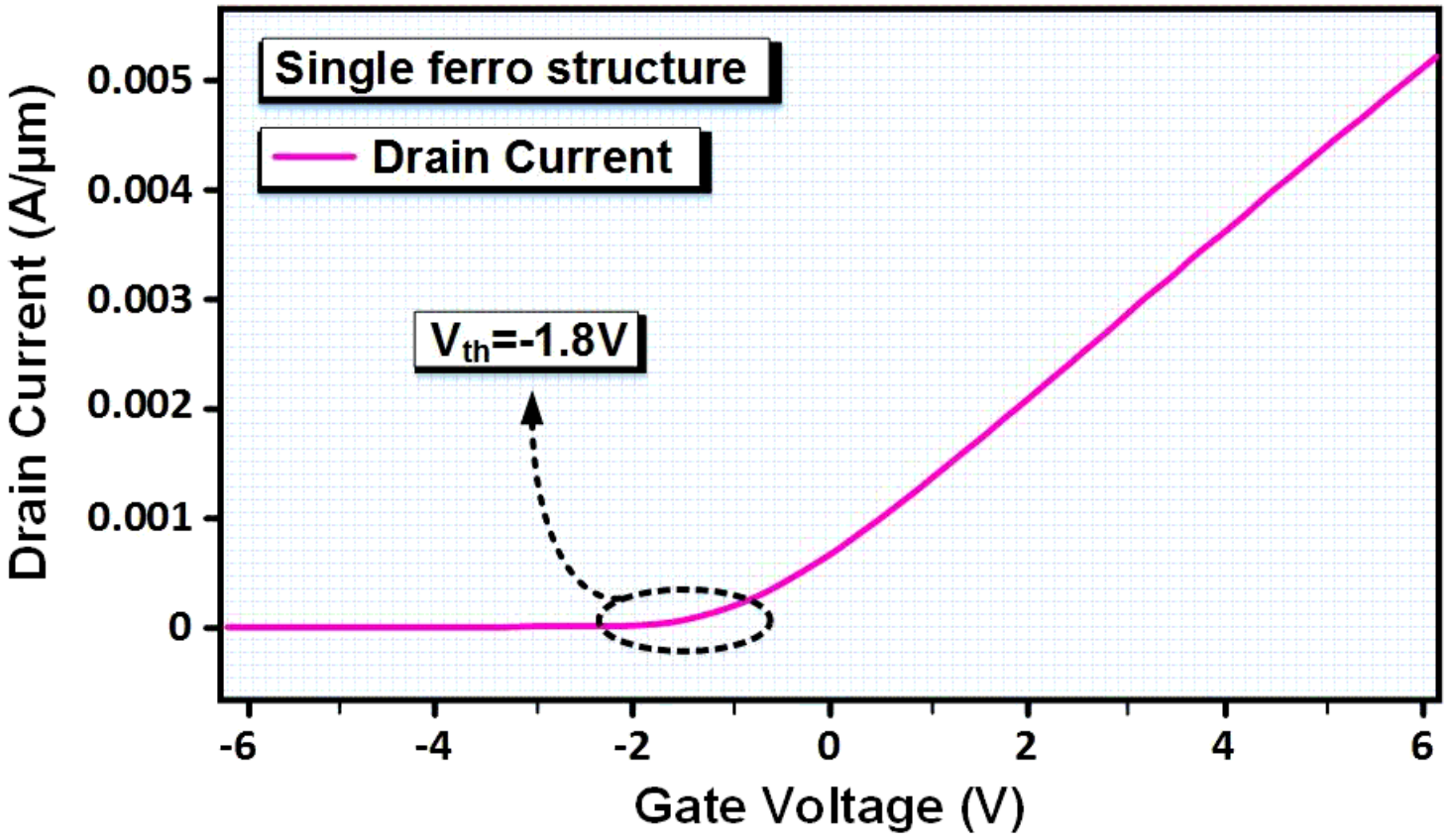

Figure 3

I-V curve of single ferroelectric transistor.

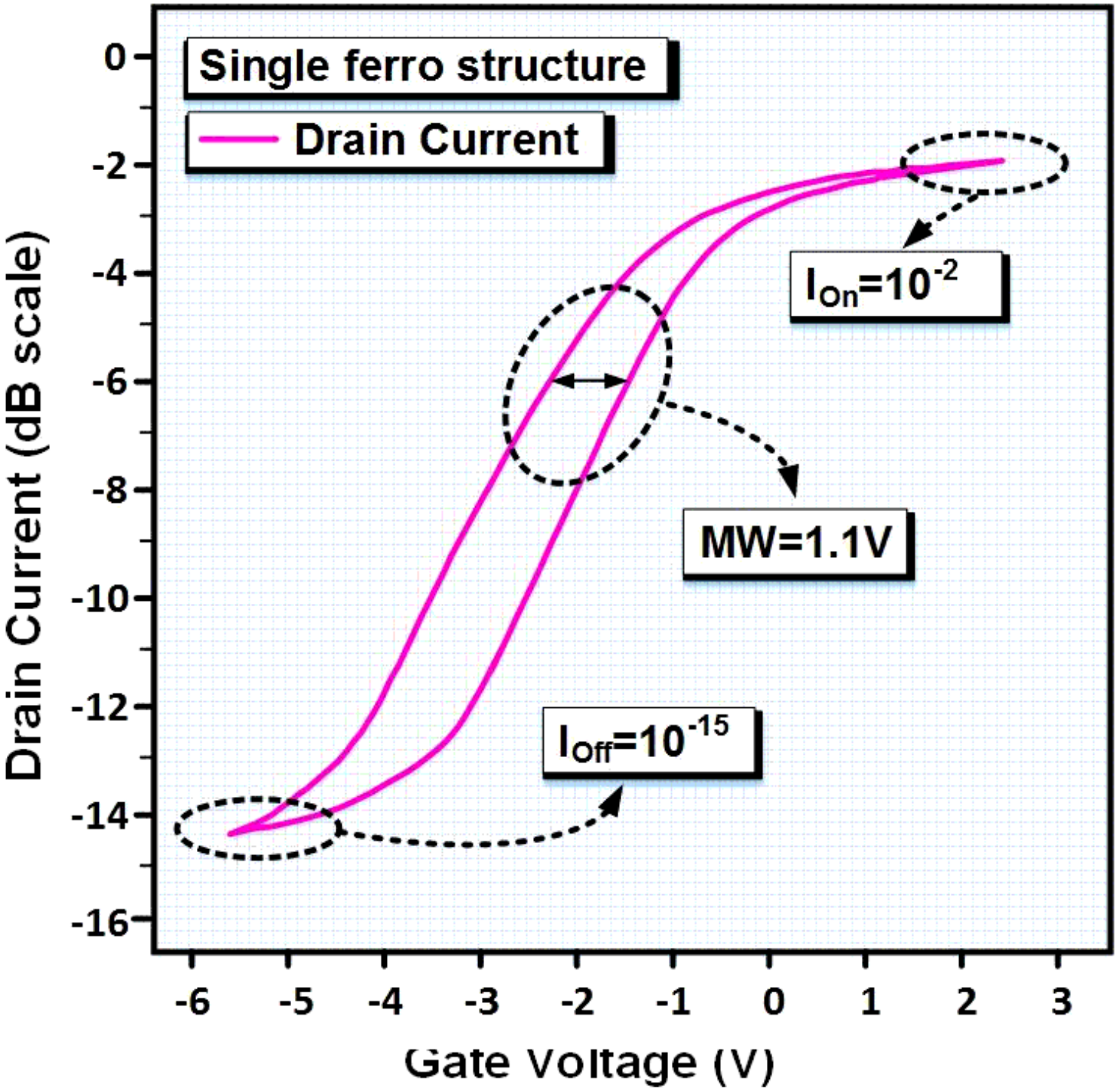

Figure 4

I-V curve of single ferroelectric transistor (dB scale).

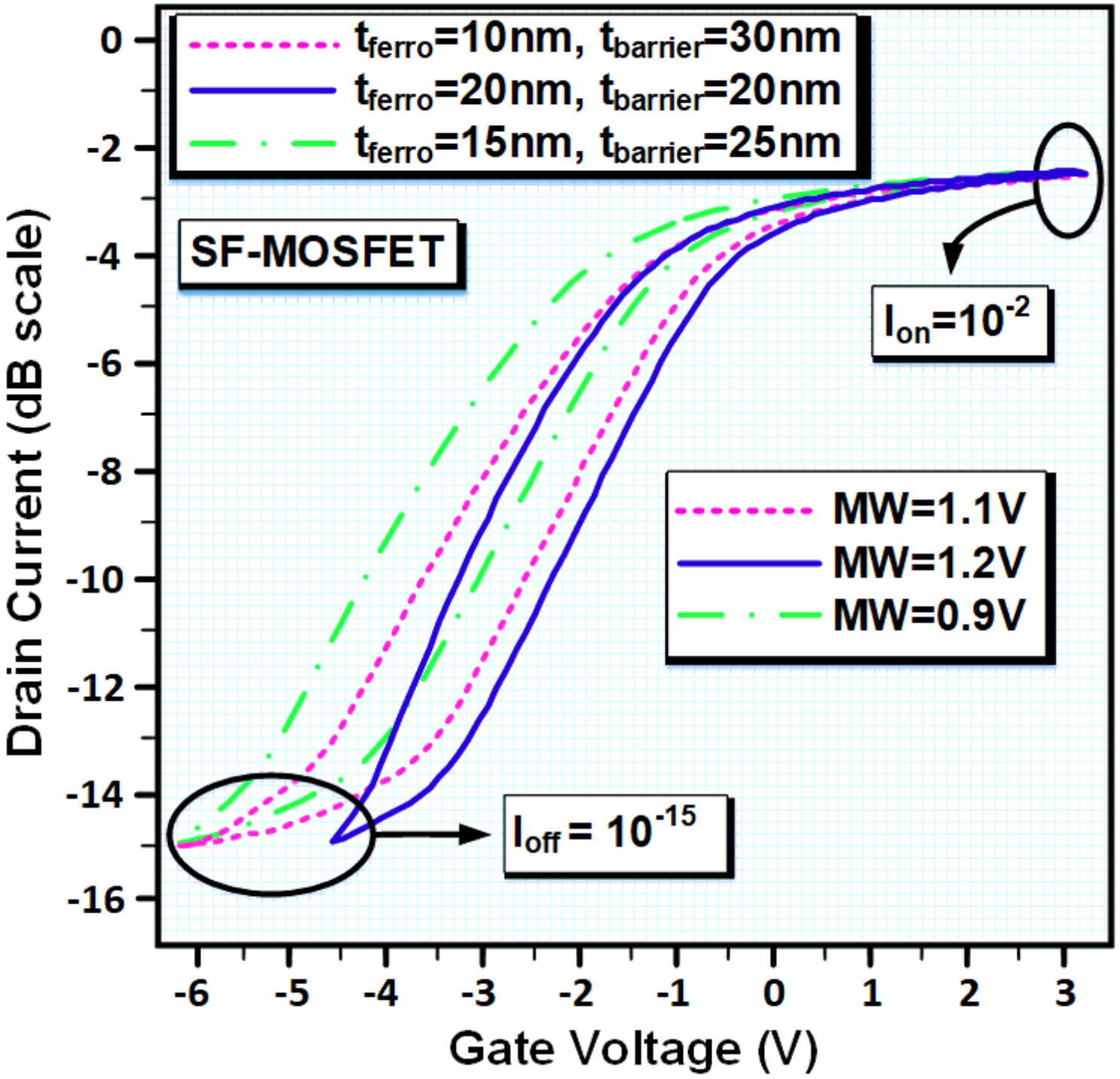

Figure 5

Effects of thickness changes on SF-MOSFET (dB scale).

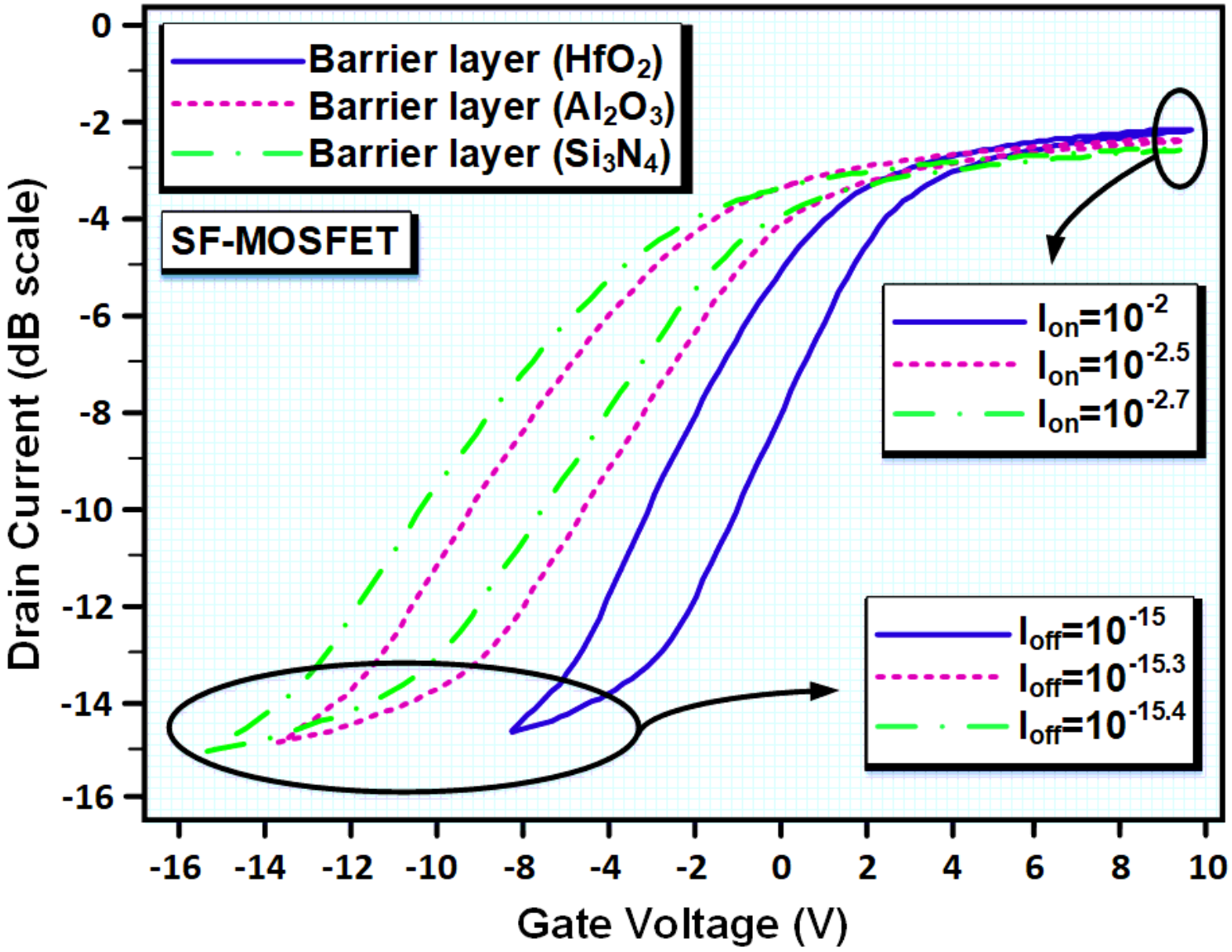

Figure 6

Effects of different materials changes on SF-MOSFET (dB scale).

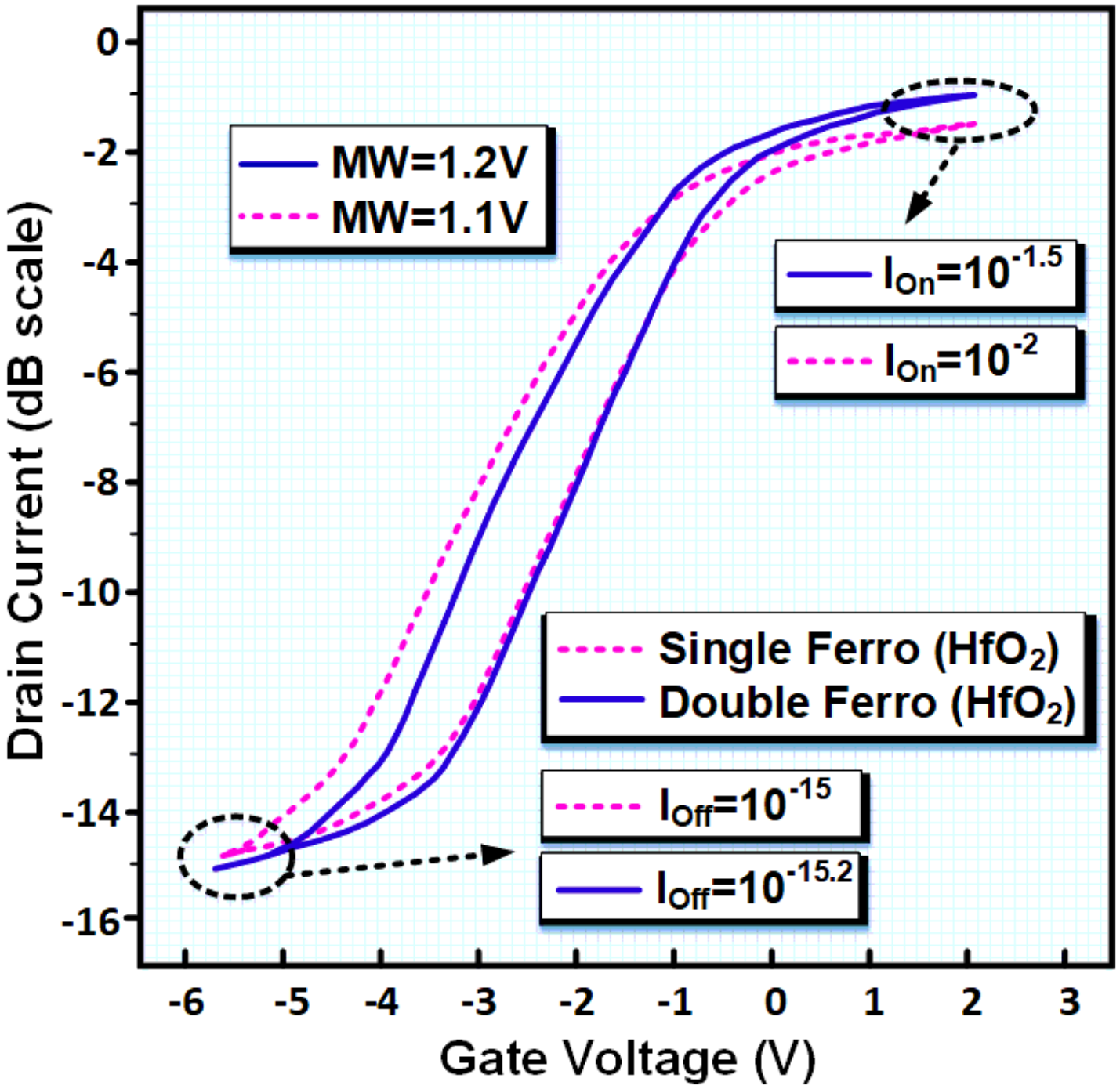

Figure 7

Comparison of single and double output structures.

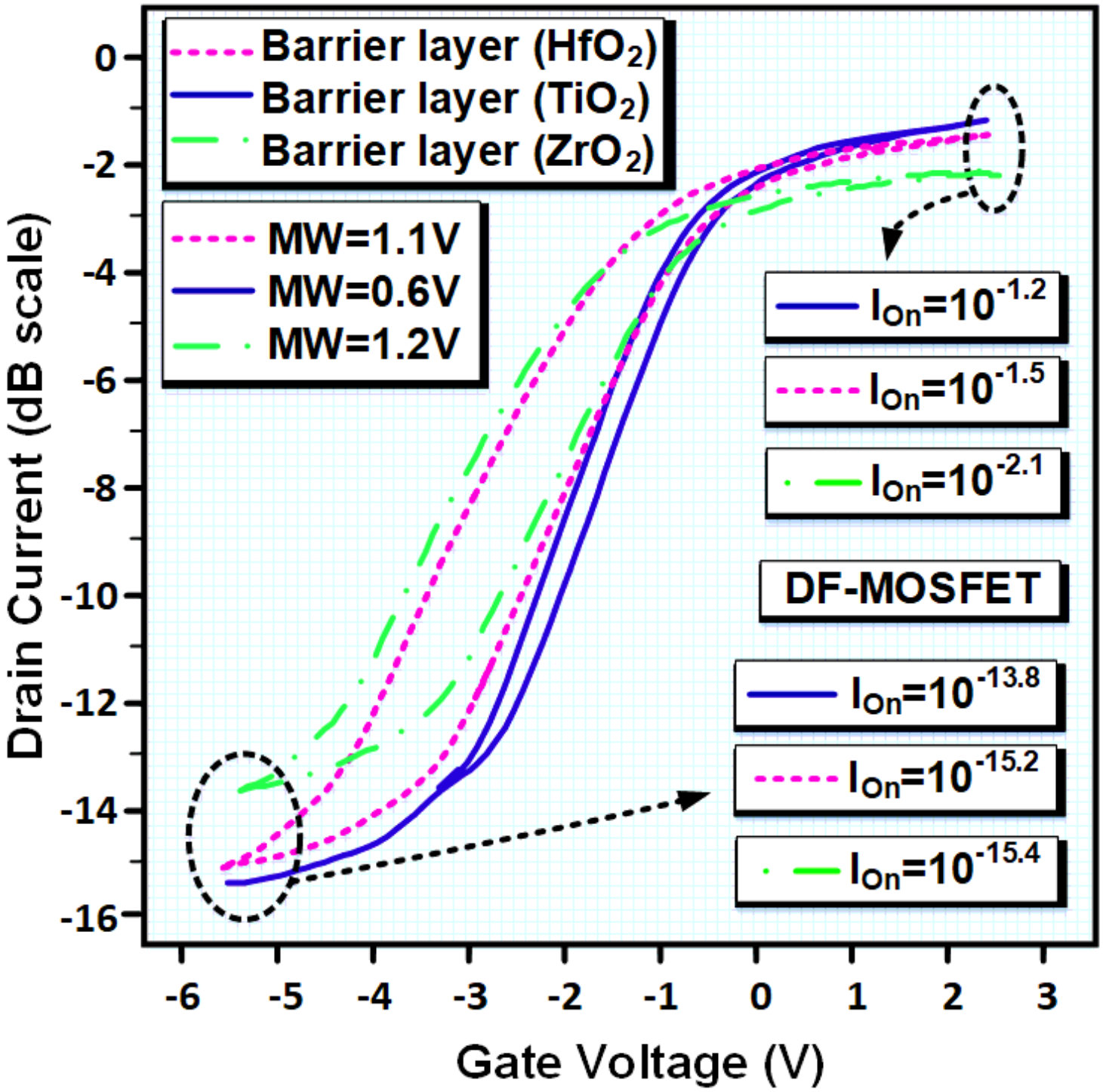

Figure 8

Effects of material changes on the DF-MOSFET structure.

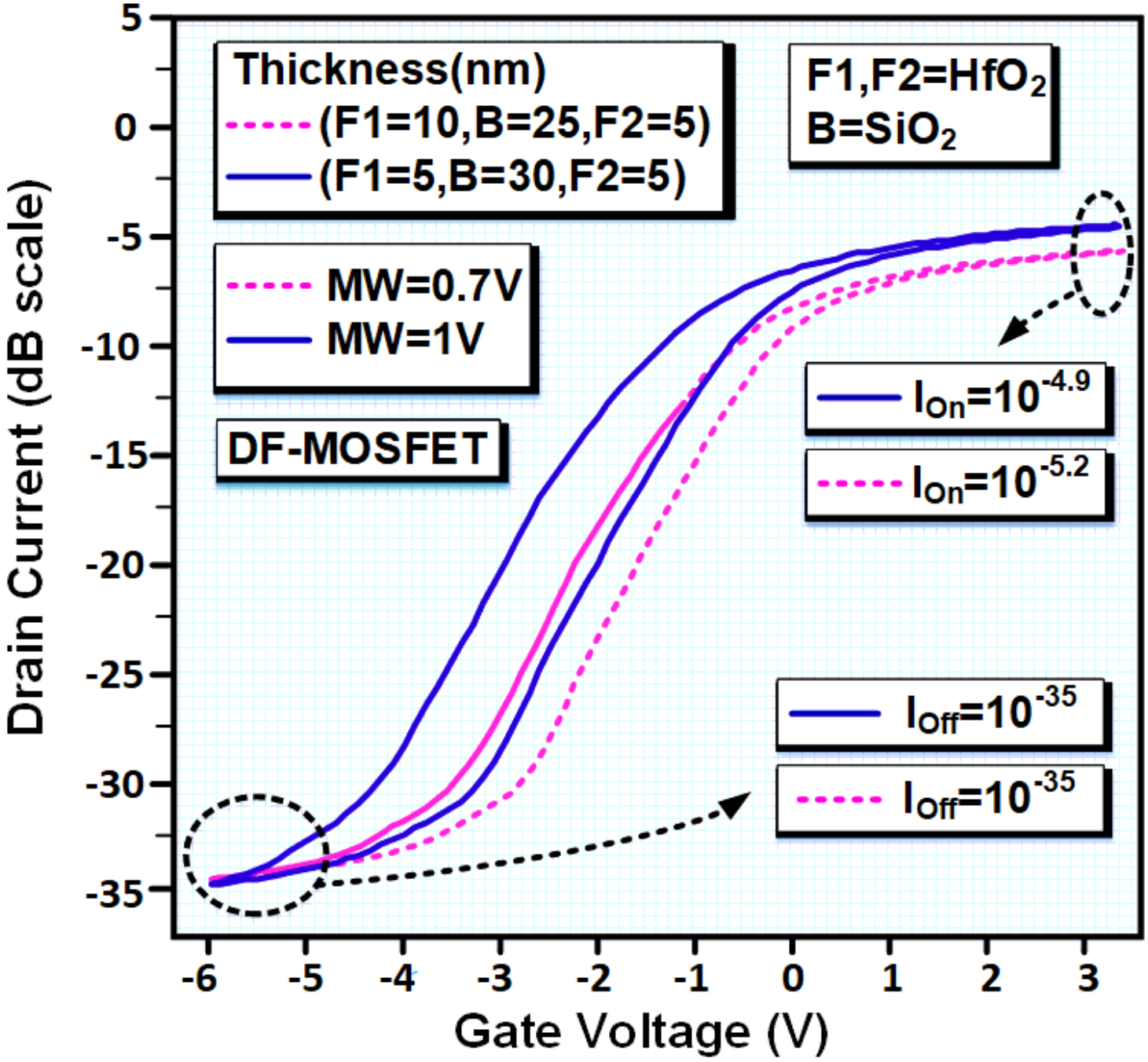

Figure 9

Effects of thickness changes on the DF-MOSFET structure.

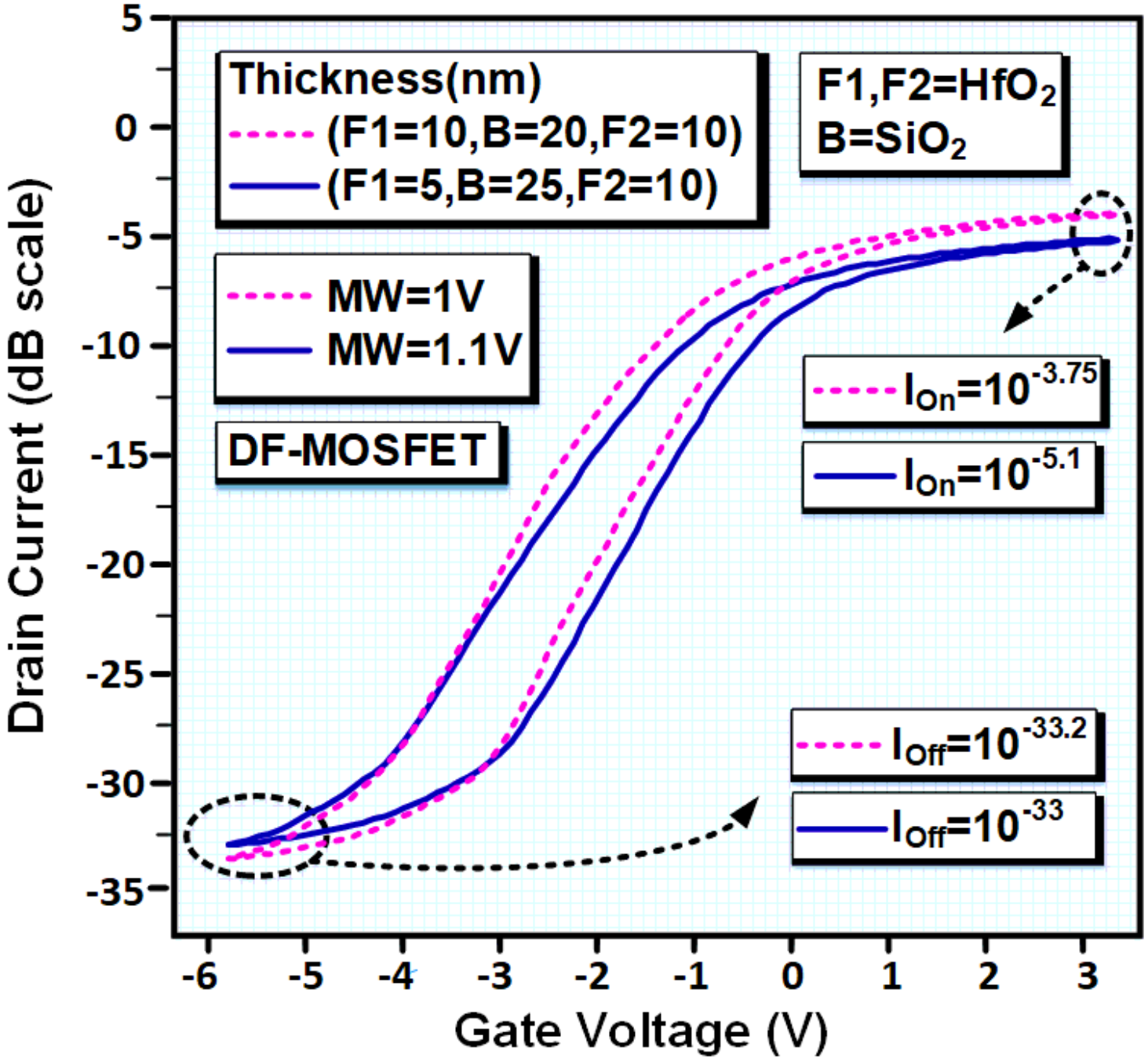

Figure 10

Effects of thickness changes on the DF-MOSFET structure.

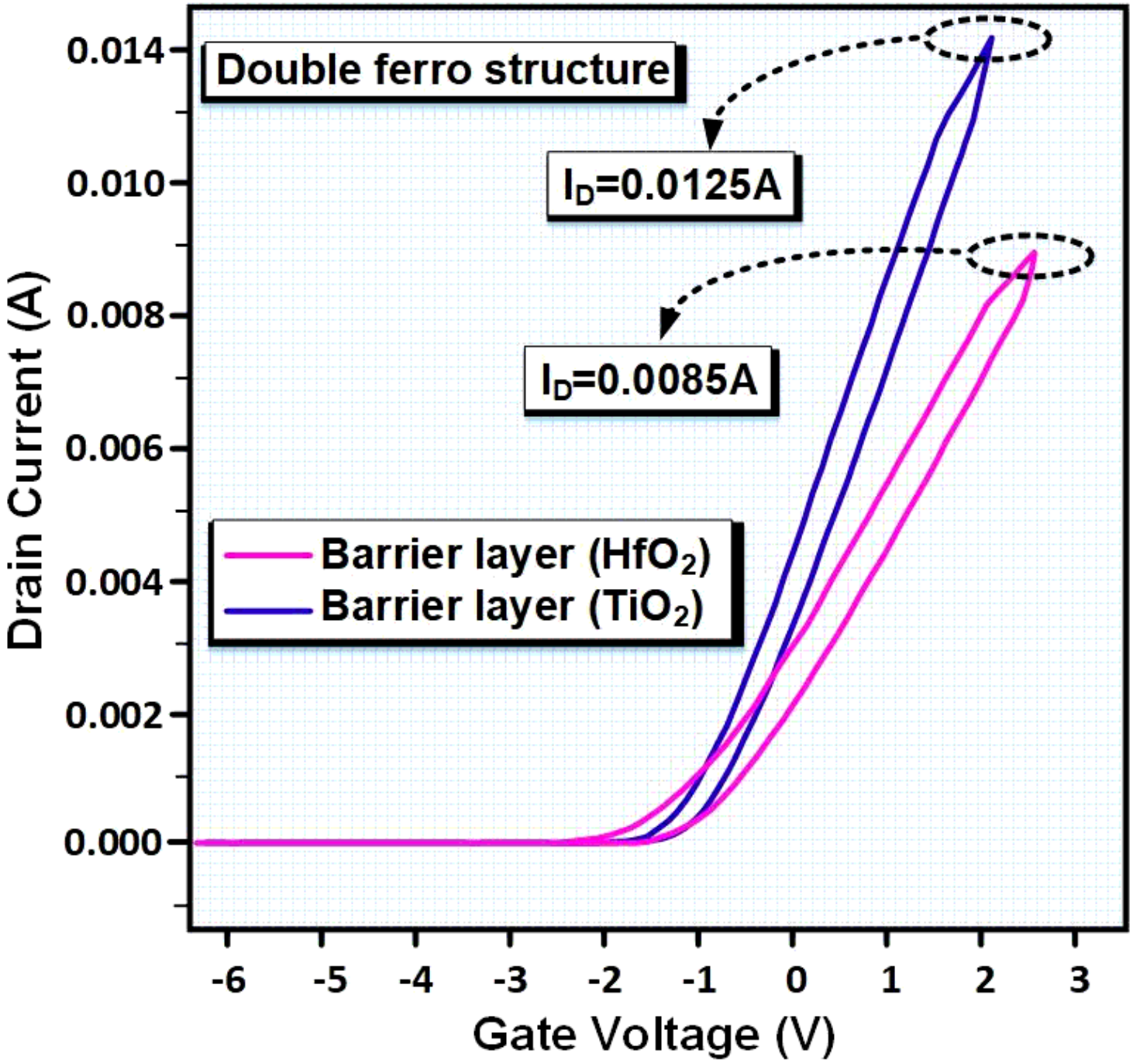

Figure 11

Effects of material changes (HfO_2, TiO_2) on the DF-MOSFET structure.

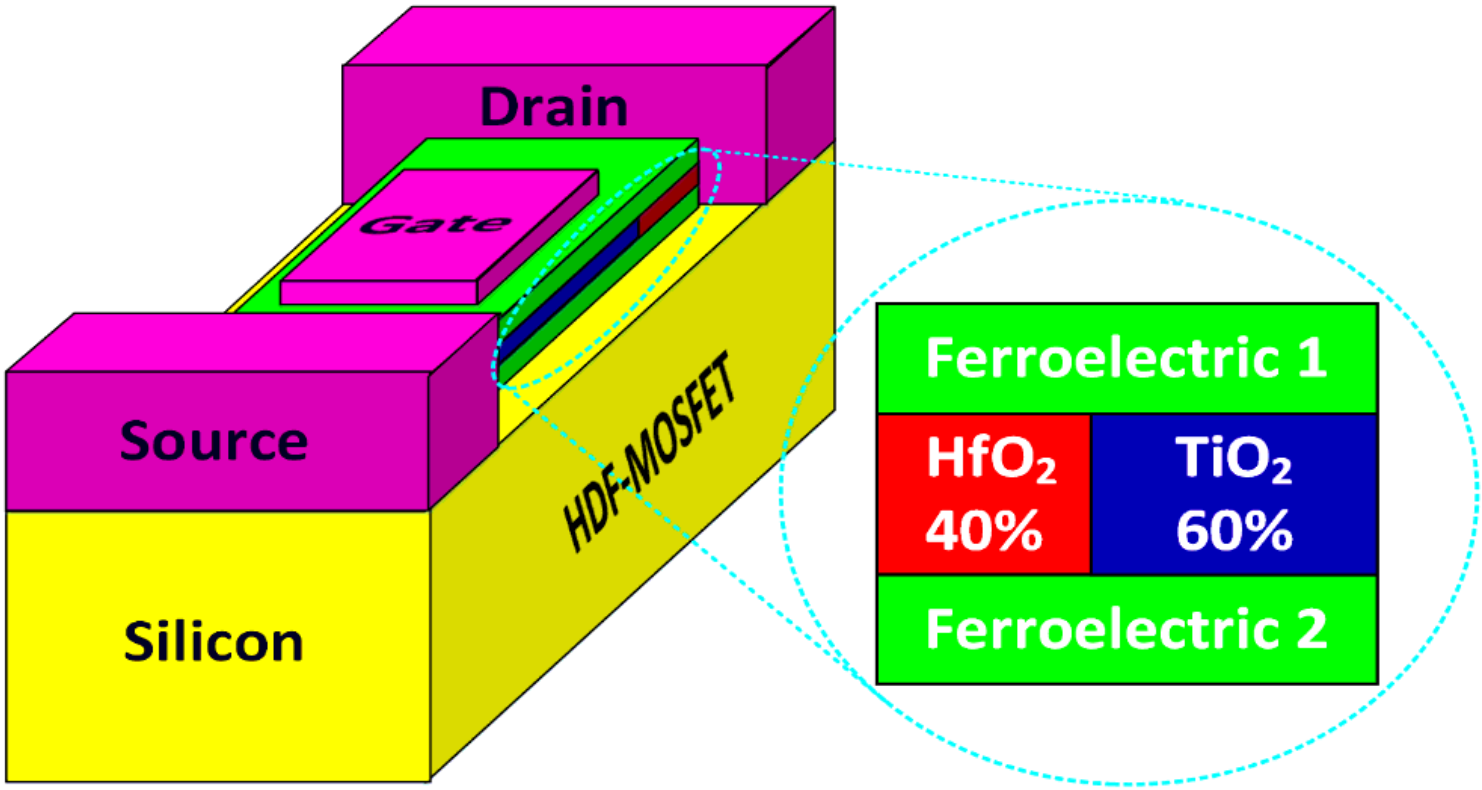

Figure 12

The final proposed heterojunction DF-MOSFET (HDF-MOSFET).

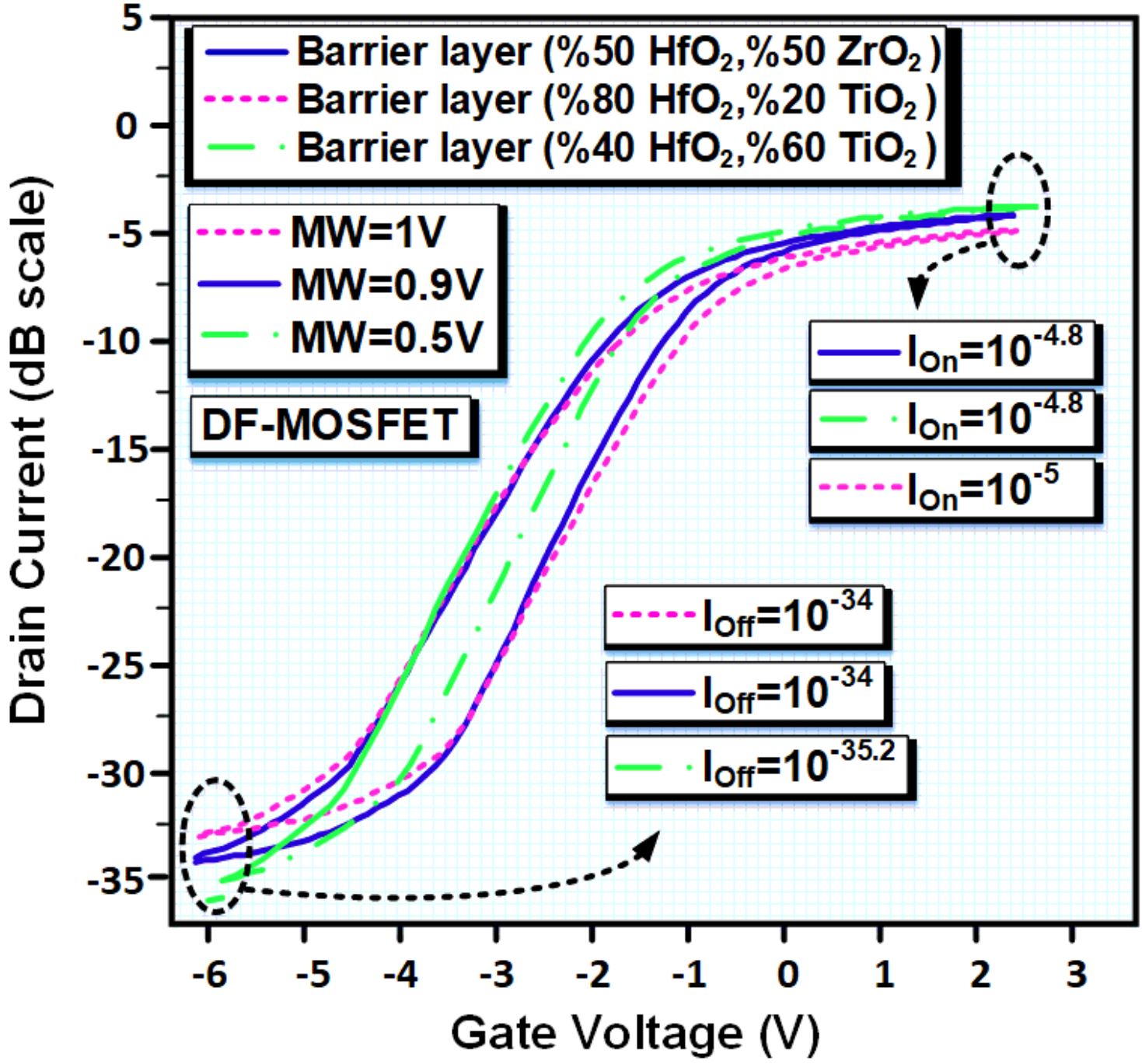

Figure 13

Effects of transverse changes of two-part barrier layer and different materials on important parameters of DF-MOSFET structure.