Enhanced Breakdown Voltage of Si-GaN Monolithic Heterogeneous Integrated Cascode FETs by the Device Structure Design

Jiaqi Zhang

Xidian University School of Microelectronics

Weihang Zhang

Xidian University School of Microelectronics

Jing Wan

School of Information Science and Engineering Fudan University

Guofang Yang

Xidian University School of Microelectronics

Ya'nan Cheng

Xidian University School of Microelectronics

Yachao Zhang

Xidian University School of Microelectronics

Dazheng Chen

Xidian University School of Microelectronics

Shenglei Zhao

Xidian University School of Microelectronics

Jincheng Zhang

Xidian University School of Microelectronics

Chunfu Zhang (✉ cfzhang@xidian.edu.cn)

Xidian University <https://orcid.org/0000-0001-9555-3377>

Yue Hao

Xidian University School of Microelectronics

Nano Express

Keywords: Monolithic heterogeneous integration, cascode FET, breakdown voltage, LDMOS, polarization charge

Posted Date: November 1st, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-1017098/v1>

License: © ⓘ This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

Version of Record: A version of this preprint was published at Solid-State Electronics on February 1st, 2022. See the published version at <https://doi.org/10.1016/j.sse.2022.108251>.

Enhanced breakdown voltage of Si-GaN Monolithic Heterogeneous Integrated Cascode FETs by the device structure design

Jiaqi Zhang¹, Weihang Zhang¹, *Member, IEEE*, Jing Wan², Guofang Yang¹, Ya'nan Cheng¹, Yachao Zhang¹, Dazheng Chen¹, Shenglei Zhao¹, Jincheng Zhang¹, *Member, IEEE*, Chunfu Zhang^{1*}, and Yue Hao¹, *Senior Member, IEEE*

Abstract—In this work, the factors affecting the breakdown voltage of Si-GaN monolithic heterogeneous integrated Cascode FET fabricated by transfer printing were investigated. These two factors are the avalanche breakdown resistance of the Si device and the thickness of SiN electrical isolation layer. Two kinds of device structures, Si MOSFET and Si laterally-diffused MOSFET (LDMOSFET), were designed to study the effect of the avalanche breakdown resistance of the Si devices on the breakdown characteristics of Cascode FET. The effect of the thickness of SiN electrical isolation layer was analyzed. Finally, the breakdown voltage of monolithic integrated Cascode FET reached 770 V.

Index Terms—Monolithic heterogeneous integration; cascode FET; breakdown voltage; LDMOS; polarization charge.

I. INTRODUCTION

Monolithic heterogeneous integrated devices and circuits are getting more and more attention in this era of Moore's Law coming to an end. Monolithic heterogeneous integrated devices and circuits, compared with the traditional packaging form of integrated devices and circuits, have a higher degree of integration, higher operating frequency and more diverse functions. These advantages are needed for devices and chips in the 5G era, and are needed to continue Moore's Law.

In recent years, there have been many reports on the fabrication of various monolithic heterogeneous integrated devices and circuits by different heterogeneous integration methods, heteroepitaxy [1]-[3], wafer bonding [4],[5] and transfer printing [6],[5]-[8], respectively. At present, monolithic heterogeneous integrated devices reported include Cascode FETs, Cascode diodes, flexible UV PDs and UV LEDs, etc [1],[2],[5],[6],[8]-[12]. And monolithic heterogeneous integrated circuits reported include GaN-Si hybrid amplifier, current mirror integrated circuits and half-bridge circuits [13].

Manuscript received xxxx, 2021 and revised xxxx, 2021; accepted xxxx, 2021. Date of publication xxxx 2021; date of current version xxxx, 2020.

¹ Jiaqi Zhang, Weihang Zhang, Guofang Yang, Ya'nan Cheng, Yachao Zhang, Dazheng Chen, Shenglei Zhao, Jincheng Zhang, Chunfu Zhang and Yue Hao are with State Key Discipline Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China (C. Zhang: cfzhang@xidian.edu.cn).

² Jing Wan is with State Key Laboratory of ASIC and System, School of Information Science and Engineering, Fudan University, Shanghai 200433, China

Among the three heterogeneous integration methods mentioned above, the transfer printing method isn't limited to the sizes of material lattices, the crystal orientations of materials and the types of the integrated materials. And, the requirements on wafer flatness are not harsh, the operation is simple, the cost is low, so the transfer printing method has more universality and application prospect [14]-[16].

In our previous work, wafer-scale Si-GaN monolithic integrated Cascode FETs were realized by transfer printing and self-aligned etching technology preliminarily [6]. However, the breakdown characteristics of monolithic heterogeneous integrated Cascode FET realized by transfer printing method were very poor (~ 40 V) [6]. To solve this problem, two key factors affecting the breakdown characteristics of the monolithic heterogeneous integrated Cascode FET devices have been found in this work. Firstly, the silicon devices in Cascode FET devices must have a certain anti-avalanche ability to turn off the GaN HEMTs. Secondly, the SiN used for the electrical isolation of Si and GaN should be thick enough to isolate the effect of 2DEG on the silicon devices. The relevant devices were tested, and the results verified the above viewpoints. What's more, the effect of polarization charge in AlGaIn/GaN on silicon device is analyzed by physical model. Finally, the monolithic heterogeneous integrated Cascode FET with breakdown voltage of 770 V was realized. And, its switching characteristics at 100 Hz and 1 kHz were tested.

II. DEVICE FABRICATION

The fabrication process of Si-GaN monolithic heterogeneous integrated substrate is detailed in the previous work [6]. The Si-GaN monolithic integrated cascode FETs were fabricated on this Si-GaN heterogeneous integrated substrate prepared by the transfer printing method [6]. Drift regions and S/D regions of Si devices were defined by phosphorus ion implantation. Boron ion implantation defined P+ regions of Si devices, and the dopants were activated by rapid thermal processing (RTP) at 1000°C for 60 sec. Subsequently, SiN was etched away to form the Ohmic contact windows in source regions. And, Ti/Al/Ni/Au stack was deposited on it. By using RTP (875 °C, 30 sec), the Ohmic contact was formed. The gate and drain windows of GaN HEMTs were opened by Etching the SiN layer. Then, the gates and Schottky drains of GaN HEMTs were

formed by Ni/Au stack deposition. The gate dielectric of Si device is 30 nm Al_2O_3 grown by ALD and the gate electrode is Ti/Au stack. DHF (2%) opened the windows of S/D regions of Si devices. Ohmic alloy of the Si device was formed by Ti/Au (20/120 nm) deposition and RTA (400 °C, 60 sec). In the end, DHF (2%) opened the windows of G/S/D electrodes of GaN HEMTs. The metal interconnects were formed by Ni/Au stack deposition.

Fig. 1. (a) Schematic cross-sectional view of the Si MOSFET on the SiN/AlGaIn/GaN substrate by transfer printing heterogeneous integration, (b) schematic cross-sectional view of the Si LDMOSFET on the SiN/AlGaIn/GaN substrate by transfer printing heterogeneous integration.

In order to study the effect of anti-avalanche ability of silicon devices on the breakdown characteristics of monolithic heterogeneous integrated Cascode FET devices, two kinds of Si devices with different structures on the SiN/AlGaIn/GaN substrate were designed, as shown in Fig. 1. Fig. 1 (a) shows the normal Si MOSFET device transferred on the SiN/AlGaIn/GaN substrate. Fig. 1 (b) shows the Si LDMOS device transferred on the SiN/AlGaIn/GaN substrate. In addition, each of the different silicon devices has a different SiN layer thickness of 20 nm and 200 nm, respectively, was deposited followed by RTA at 400 °C for 30 sec to form ohmic alloy of the Si MOSFET. Finally, the vias of G/S/D electrodes of GaN HEMT were opened by BOE. Ni/Au stack deposition formed the metal interconnects.

III. RESULTS AND DISCUSSION

The Si devices were placed on top of an active 2DEG from AlGaIn/GaN structure in our previous work [6]. This kind of monolithic heterogeneous integration is likely to cause problems with backgate effect and other coupling effects, which may adversely affect the performances of heterogeneous integrated Cascode FETs. Fig. 2 shows the cross-section diagram of the Si/SiN/AlGaIn/GaN structure realized by transfer printing and self-aligned etching. The polarization charge generated by AlGaIn/GaN structure is represented by white balls in the figure. Under normal circumstances, the polarization charges will induce a high concentration of electrons at the interface of AlGaIn/GaN heterojunction, 2DEG, namely. At this time, the polarization charges and 2DEG reach the charge balance, and the AlGaIn/GaN heterostructure is electrically neutral. The Si/SiN/AlGaIn/GaN structure can be simplified to the equivalent graph, as shown in Fig. 2 (b). This equivalent structure consists of two capacitors (C_{SiN} , $C_{\text{AlGaIn/GaN}}$) in series and the polarization charge (Q_{pol}). Due to the existence of Si (100) layer, the polarization charges will also induce electron channel at the bottom interface of Si, and the charges

balance relationship at this time is as follows:

$$\begin{cases} Q_{\text{Si}} = U \cdot C_{\text{SiN}} & (1) \\ Q_{\text{2DEG}} = U \cdot C_{\text{AlGaIn/GaN}} & (2) \\ Q_{\text{pol}} = Q_{\text{Si}} + Q_{\text{2DEG}} & (3) \end{cases}$$

In the above formula, Q_{Si} is the amount of electron charge induced by the polarization charge in the Si layer. $Q_{\text{AlGaIn/GaN}}$ is the charge amount of 2DEG in AlGaIn/GaN heterojunction. In order to weaken the effect of polarization charge on the Si layer, the electrons induced in the Si layer by polarization charge need to be reduced. It follows from the formula that it can be realized by reducing the C_{SiN} . Therefore, the thickness of the SiN layer was increased to 200 nm to reduce the effect of polarization charge on the silicon layer. And, a 20 nm SiN layer was used as a control.

Fig. 2. (a) The cross-section diagram of the Si/SiN/AlGaIn/GaN structure realized by transfer printing and self-aligned etching, (b) the equivalent graph of the Si/SiN/AlGaIn/GaN structure.

Fig. 3 shows the breakdown characteristics of Si MOSFET and Si LDMOSFET with different thicknesses of SiN layers. As can be seen from Fig. 3 (a), the breakdown voltage of Si LDMOSFET is 12 V, and the breakdown voltage of Si MOSFET is 6 V. And both of these Si devices on SiN/AlGaIn/GaN substrate with 20 nm SiN have large current leakage. Similarly, it can be seen from Fig. 3 (b) that the breakdown voltage of Si LDMOSFET is 13 V, and the breakdown voltage of Si MOSFET is 6.5 V. And the turn-off currents of these two kinds of Si devices are both in a lower magnitude (10^{-7} A). Therefore, through the above comparison, it can be concluded that the thinner SiN layer will have an adverse effect on the off-state current of the Si devices. This is because the C_{SiN} of the thinner SiN layer (20 nm) is larger. The Q_{Si} induced by polarization charge is more in Si layer. Therefore, the electron channel formed by Q_{Si} is less easily controlled by the gate of silicon device. The gate was applied a voltage of -3 V to shut down the top channel and the bottom channel. However, due to the weak control force of the gate on the bottom channel and the high electron concentration of the bottom channel, the gate can't control the bottom channel well. Therefore, as the V_{DS} is increasing, the gate voltage is at a disadvantage in the competition with the V_{DS} for the control of the bottom channel. It leads to the increase of current leakage. Moreover, Si LDMOSFET has higher breakdown voltage compared with Si MOSFET. The reason is that LDMOS has an N- drift region which enables the Si device to withstand a larger voltage.

Fig. 3. (a) The breakdown characteristics of Si MOSFET and Si LDMOSFET with 20 nm SiN layer, (b) the breakdown characteristics of Si MOSFET and Si LDMOSFET with 200 nm SiN layer.

Fig. 4 shows the transfer characteristics of the Si LDMOSFETs with different thicknesses of SiN layers (20 nm, 200 nm). The threshold voltages of Si LDMOSFETs with 20 nm SiN layer and 200 nm SiN layer were extracted as 0.3 V and 2.8 V, respectively. As can be seen from the figure, the off-state current of Si LDMOSFET with 20 nm SiN layer is an order of magnitude higher than that with 200 nm SiN layer. That is to say, the thinner the SiN layer, the more negative the threshold voltage of Si LDMOSFET drift, and the greater the off-state leakage current. The reason is that the thin SiN layer isn't thick enough to eliminate the influence of the polarization charge on the Si layer, so that the bottom interface of the Si layer is induced to generate a high concentration of electrons, forming a conductive channel. This bottom interface channel enables the Si device to have normally-on property, and it also makes the threshold voltage drift negatively. Compared with the Si device with 200 nm SiN layer, the Si device with 20 nm SiN layer has higher induced electron concentration in bottom interface channel. And, the bottom interface channel of Si device with 20 nm SiN layer is less likely to be clamped by the gate, so there will be higher off-state leakage current.

Fig. 4. The transfer characteristics of the Si LDMOSFETs with different thicknesses of SiN layers (20 nm, 200 nm).

Based on the above discussion and research, the SiN (200 nm)/AlGaIn/GaN substrate was selected as the substrate for the fabrication of monolithic heterogeneous integrated Cascode FET devices. In addition, Si LDMOS structure replaced the original Si MOS structure to form a part of Cascode FET devices. Fig. 5 (a) and (b) show the optical photographs of the Cascode FET devices containing a Si MOSFET ($V_{BR} = 6.5$ V) and a Si LDMOSFET ($V_{BR} = 13$ V), respectively. Fig. 5 (c) shows the breakdown characteristics of Cascode FET containing Si MOSFET. The breakdown voltage of the Cascode FET is only 50 V at the breakdown standard of 10^{-2} mA/mm. However, the breakdown voltage of the Cascode FET device containing Si LDMOSFET can reach 770 V, as shown in Fig. 5 (d). It indicates that silicon devices in Cascode FET devices need to have a certain ability to resist avalanche, which make Cascode FET have normal breakdown characteristics.

Fig. 5. (a) The optical photographs of the Cascode FET devices containing a Si MOSFET ($V_{BR} = 6.5$ V), (b) the optical photographs of the Cascode FET devices containing a Si LDMOSFET ($V_{BR} = 13$ V), (c) the breakdown characteristics of Cascode FET containing Si MOSFET, (d) the breakdown characteristics of Cascode FET containing Si LDMOSFET.

Finally, the pulse switch response waveform of the Cascode FET device was tested in Fig. 6. The gate signal was set ($V_{high} = 7$ V, $V_{low} = 0$ V). The dynamic response of the I_{DS} of the Cascode FET at 100 Hz was good, as shown in Fig. 6 (a). Although the I_{DS} is somewhat sluggish at 1 kHz, it can still reach saturation and follow the change of the V_{GS} , as shown in Fig. 6 (b). In future work, we will continue to improve and optimize the dynamic characteristics of the Cascode FET by reducing the interface states and defects of Si devices.

Fig. 6. (a) The pulse switch response waveform of the Cascode FET device at the frequency of 100 Hz, (b) the pulse switch response waveform of the Cascode FET device at the frequency of 1 kHz.

IV. CONCLUSION

In conclusion, monolithic heterogeneous integrated Cascode FET devices fully demonstrate their advantages, but there is still a problem of poor breakdown characteristics. In this work, the influence mechanism of 2DEG on silicon layer was analyzed and explained in depth. Then, the above mechanism was verified by experiments. Finally, the breakdown voltage of Cascode FET reached 770 V by changing the structure of the silicon device and thickening the SiN layer. And, the dynamic characteristics of the Cascode FET device were tested and the optimization scheme was proposed.

ACKNOWLEDGMENT

This work is supported by National Key R&D Program of China (2018YFB1802001), Natural Science Basic Research Program of Shaanxi (Program No. 2021JC-24) and in part by the Fundamental Research Funds for the National 111 Center (Grant No. B12026).

REFERENCES

- [1] J. Ren, C. Liu, C. W. Tang, K. M. Lau, and J. K. Sin, "A Novel Si-GaN Monolithic Integration Technology for a High-Voltage Cascoded Diode," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 501–504, 2017. DOI: 10.1109/LED.2017.2665698.
- [2] J. Ren, C. W. Tang, H. Feng, H. Jiang, W. Yang, X. Zhou, and J. K. Sin, "A novel 700V monolithically integrated Si-GaN cascaded field effect transistor," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 394–396, 2018. DOI: 10.7567/apex.7.041003.

- [3] W. E. Hoke, R. V. Chelakara, J. P. Bettencourt, T. E. Kazior, J. R. LaRoche, T. D. Kennedy, J. J. Mosca, A. Torabi, A. J. Kerr, H.-S. Lee, and T. Palacios, "Monolithic integration of silicon CMOS and GaN transistors in a current mirror circuit," *Journal of Vacuum Science & Technology B.*, vol. 101, no. May, 2014. DOI: 10.1116/1.3665220.
- [4] K. H. Lee, S. Bao, L. Zhang, D. Kohen, E. Fitzgerald, and C. S. Tan, "Integration of GaAs, GaN, and Si-CMOS on a common 200mm Si substrate through multilayer transfer process," *Appl. Phys. Express*, vol. 9, no. 8, pp. 1–4, 2016. DOI: 10.7567/APEX.9.086501.
- [5] C. G. Nunez, F. Liu, W. T. Navaraj, A. Christou, D. Shakthivel, and R. Dahiya, "Heterogeneous integration of contact-printed semiconductor nanowires for high-performance devices on large areas," *Microsystems & Nanoengineering*, vol. 4, no. 22, 2018. DOI: 10.1038/s41378-018-0021-6.
- [6] J. Zhang, W. Zhang, Y. Wu, Y. Zhang, Y. Peng, Z. Feng, D. Chen, S. Zhao, J. Zhang, C. Zhang and Y. Hao, "Wafer-Scale Si–GaN Monolithic Integrated E-Mode Cascode FET Realized by Transfer Printing and Self-Aligned Etching Technology," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 67, no. 8, pp. 3304–3308, 2020. DOI: 10.1109/TED.2020.3001083.
- [7] J. Zhang, Y. Zhang, D. Chen, W. Zhu, H. Xi, J. Zhang, C. Zhang, and Y. Hao, "Bendable Single Crystal Silicon Nanomembrane Thin Film Transistors with Improved Low-Temperature Processed Metal/n-Si Ohmic Contact by Inserting TiO₂ Interlayer", *Nanomaterials*, vol. 8, no. 12, 2018. DOI: 10.3390/nano8121060.
- [8] D. Liu, S. J. Cho, J. Park, J. Gong, J. Seo, R. Dalmau, D. Zhao, K. Kim, M. Kim, A. R. K. Kalapala, J. D. Albrecht, W. Zhou, B. Moody, and Z. Ma, "226 nm AlGaIn/AlN UV LEDs using p-type Si for hole injection and UV reflection," *Applied physics letters.*, vol. 113, no. 1, Jul. 2018, Art. no. 011111, doi: 10.1063/1.5038044
- [9] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuratio," *IEEE Transactions on power electronics*, vol. 29, no. 5, pp. 2208–2219, May. 2014. doi: 10.1109/TPEL.2013.2267804.
- [10] K.-T. Lee, C. Bayram, D. Piedra, E. Sprogis, H. Deligianni, B. Krishnan, G. Papasouliotis, A. Paranjpe, E. Aklimi, K. Shepard, T. Palacios, and D. Sadana, "GaN devices on a 200 mm Si platform targeting heterogeneous integration," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1094–1096, Aug. 2017, doi: 10.1109/LED.2017.2720688.
- [11] H.-S. Lee, K. Ryu, M. Sun, and T. Palacios, "Wafer-level heterogeneous integration of GaN HEMTs and Si (100) MOSFETs," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 200–202, Feb. 2012, doi: 10.1109/LED.2011.2174136.
- [12] W. -T. Navaraj, S. Gupta, L. Lorenzelli, and R. Dahiya, "Wafer Scale Transfer of Ultrathin Silicon Chips on Flexible Substrates for High Performance Bendable Systems," *Advanced Electronic Materials*, vol. 4, no. 4, 2018. DOI: 10.1002/aelm.201700277.
- [13] K. H. Lee, S. Bao, L. Zhang, D. Kohen, E. Fitzgerald, and C. S. Tan, "Integration of GaAs, GaN, and Si-CMOS on a common 200mm Si substrate through multilayer transfer process," *Appl. Phys. Express*, vol. 9, no. 8, pp. 1–4, 2016. DOI: 10.7567/APEX.9.086501.
- [14] M. -A. Meitl, Z. Zhu, V. Kumar, K. -J. Lee, X. Feng, Y. -Y. Huang, I. Adesida, R. -G. Nuzzo, and J. -A. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," *Nature Materials*, vol. 5, pp. 33–38, 2006. DOI: :10.1038/nmat1532.
- [15] J. Zhang Yichang Wu, Zhe Li, Yachao Zhang, Yue peng, Dazheng chen, Weidong Zhu, Shengrui Xu chunfu Zhang & Yue Hao., "High-performance Acetone Soluble Tape Transfer Printing Method for Heterogeneous Integration," *Scientific Reports*, pp. 1–7, 2019. DOI: 10.1038/s41598-019-52235-0.
- [16] L. Sun, G. Qin, J. H. Seo, G. K. Celler, W. Zhou, and Z. Ma, "12-GHz thin-film transistors on transferrable silicon nanomembranes for high-performance flexible electronics," *Small*, vol. 6, no. 22, pp. 2553–2557, 2010. DOI: 10.1002/small.201000522.