High-performance hysteresis-free perovskite transistors through anion engineering

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Article

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Abstract

Despite the impressive development of metal halide perovskites in diverse optoelectronics, progress on high-performance transistors employing state-of-the-art perovskite channels has been limited owing to ion migration and large organic spacer isolation. Herein, we report high-performance and hysteresis-free p-channel perovskite thin-film transistors (TFTs) based on methylammonium tin iodide (MASnI_3) and rationalise the effects of halide (I/Br/Cl) anion engineering on crystallinity enhancement and vacancy suppression, realising a high hole mobility of $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, current on/off ratio exceeding 10^7 , and threshold voltage of 0 V with high operational stability and reproducibility. We reveal ion migration has a negligible contribution to the hysteresis of Sn-based perovskite TFTs; instead, minority carrier trapping is the primary cause. Finally, we integrate the perovskite TFTs with commercialised n-channel indium gallium zinc oxide TFTs on a single chip to construct high-gain complementary inverters, facilitating the development of halide perovskite semiconductors for printable electronics and circuits.

Introduction

As an emerging class of semiconductors with remarkable properties, metal halide perovskites have enabled unprecedented performance improvements in diverse optoelectronic devices, such as solar cells^{1–3}, light-emitting diodes (LEDs)^{4–7}, and photo/X-ray detectors^{8,9}. In comparison, their prospects in high-performance transistors, which are fundamental building blocks for modern electronics, remain to be seen^{10,11}. The dominant lead halide perovskites in state-of-the-art optoelectronic devices, e.g. methylammonium lead iodide (MAPbI_3), exhibit small carrier effective masses comparable with silicon; however, their room-temperature charge-carrier mobilities are strongly limited by Fröhlich interactions due to the polar nature of Pb–halide bonds^{12,13}. Furthermore, the severe ion migration induced by halide vacancies results in poor field-effect modulation and large current–voltage hysteresis^{14–18}. After considerable efforts in ionic defect cleaning/healing, a MAPbI_3 transistor with a room-temperature field-effect mobility (μ_{FE}) of $\sim 4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was recently demonstrated¹⁹. In comparison, tin halide perovskites are predicated to possess higher room-temperature mobilities than their Pb-halide analogues owing to the reduced Fröhlich effect¹². However, current Sn-perovskite transistors rely on two-dimensional (2D) layered perovskites, in which carrier transport is notably hindered by the bulky/insulating organic spacers, posing a critical barrier for further performance enhancement^{20–25}.

Here, we demonstrate high-performance and hysteresis-free p-channel perovskite thin-film transistors (TFTs) with a three-dimensional (3D) methylammonium tin iodide (MASnI_3)-based channel layer via rational halide anion (I/Br/Cl) engineering. The co-substitution of small amounts of bromide and chloride for iodide enhances the crystallinity and vacancy passivation, enabling TFTs with excellent electrical characteristics, such as a high μ_{FE} of $\sim 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of over 10^7 , and a threshold voltage (V_{TH}) of 0 V. Unlike the dominant role of ion migration in the hysteresis of Pb-halide perovskite TFTs, we declare that the device hysteresis in Sn-based perovskite TFTs originates from

minority carrier trapping at iodide vacancy sites. These deep traps are substantially reduced by proper Br and Cl co-substitution, which eliminates the hysteresis and provides high operational stability and reproducibility. By integrating the perovskite TFTs with n-channel indium gallium zinc oxide (IGZO) TFTs, we realised complementary inverters with high gain of 140 and noise margin of over 70%, suggesting great processability and compatibility for large-area electronic circuits.

Results And Discussion

Perovskite films were spin-coated on hafnium (IV) oxide (HfO_2) layers fabricated by atomic layer deposition (ALD) from precursors consisting of methylammonium iodide (MAI) and tin(II) halide (SnX_2 , $\text{X}=\text{Cl}, \text{Br}, \text{I}$), and then thermally annealed (see more details in Methods). Subsequently, gold source/drain electrodes were deposited, constructing the bottom-gate, top-contact TFTs (Fig. 1a). The TFTs obtained without halide engineering, denoted 'I-pristine', exhibited typical p-channel transfer characteristics under continuous mode at room temperature. The representative I-pristine device exhibited a low gate leakage current of $\sim 10^{-10}$ A, large $I_{\text{on}}/I_{\text{off}}$ ratio exceeding 10^6 , and maximum μ_{FE} of $1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Fig. 1b). This is the first demonstration of p-channel TFTs based on 3D MASnI_3 perovskite films, demonstrating electrical parameters comparable to those of previously reported perovskite TFTs (Supplementary Table 1).

We achieved TFTs with markedly improved performance by carefully engineering the halide compositions of the precursors for perovskite film deposition (Fig. 1b and Supplementary Fig. 1), inspired by the fact that recent breakthroughs in perovskite photovoltaics have been made mostly based on multiple compositions^{3, 26, 27}. Specifically, partially substitution of the iodide source with bromide salt (2 mol%, the devices are denoted 'I/Br') resulted in an over three-fold improvement in the μ_{FE} of the TFTs ($4.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). With the channel films deposited from a precursor with 6 mol% chloride substitution, we obtained devices (denoted as 'I/Cl') exhibiting an even higher μ_{FE} ($9.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). Surprisingly, a rational combination of the two halide engineering strategies, i.e. employing channels deposited from perovskite precursors with simultaneous Br and Cl substitution (2 mol% Br and 6 mol% Cl), led to greatly enhanced TFT (denoted as 'I/Br/Cl') performance. As shown in Fig. 1b, the optimised I/Br/Cl perovskite TFTs exhibited a μ_{FE} of $19.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an $I_{\text{on}}/I_{\text{off}}$ of 3×10^7 , which is superior to reported Pb- and 2D Sn-based perovskite TFTs (Supplementary Table 1). Textbook-like output curves (I_{DS} versus V_{DS}) with clear linear and saturation currents were observed for all the devices (Supplementary Fig. 2), indicating Ohmic contact between the channel films and electrodes and validating the reliability of mobility extraction²⁸. Furthermore, the I/Br/Cl device operated in an ideal enhancement mode with a V_{TH} of 0 V (Supplementary Fig. 3), suggesting that no applied bias voltage is needed to turn off the transistor, which is highly desirable for simplifying circuit design and minimising power consumption in practical applications²⁹.

In addition to higher mobilities than those of I-pristine, I/Br, and I/Cl devices, the TFTs based on I/Br/Cl perovskite channels also exhibited significantly reduced, even negligible, current–voltage hysteresis. To

quantitatively analyse the hysteresis for the I-pristine, I/Br, I/Cl, and I/Br/Cl TFTs, we calculated the difference in V_{GS} (ΔV_{GS}) at $|I_{DS}|=10^{-7}$ A, halfway between the on and off states³⁰, and presented the data in Fig. 1c. Notably, the I/Br/Cl devices exhibited an average ΔV_{GS} of 0.1 V, which is less than 1/10 of that of the other three types of TFTs, in which ion migration and/or carrier trapping probably occurred (discussed later). The negligible hysteresis for the I/Br/Cl devices is comparable with commercialised amorphous metal oxide TFTs³¹. Similar to previous perovskite solar cells³², the hysteresis in the dual-sweep transfer curves of the TFTs also causes variations of the extracted performance parameters. We observed notable differences in the maximum mobility values extracted from the reverse (on-to-off, -12 to 7 V) and forward (off-to-on, 7 to -12 V) scans of the I-pristine, I/Br, and I/Cl TFTs (Supplementary Fig. 4), and presented the μ_{FE} statistics in Fig. 1d. The I/Cl TFTs demonstrated the largest mobility variations (>70%) because of their largest hysteresis, while the variations for the I-pristine and I/Br devices were slightly lower (50%). Notably, the I/Br/Cl devices exhibited the smallest mobility variations (12%) owing to their negligible hysteresis. Because a strong mobility–hysteresis correlation exists but has been usually neglected in previous research on perovskite TFTs¹⁷, we recommend more information on the measurement methods, device hysteresis, and mobilities extracted from both the forward and reverse scans of devices be provided. The hysteresis-free character is highly desired for a wide range of electronic applications, such as logic circuits and backplanes in OLED displays³³.

To comprehensively understand the benefits of halide engineering for perovskite TFTs, we performed a series of film characterisations. The scanning electron microscope (SEM) images in Fig. 2a reveal a few pinholes in the I-pristine perovskite film, and slight Br substitution suppressed the pinholes. The incorporated Br anions could compete with I anions and coordinate more strongly with the metal ions (Sn^{2+}), modulating the nucleation and crystallisation kinetics of the perovskite films^{34,35}. In comparison, both the I/Cl and I/Br/Cl films exhibited a considerably smoother surface morphology, suggesting the incorporation of Cl in the precursor significantly promoted perovskite formation, similar to observations about Cl in lead halide perovskites for solar cells^{34,36,37}. The results are consistent with X-ray diffraction (XRD) analyses, where the I/Cl and I/Br/Cl samples exhibited substantially increased intensities of the main diffraction peaks compared with those of the I-pristine and I/Br samples, suggesting notably enhanced crystallinity (Fig. 2b).

Interestingly, both the I/Br and I/Br/Cl films exhibited identifiable XRD peak shifts to higher angles compared with that of the I-pristine film. The peak shifts indicate a reduced d -spacing due to the incorporation of smaller Br and/or Cl ions into the I-based perovskite lattices. However, the I/Cl sample showed negligible peak shifts (Supplementary Fig. 5), which suggests that the Cl anions in the I/Cl perovskite film did not enter the perovskite lattice but only functioned to improve the film morphology and crystallinity³⁸. The X-ray photoelectron spectroscopy (XPS) Cl 2*p* core level spectra further confirmed that Cl was undetectable in the I/Cl films but was successfully incorporated into the triple-halide I/Br/Cl films (Fig. 2c). These results are unsurprising considering the large discrepancy in ionic size between I and Cl anions and the potential volatilisation of Cl additives during film annealing³⁹. However, in the I/Br/Cl

perovskite film, the Br-substituted I-based lattice was capable of hosting Cl anions owing to the bridging effect of Br^{40, 41}, enabling the formation of the triple-halide MASn(I/Br/Cl)₃ perovskite.

We then conducted Hall-effect measurements to investigate the carrier concentrations and Hall mobilities of the perovskite films, which are important for understanding the performance of the resulting TFTs. As shown in Fig. 2d, the I-pristine films exhibited an average hole concentration of $2.8 \times 10^{17} \text{ cm}^{-3}$, which gradually decreased to 6.9×10^{16} , 4.5×10^{16} , and $2.2 \times 10^{15} \text{ cm}^{-3}$ for the I/Br, I/Cl, and I/Br/Cl films, respectively. This trend resulted from decreasing hole sources (tin vacancies). Generally, in 3D Sn-based perovskites, Sn²⁺ can easily oxidise into Sn⁴⁺ even under trace oxygen, and intrinsic tin vacancies (V_{Sn}) have a low formation energy, which both cause notoriously high hole concentrations. As revealed by the Sn 3d_{5/2} XPS spectra in Fig. 2e, the I-pristine sample had a substantial Sn⁴⁺ signal at a high binding energy (487.5 eV), which is ~42% of the Sn 3d_{5/2} peak area. Notably, the peak area of the Sn⁴⁺ signal gradually decreased in the I/Br (29%), I/Cl (29%), and I/Br/Cl (20%) samples, indicating suppressed Sn²⁺ oxidation. Furthermore, previous studies have suggested that the incorporation of anions with electronegativity stronger than that of I⁻ raises the V_{Sn} formation energy during perovskite crystallisation, further reducing the hole concentration^{24, 42}. Additionally, for both the I-pristine and I/Br samples, a small shoulder peak appeared at a low binding energy (~485.4 eV), which is ascribed to under-coordinated Sn with an oxidation state of $\delta < 2^+$ (Sn ^{$\delta < 2^+$})⁴³. However, this shoulder peak was undetectable in both the I/Cl and I/Br/Cl samples, indicating well-coordinated Sn sublattices and reduced structural imperfections. The results are in good agreement with the improved quality of the perovskite films deposited from Cl-containing precursors, as demonstrated above, which also rationalises the slightly lower hole concentration of the I/Cl film compared with that of the I/Br film despite their similar degree of Sn²⁺ oxidation.

The Hall mobilities (μ_{Hall}) of the perovskite films showed a consistent trend with the μ_{FE} extracted from the corresponding TFTs, with the average μ_{Hall} increasing from $25 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (I-pristine) to 57 (I/Br) and $92 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (I/Cl), respectively. The μ_{Hall} for I/Br/Cl films was up to $301 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. According to the simple Drude model, the hole mobility of a p-type semiconductor is determined by the hole effective mass (m_h^*) and the average scattering time (τ): $\mu = q\tau / m_h^*$, where q is the elementary charge¹². Considering the small halide substitution in the perovskite lattice, negligible changes to m_h^* were expected. Therefore, μ_{Hall} should be mainly determined by the scattering time interval during carrier transport, which is dominated by scattering centres, e.g. ionised (negatively or positively charged) defects and crystal disorders, in the perovskite films. As revealed by the characterisations above, halide engineering effectively enhanced the crystallinity and reduced ionised defects, particularly in the I/Br/Cl film, significantly suppressing charge carrier scattering and providing a rationale for the enhanced μ_{Hall} of the halide-engineered perovskite films.

In addition to the improved perovskite film quality, the considerably improved performance of the I/Br/Cl devices is related to the properties of the dielectric–perovskite interfaces. Generally, the density of states

(N_s) at the interface, which negatively affects the device performance of TFTs, can be estimated from the

average subthreshold swing (SS, Supplementary Fig. 6): $SS = \frac{\kappa T \ln 10}{e} \left[1 + \frac{e^2}{C_i} N_s^{max} \right]$, where κ is the

Boltzmann constant, e is the electron charge, and C_i is the areal capacitance of the dielectric layer⁴⁴.

Accordingly, N_s^{max} of the I-pristine TFTs was calculated to be $1.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, which was notably reduced to $\sim 3.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ in the I/Br/Cl TFTs. This suggests that Br and Cl co-substitution greatly enhanced not only the film quality but also the dielectric-perovskite interfaces of the TFTs.

Having elucidated the benefits of rational halide engineering of MASnI_3 precursors on the TFT performance, we attempted to gain an in-depth understanding of the hysteresis behaviour of the devices. The commonly observed hysteresis of transistors utilising 3D lead-halide perovskite films is typically attributed to ion migration in the perovskite channel⁴⁵. However, ion-migration-induced hysteresis is strongly dependent on the sweep rate during device measurement. For example, transistors based on single crystalline MAPbX_3 channels exhibited gradually expanded hysteresis when the sweep rate increased from 0.05 to 0.25 V s^{-1} (ref⁴⁶). However, we observed negligible changes to the hysteresis in the transfer curves of both the I-pristine and I/Br/Cl devices when the sweep rate increased from 0.4 to 4 V s^{-1} (Fig. 3a), suggesting that ion migration did not contribute significantly to TFT hysteresis in the MASnI_3 -based perovskite films. This can be partially explained by the different defect properties of Pb- and Sn-based perovskites²⁷. In p-type MASnI_3 , iodine defects, e.g. iodine vacancies (V_I) and interstitials (I_i), are less dominant (if even present) than V_{Sn} ⁴⁷. Consequently, the migration of iodide ions, which have the lowest activation energy and move the most easily, is less significant in MASnI_3 than in Pb-based perovskites, greatly reducing the associated electric-field screening effects during TFT operation.

We then considered charge carrier trapping as the primary reason for the hysteresis in our perovskite TFTs, which exhibited a higher current in the transfer curves during the off-to-on sweep than that during the on-to-off sweep. The established models indicate deep electron and hole traps in the semiconductor channels⁴⁸ are possible causes for this type of hysteresis in TFTs. Theoretical calculations have predicted that in MASnI_3 , hole traps induced by I_i and V_{Sn} defects are shallow, with thermodynamic ionisation levels close to or inside the valance band maximum⁴⁷. Thus, they are expected to mainly affect the μ_{FE} and SS of the TFTs rather than induce hysteresis.⁴⁸ We postulated that V_I defects, which possess the lowest formation energy among possible deep electron traps in MASnI_3 , were the root cause of the hysteresis in the p-channel TFTs. As shown in the inset of Fig. 3a, when $V_{\text{GS}} \ll V_{\text{TH}}$, negative charge accumulated in the channel, and V_I -related long-lifetime electron traps were filled. The trapped electrons shifted the flat-band voltage; that is, the threshold voltage was reduced. When V_{GS} swept towards negative potentials, more holes were induced, leading to a higher drain current. In comparison, the on-to-off sweep started directly from hole accumulation at $V_{\text{GS}} = -12 \text{ V}$ without the influence of stored negative charge⁴⁸, demonstrating a lower drain current. Therefore, the on-to-off measurement of the perovskite

TFTs should more closely resemble the ideal field-effect transistor model, indicating the mobility extracted from the on-to-off transfer curve may be closer to the actual μ_{FE} .

With the hypothesis that deep electron traps dominate the hysteresis in our p-channel perovskite TFTs, we investigated the different V_I properties of the I-pristine and I/Br/Cl perovskite films to unveil the mechanism that eliminated hysteresis in the optimised I/Br/Cl devices. In the I $3d_{3/2}$ core level XPS spectra (Fig. 3b), the peak shifted by 0.5 eV towards higher binding energies for the I-pristine sample compared with that of the I/Br/Cl perovskite. This peak shift was previously ascribed to iodine loss from the perovskite lattice, indicating a higher probability of V_I formation in the I-pristine perovskite film. In addition, a noticeable shoulder peak appeared at ~ 631.7 eV in the I $3d_{3/2}$ core level spectra of the I-pristine film, corresponding to the I_3^- species. These species were assigned to iodide interstitials/ V_I^+ iodine Frenkel defects, which form preferentially under V_{Sn} -rich conditions⁴⁹. The almost invisible shoulder peak for the I/Br/Cl perovskite can be attributed to the reduced iodine loss from the perovskite lattice, along with the significantly reduced hole concentration (V_{Sn} defects) revealed by the Hall measurements. Density functional theory (DFT) calculations further confirmed the benefits of passivating V_I sites in the I/Br/Cl perovskite film. As shown in Fig. 3c, Br or Cl anions, if successfully incorporated into the $MASnI_3$ perovskite lattice, possess higher binding affinities towards V_I sites than that of I anions (slab models in Supplementary Fig. 7), in agreement with recent Pb perovskites with double anions³. Based on the $MASn(I/Br)_3$ perovskite, the calculated binding affinity of a third anion, Cl^- , to V_I was further enhanced (Figs. 3c and 3d), and hence the V_I sites in the I/Br/Cl perovskite were expected to be notably suppressed, rationalising the elimination of hysteresis in the resulting TFTs.

We then characterised the operational stability of our perovskite TFTs, which is another critical figure of merit for practical applications. We first monitored the on/off switching stability of the devices (Fig. 4a). The I-pristine device exhibited a noticeable current decay during the consecutive on/off switching test, while the currents of both the on and off states of the I/Br/Cl device remained consistent. We also examined the device stability under dynamic V_{GS} scans. The transfer characteristics of the I-pristine TFTs gradually shifted, while those of the I/Br/Cl TFTs overlapped completely over 100 cyclic sweeps (Supplementary Fig. 8), suggesting considerably enhanced reliability of the I/Br/Cl devices. To evaluate the stability of the TFTs more rigorously, we performed a bias stress test, during which -12 V was applied constantly, and the shift in V_{TH} was monitored. As shown in Fig. 4b, the V_{TH} of the I-pristine device shifted significantly by -2 V ($\sim 17\%$ of the operating voltage) after only 1000 s during the bias test (Supplementary Fig. 9), reflecting the serious carrier trapping in the devices⁵⁰. Encouragingly, the optimised I/Br/Cl TFT exhibited greatly improved stability with a small threshold voltage shift (ΔV_{TH}) of 0.52 V even after biasing for 12 h, approaching the stability of previously demonstrated stable transistors based on organic and amorphous silicon channels^{45, 51}.

With the reproducible and stable p-channel I/Br/Cl perovskite TFTs (Supplementary Fig. 10), we moved a step further to explore their compatibility with existing TFTs based on n-channel metal oxides for

monolithic complementary circuit integration. We fabricated complementary inverters by integrating perovskite TFTs with IGZO TFTs on a single chip. Figure 4c shows an optical image and diagram of the complementary inverter. The standard rail-to-rail voltage transfer characteristics of the inverter at different V_{DD} (Fig. 4d) show V_{OUT} being either 0 V or the supplied V_{DD} , suggesting an ideal logic '1' to '0' transfer. The inverter exhibited a high gain of over 100 at all measured V_{DD} and a peak gain of 140 at $V_{DD}=11$ V (Fig. 4e), which is significantly higher than that of the wire-connected complementary inverter or CMOS-like inverters involving perovskite TFTs in previous studies^{24, 52}. To the best of our knowledge, this is also the first demonstration of the monolithic integration of a complementary circuit involving perovskite TFTs. Additionally, the noise margin of the inverter was 3.93 V, reaching 72% of the ideal value ($V_{DD}/2$) (Supplementary Fig. 11), which is sufficient for most static logic applications⁵³.

In conclusion, we have achieved high-performance and hysteresis-free MASnI_3 -based perovskite TFTs through rational halide engineering. We revealed the benefits of Br and Cl co-substitution in the precursor: enhanced crystallinity and reduced vacancy defects of the perovskite films, which enabled exceptional performance of the resulting TFTs. Moreover, we found ion migration had a negligible contribution to the hysteresis in our p-channel perovskite TFTs based on MASnI_3 films. Alternatively, we correlated the hysteresis of our MASnI_3 TFT with deep electron traps induced by V_i defects, which are notably reduced by rational Br and Cl co-substitution in the precursor. By combining our operationally stable p-channel perovskite TFTs with n-channel IGZO TFTs, we demonstrated monolithically integrated high-gain complementary inverters, suggesting high compatibility and processability for electronic applications.

Declarations

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Author Contributions

H. H. Z. and Y. Y. N. conceived the study. H. H. Z. and A. L. performed the experiments. A. L., T. Z., Y. R., H. C., J. L., H. K., and H. K. assisted with the characterisations and analyses. K. S. and J. H. performed the DFT calculations. H. J., T. Z., and A. L. assisted with the circuit mask design. H. H. Z., A. L., S. B., and Y. Y. N. wrote the manuscript. Y. C. assisted with manuscript revision. A. L. and S. B. contributed to the experimental design and data analysis. Y. Y. N. supervised the project. All the authors contributed to the discussion. All authors approved the final version of the manuscript.

Competing Interests

The authors declare no competing financial interest.

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Figures

Figure 1

Electrical characteristics of MASnX₃ perovskite TFTs. (a) TFT structure used in this work. (b) Transfer characteristics of the TFTs with different perovskite channel layers. IG: gate leakage current. (c) Hysteresis statistics of different TFTs. The error bars were calculated from ten devices per type, and the mean values are labelled. (d) Histogram of the extracted mobilities from the transfer characteristics under different scan directions for ten devices per type. The inset shows the variation ratio of the mobility values extracted from reverse (μ_{Rev}) and forward (μ_{For}) scans, calculated by $(\mu_{\text{Rev}} - \mu_{\text{For}}) / \mu_{\text{Rev}} \times 100\%$.

Figure 2

Characterisation of MASnX3 films. (a) SEM images, (b) XRD patterns, (c) Cl 2p core level XPS spectra, and (d) Hall mobilities and hole concentrations of the different perovskite films. (e) Analyses of the Sn 3d5/2 core level XPS spectra with fitting results for Sn^{δ<2+}, Sn²⁺, and Sn⁴⁺.

Figure 3

Hysteresis and VI in the MASnX₃ perovskite TFTs. (a) Transfer characteristics of I-pristine and I/Br/Cl TFTs measured at different scan speeds. (b) I 3d_{3/2} core level spectra of the I-pristine and I/Br/Cl perovskites. (c) Calculated relative interaction strengths of halide anions with VI sites in MASnI₃ and MASn(I/Br)₃. (d) Illustration of the passivation effects of a VI defect by a Cl anion.

Figure 4

Operational stability of perovskite TFTs and performance of the integrated inverters. (a) On/off switching sweep of the I-pristine and I/Br/Cl TFTs. (b) V_{TH} variation under bias ($V_{GS}=V_{DS}=-12$ V). (c) Optical image and diagram of an integrated perovskite/IGZO inverter. (d) Voltage transfer characteristics and (e) gain ((dV_{OUT})/(dV_{IN})).

Supplementary Files

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