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Dhananjaya Tripathy (dhananjaya.tripathy@silicon.ac.in)
NIT Rourkela: National Institute of Technology Rourkela
Debiprasad Priyabrata Acharya
NIT Rourkela: National Institute of Technology Rourkela
Prakash Kumar Rout
Silicon Institute of Technology

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Influence of Variation in Oxide layer Thickness on Analog and RF performances of SOI FinFET

Dhananjaya Tripathy[1,2], Debiprasad Priyabrata Acharya[1], Prakash Kumar Rout[2]

1.National Institute of Technology, Rourkela, Odisha, India-769008

2.Silicon Institute of Technology, Bhubaneswar, Odisha, India-751024

Corresponding to (dhananjaya.tripathy@silicon.ac.in)

Abstract: In this paper, the influence of oxide (SiO_2) layer thickness on the different figure of merits of a FinFET is analysed by varying the oxide layer thickness which is present between the gate and the Fin. Here, the overall thickness of the FinFET is taken to be 30nm, and the oxide (SiO_2) layer thickness is changed from 0.8 nm to 3nm, and the analog, radio frequency parameters are determined for different structures. The performance parameters like drain current (I_D), transconductance generation factor (TGF), transconductance (g_m), output conductance (g_{ds}), parasitic capacitances like Cgs, Cgd, Cgg, cut-off frequency (f_T), gain bandwidth product (GBW) and maximum frequency of oscillation (f_{max}) are calculated to learn the influence of variation in the FinFET oxide (SiO_2) layer thickness. It is detected from the result and analysis that the drain current, output conductance, transconductance generation factor, transconductance and gain bandwidth product improve with decrement in oxide layer thickness. But as a tradeoff, the internal capacitances like Cgs, Cgd, Cgg, maximum frequency of oscillation and cut-off frequency degrade when there is a reduction in oxide (SiO_2) layer thickness.

Keywords: FinFET, oxide layer thickness, transconductance generation factor, maximum frequency.

SECTION-I

INTRODUCTION

The requirement of added complex and immensely compressed electronic circuits have created the interest amongst the researchers to downscale the regular silicon MOS field effect transistor, which results in the evolution of compact ICs but, as a consequence Short-Channel Effects (SCE) are developed in the device which degrades the device parameters in a huge manner [1-8]. Many researchers have tried to improve the performance parameters of the conventional MOSFETs through gate and source/drain end engineering [9-12]. So multiple gate-based devices are considered as a solution to continue the downscaling. These devices possess improved controllability over lower leakage currents, SCEs and better yield [13,14]. FinFET is one of the evolutionary techniques for application based less-power consuming circuits as it displays

commendable performance to nullify the short-channel problems due to the fact that multiple gates monitoring a single channel [15-18].

Fin type silicon on insulator-based field effect transistor is the newly evolved technology which is presently used in ICs. FinFETs encompass a triple-gate construction to suppress the major performance problems, such as the SCEs. The silicon on insulator (SOI) technique insulates an active area from the lower part of the substrates, which intern reduces the leakage current, parasitic capacitance, and the power dissipation of circuits. Hence, SOI based FinFETs are the center of attraction now-a-days**.** The detail study of the SOI based FinFETs are presented in [19-24].

To construct tri-gate FinFETs different approaches has been followed in recent years like SOI based FinFETs [25], bulk FinFET [26]. The inverted-T structure FinFET [27] is also designed which enhances the drain current in a huge manner as compared to the SOI based FinFET. A spacer based design of FinFET[28] is also developed to improve the FinFET parameters. The effect of channel doping and Fin width on the performance parameters is represented in [29,30]. The impact of Fin shape is also studied in [31]. But it is very important to study the effect of the variation in oxide layer thickness on the key parameters of the device. The oxide layer thickness variation is studied in [32], where the thickness is varied over a range of 3 nm to 10 nm. But, in general the thickness of the oxide layer should not exceed 3nm for a FinFET of channel length 30nm.

Here, the 3-dimensional construction of FinFET is analyzed by altering the oxide layer (SiO_2) thickness keeping the total dimension of the FinFET fixed. To realize the physical mechanism of the device, various performance parameters are evaluated based on the mathematical terminologies and finally simulated to get a comparative analysis.

In section II the device description and simulation model are explained. Section III comprises the result and discussion. Section IV summarizes the total work done in the paper.

SECTION II

Device Description and Simulation Model

The core of the FinFET i.e., the fin is placed vertically with making an angle of 90º to the FinFET body and is responsible for the flow of current. A gate material with higher work function covers the silicon fin from three sides to reduce the SCEs by increasing the control over the device [33].

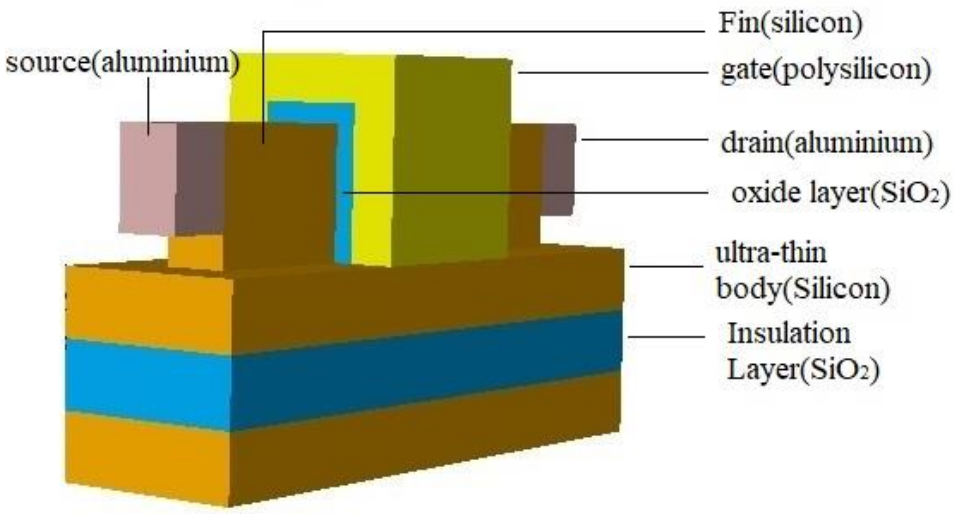

Fig.1. A 3-dimensional structure of the SOI-based FinFET,

The 3-dimensional structure of the SOI-based FinFET structure is represented in Fig.1. Here the oxide (SiO_2) layer placed between the fin and the gate is the central point of the discussion. As stated in the Table-1, the oxide layer thickness is varied from 0.8nm to 3nm keeping the total dimension of the FinFET as a constant i.e 30nm. The Fin height and width are taken to be 20nm and 10nm with a channel length of 30nm. The length of the device is kept as 110nm which is epresented in Table-1.

TABLE 1

Device Specifications of FinFET

Parameters	**Measurements**
Length of the channel (L_g)	30 nm
Height of the Fin (H_{Fin})	20 nm
Width of the Fin (W_{Fin})	10 nm
Fin Angle (θ)	90^o
Equivalent Oxide Thickness (EOT)	0.8 nm - 3 nm
Ultra-thin Body Thickness (UTB)	10 nm
Total Device Length	110 nm
Total Device Width	30 nm

The simulation process was carried out using the Silvaco ATLAS (2016) which is a standard TCAD simulation tool. To achieve better accuracy, the 3D quantum transport equations and the drift-diffusion equations are included. The Bohm Quantum Potential (BQP) model is used for the simulation process in order to take care of the quantum effect produced in the nano scale devices. In order to record the effect of the leakage currents, which occur as a result of the thermal generation process the Auger recombination/generation and Shockley–Read–Hall (SRH) model is used. The impact of Quantum confinement is not taken for consideration in this case as it is insignificant for the junction-less transistors. Gummel-Newton method is used for mathematical calculations in this study. During the whole simulation process the temperature is set at 300K. The simulation model used in this case is calibrated with the experimental data which is published in [34] and is represented in Fig.2.

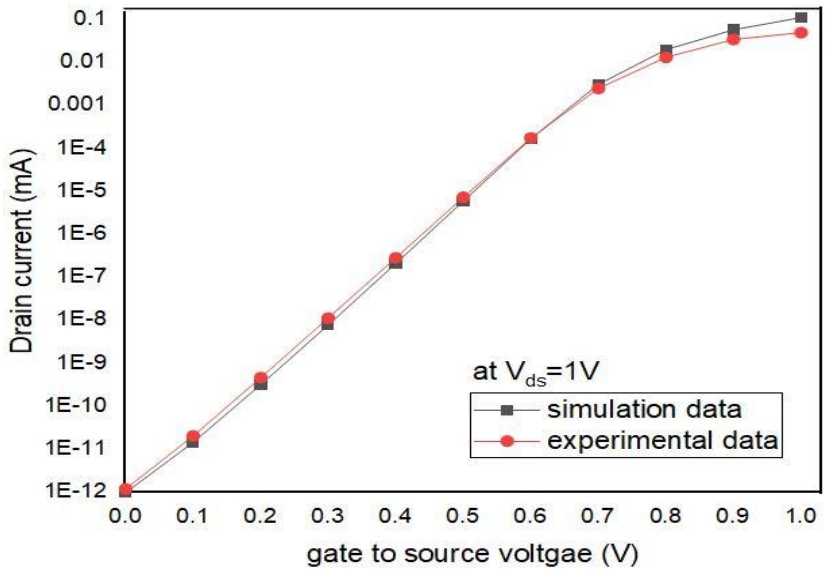

Fig.2. The calibration of the Drain Current w.r.t. Gate to Source Voltage of the FinFET against experimental data [22]

SECTION III

Results and Discussion

To investigate the effect of oxide (SiO_2) layer thickness, the Silicon dioxide (SiO_2) material thickness was altered in the range of 0.8 nm to 3 nm, while preserving the overall dimension of the FinFET static at 30 nm. To perceive the influence of the oxide layer thickness on numerous vital performance parameters like drain current, transconductance, output conductance, TGF, parasitic capacitances, cut-off frequency, gain bandwidth product and maximum frequency of oscillation etc. SOI FinFETs were simulated and investigated for structures with different oxide layer thickness.

1. *ANALOG PERFORMANCES*

In Fig.3 the variation of drain current with respect to gate to source voltage is plotted for FinFETs with variation in SiO_2 layer thickness and it can be noticed from the graph that the drain current improves for lesser oxide layer thickness which suggests that, in order to get a better drain current the oxide layer thickness should be reduced. By plummeting the SiO_2 thickness, the oxide capacitance (C_{ox}) enhances, which intern rises the drain current as it is directly proportional to the C_{ox}.

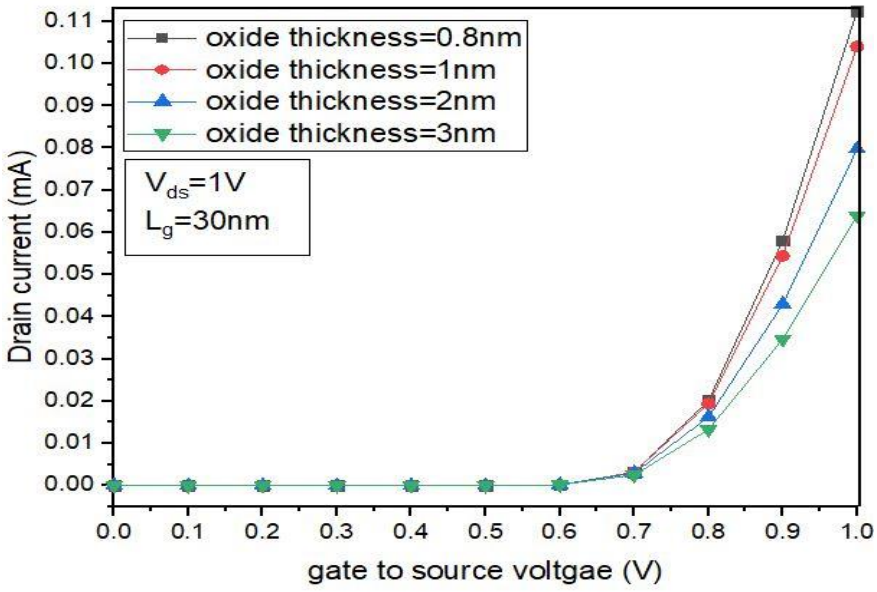

Fig.3. variation of Drain Current w.r.t. Gate to Source Voltage for different oxide layer thickness

For operations at higher frequencies, the transconductance (g_m) plays a dynamic part as it implies the exaggeration capability of the FinFET. It is mathematically denoted as [35],

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad \text{----------(1)}$$

Fig.4 shows the variation of transconductance with respect to gate to source voltage for the FinFETs with different SiO_2 layer thickness, which displays that the lower value of oxide layer thickness provides better transconductance value. In other words, it can be said that the transconductance worsens due to rise in SiO_2 thickness. This happens due to the fact that the transconductance is proportional to drain current, and the drain current is increasing with reduction in oxide layer thickness.

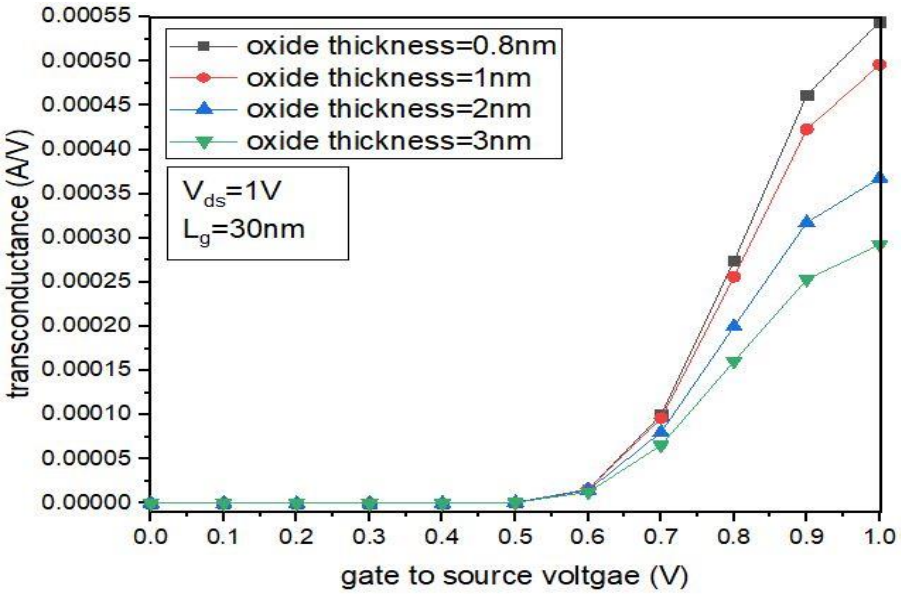

Fig.4. variation of Transconductance w.r.t. Gate to Source Voltage for different oxide layer thickness

To analyse the impact of both transconductance and drain current on the device, the transconductance generation factor needs to be examined. The transconductance generation factor is considered to be the attainable gain per unit power dissipation. In a semiconductor-based device, the TGF attains a higher value at lower range of input i.e., Vgs and decreases severely with rise in gate to source voltage. The device with higher transconductance generation factor is desirable. Mathematically it is defined as [35],

$$TGF=\frac{g_m}{I_D} \quad \text{----------(2)}$$

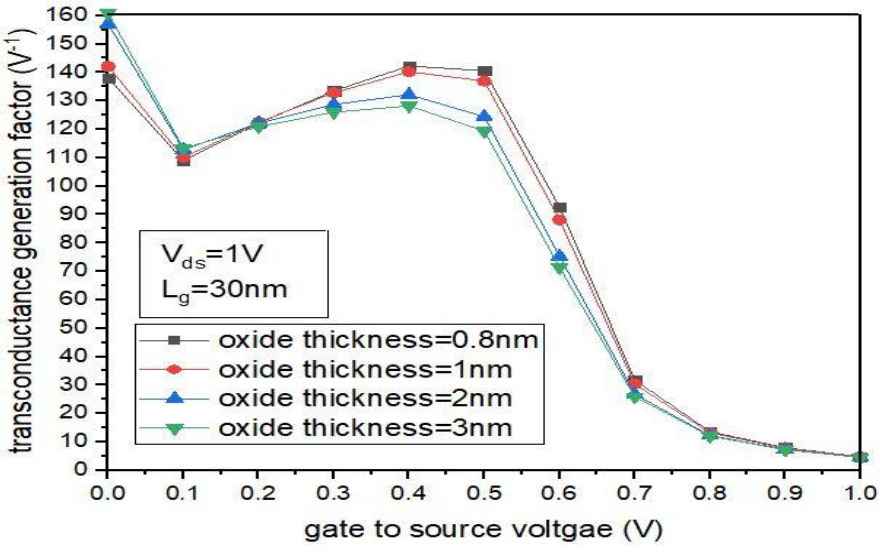

Fig.5. variation of Transconductance Generation Factor w.r.t. Gate to Source Voltage for different oxide layer thickness

Fig.5 shows the variation of transconductance generation factor with respect to gate to source voltage for the FinFETs with different SiO_2 layer thickness, which displays that the lower value of oxide layer thickness provides better transconductance generation factor value.

The next parameter which should be analysed is the output conductance (g_{ds}) which determines the overall gain of the device. The variation of output conductance with respect to gate to source voltage is plotted in Fig.6 by varying the SiO_2 layer thickness from 0.8 nm to 3 nm and it is clear from the graphical analysis that the structure with lesser oxide layer thickness possesses maximum output conductance. The reason behind such behaviour of the output conductance is that, the output conductance is proportional to the rate of change in drain current. As the drain current increases for device with lower oxide thickness, the output conductance also increases when the thickness of the oxide layer reduces.

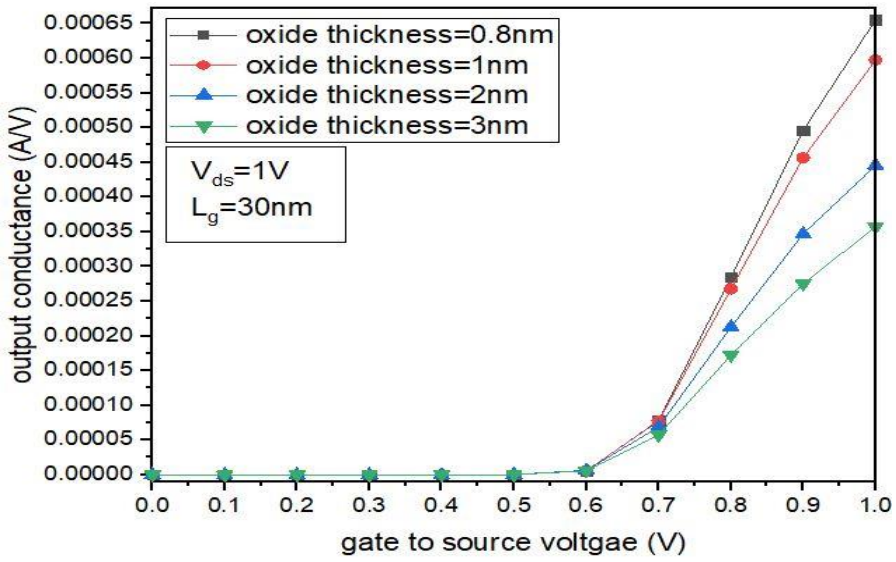

Fig.6. variation of Output Conductance w.r.t. Gate to Source Voltage for different oxide layer thickness

2. *RF ANALYSIS*:

The internal parasitic capacitances play a vital role in the radiofrequency (RF) performances of any device. The behaviour of different parasitic capacitances is plotted in Fig. 7,8,9,10. The change in gate to drain capacitance (Cgd) with respect to gate to source voltage is represented in Fig.7. In Fig.8 the change in gate to source capacitance(Cgs) with respect to gate to source voltage is plotted. Fig.9 displays the change in gate to gate capacitance (Cgg) with respect to gate to source voltage. In each case the thickness of the SiO_2 layer is altered in the range of 0.8nm to 3nm and the behaviour of each structure is analysed. It is found in all the cases that the parasitic capacitance values get reduced for increment in oxide layer thickness.

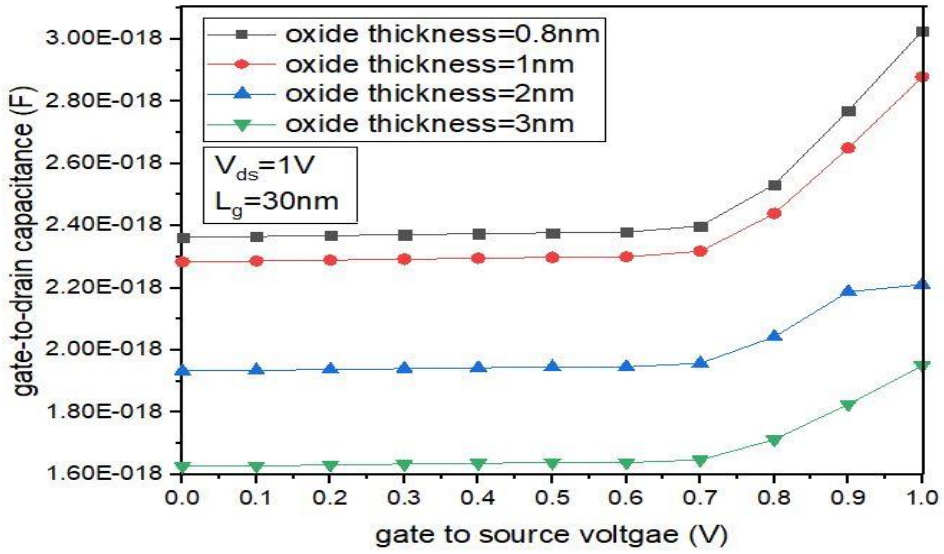

Fig.7. variation of Gate to Drain Capacitance w.r.t. Gate to Source Voltage for different oxide layer thickness

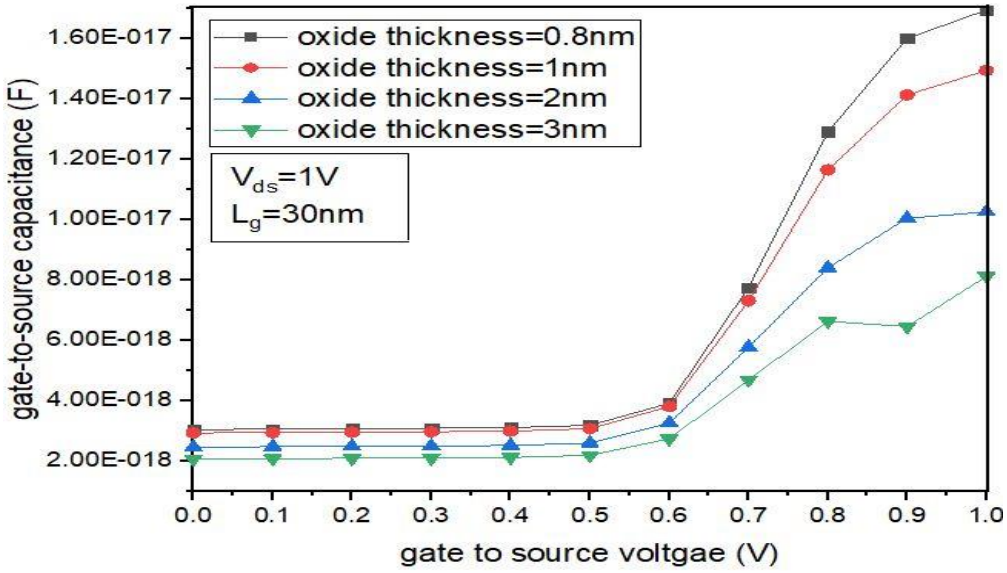

Fig.8. variation of Gate to Source Capacitance w.r.t. Gate to Source Voltage for different oxide layer thickness

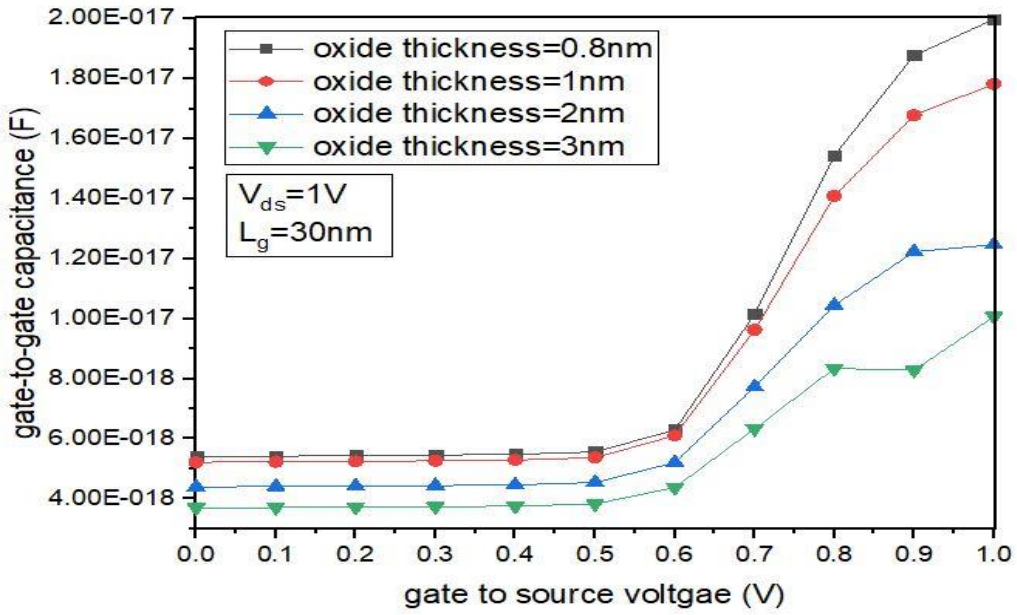

Fig.9. variation of Gate to Gate Capacitance w.r.t. Gate to Source Voltage for different oxide layer thickness

The dependency of all the internal capacitances i.e., gate-to-drain capacitance, gate-to-source capacitance and gate-to-gate capacitance on the variation of SiO_2 layer thickness is displayed in Fig.10. It is observed that the parasitic capacitance values get better due to increment in oxide layer thickness as the thickness of the oxide layer is inversely proportional to the internal capacitance.

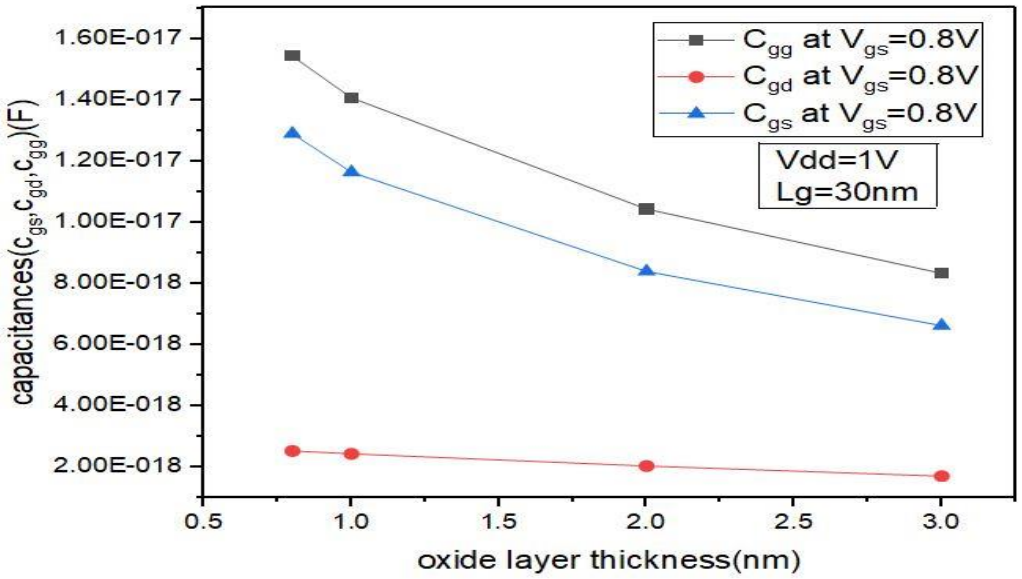

Fig.10. variation of Capacitances (Cgs,Cgd,Cgg) w.r.t. oxide layer thickness for a fixed Gate to Source Voltage

The cut-off frequency (f_T) is treated as the utmost imperative component to be studied when it comes to RF applications. It is the frequency value for which the device attains the current gain value as '1' and is denoted as [31],

$$f_T = \frac{g_m}{2*\Pi*C_{gg}} \quad \text{---------- (3)}$$

and $C_{gg} = C_{gs} + C_{gd}$,

where $C_{gs}$and C_{gd} are the capacitances at the source and drain terminals respectively with respect to gate terminal.

The variation of cut-off frequency with respect to gate to source voltage is analysed in Fig.11 by varying the SiO_2 thickness ranging from 0.8 nm to 3 nm and it is observed that, the device with higher oxide layer thickness achieves better cut-off frequency which suggests that, the f_T value improves with rise in SiO_2 thickness. From equation (3) it is clear that the cut-off frequency is inversely proportional to the capacitance which increases for lower oxide layer thickness. So, the device with lower values of oxide layer thickness possesses lesser cut-off frequency compared to the device with higher oxide layer thickness.

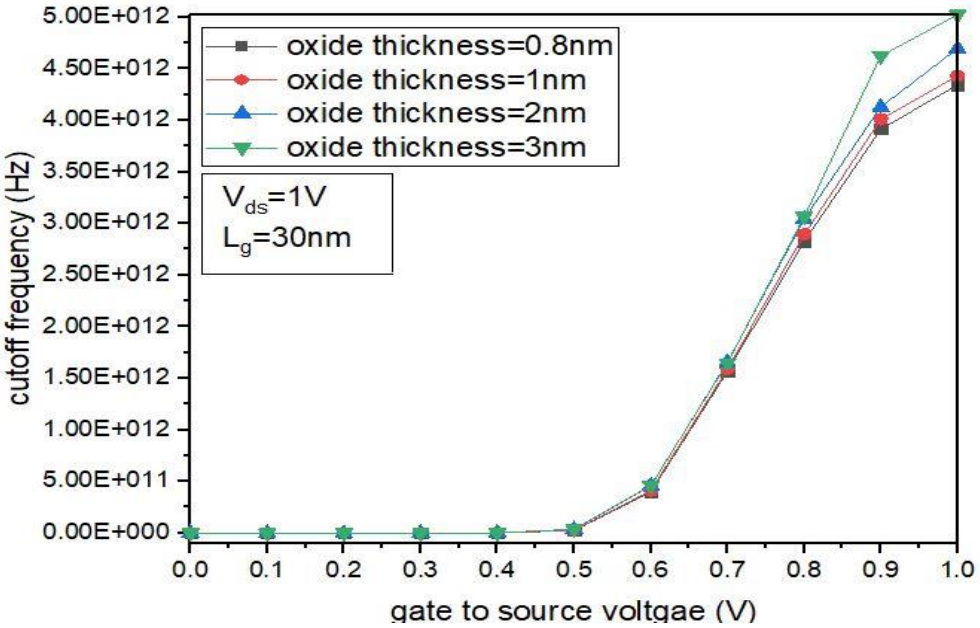

Fig.11. variation of Cutoff Frequency w.r.t. Gate to Source Voltage for different oxide layer thickness

The maximum frequency of a device is defined as the frequency at which the power gain becomes unity. It is mathematically defined as [31],

$$f_{max} = \frac{g_m}{2*\Pi*C_{gs}\sqrt{4(R_s+R_i+R_g)*(g_{ds}+g_m(\frac{C_{gd}}{C_{gs}}))}} \quad \text{---------- (4)}$$

where Rg, Rs, and Ri are the gate, source and channel resistances respectively [36].

The dependency of the maximum frequency of oscillation on the oxide layer thickness variation is analysed through Fig.12 where the variation of maximum frequency with respect to gate to source voltage for different oxide layer thickness is represented. It is found that the maximum frequency improves with rise in oxide layer thickness. From equation (4) it is clear that the maximum frequency is inversely proportional to the parasitic capacitance which increases for lower values of oxide layer thickness. So, the device with lower values of oxide layer thickness possesses lesser maximum frequency compared to the device with higher oxide layer thickness.

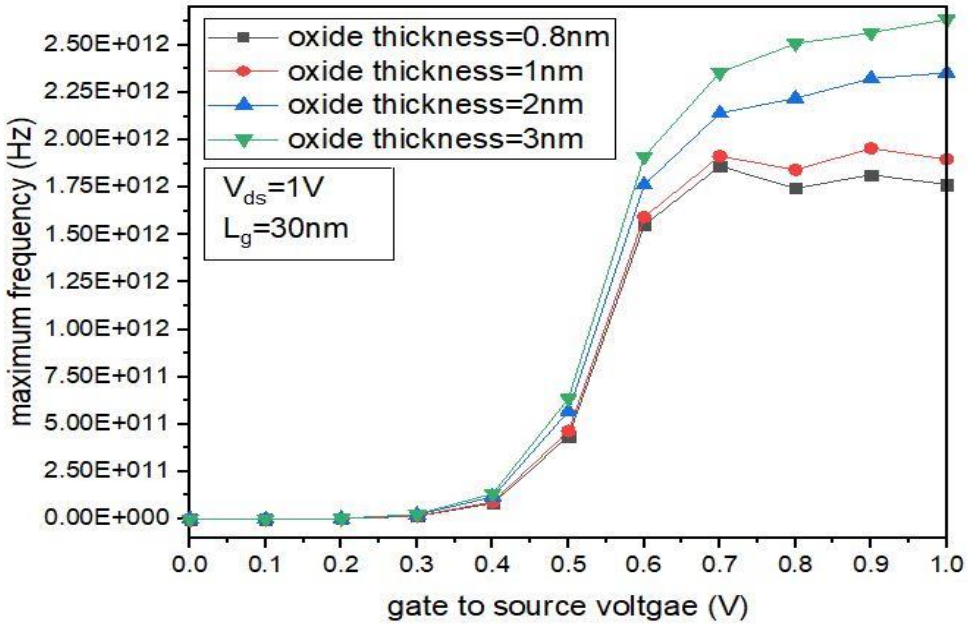

Fig.12. variation of Maximum Frequency w.r.t. Gate to Source Voltage for different oxide layer thickness

The trade-off between gain and bandwidth is calculated by Gain bandwidth product (GBW) [37,38]. For semiconductor devices it is defined as,

$$\text{GBW} = \frac{g_m}{20*\Pi*C_{gd}} \qquad \text{----------(5)}$$

The variation of gain bandwidth product with respect to gate to source voltage is represented in Fig.13 for different SiO_2 thickness. It is observed from the graph that, the GBW value gets worsen with the rise in thickness of the oxide layer. From equation (5) it is clear that the gain bandwidth is inversely proportional to the gate to drain capacitance and directly proportional to transconductance. The transconductance being the more dominant parameter helps to improve the gain bandwidth for device with lower value of oxide layer thickness.

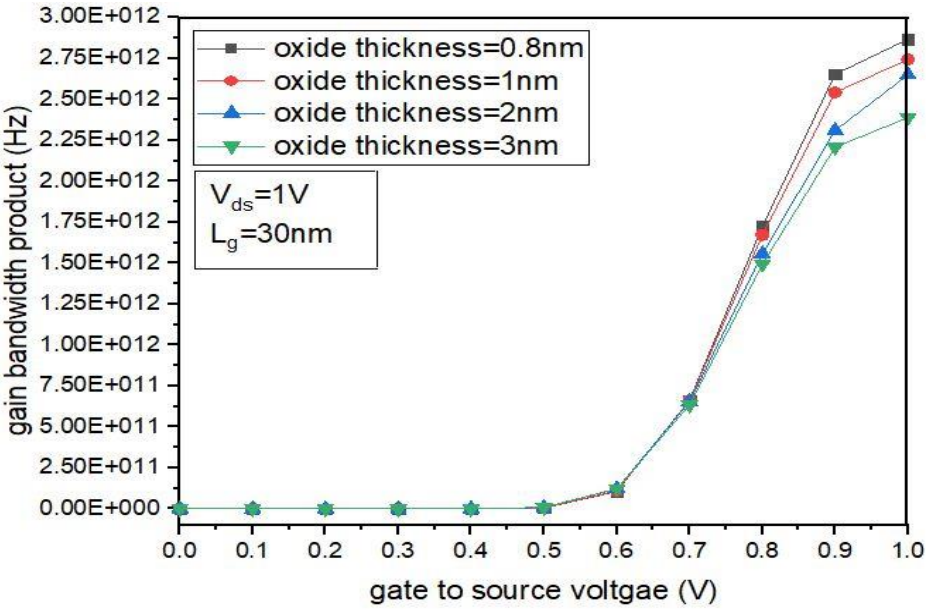

Fig.13. variation of Gain Bandwidth Product w.r.t. Gate to Source Voltage for different oxide layer thickness

All the performance parameters simulated above for different oxide layer thickness at fixed gate to source voltage, V_{GS}= 0.8V and drain to source voltage, V_{DS}=1V are represented in tabular form through Table-2.

TABLE-2

COMPARISION OF ANALOG/RF FOMS FOR DIFFERENT OXIDE LAYER THICKNESS AT V_{GS} = 0.8 V, V_{DS} =1.0V

Figure of Merits(FOMs)	**Oxide thickness=0.8 nm**	**Oxide thickness=1 nm**	**Oxide thickness=2 nm**	**Oxide thickness=3 nm**
Drain Current (I_D)	2.02E-05	1.94E-05	1.63E-05	1.33E-05
Transconductance (g_m)	2.74E-04	2.56E-04	2.00E-04	1.61E-04
Output Conductance(g_{ds})	2.84E-04	2.68E-04	2.13E-04	1.72E-04
Transconductance Generation Factor (TGF)	1.36E+01	1.32E+01	1.23E+01	1.21E+01
Gate to Drain Capacitance (C_{GD})	2.53E-18	2.44E-18	2.04E-18	1.71E-18
Gate to Source Capacitance (C_{GS})	1.29E-17	1.17E-17	8.41E-18	6.63E-18
Gate to Gate Capacitance (C_{GG})	1.55E-17	1.41E-17	1.05E-17	8.34E-18
Cut off frequency (f_T)	2.83E+12	2.90E+12	3.05E+12	3.07E+12
Maximum frequency (f_{max})	1.75E+12	1.84E+12	2.22E+12	2.51E+12
Gain Bandwidth Product (GBW)	1.72E+12	1.67E+12	1.56E+12	1.49E+12

SECTION-IV

Conclusion

In this paper, the basic FinFET structure has been analysed by varying the oxide layer thickness while maintaining the total dimension of the FinFET a constant. Different analog and radio frequency performance parameters of the device like the drain current, transconductance generation factor, transconductance, parasitic capacitances, output conductance, cut-off frequency, gain bandwidth product and maximum frequency of oscillation are determined. From the analysis it is observed that the drain current, transconductance generation factor, transconductance, gain bandwidth and output conductance degrade with increment in oxide layer thickness. Whereas the parasitic capacitances get better when the oxide layer thickness rises, due to which the cut-off frequency and maximum frequency improves at higher oxide layer thickness. Hence, it can be concluded that the increment in oxide layer thickness improves the radio frequency parameters whereas degrades the analog parameters.

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There is no funding for this research work.

Conflict of Interest

The authors declare that they have no conflict of interest.

Author contributions: Dhananjaya Tripathy- Conceptualization, methodology, simulation and investigation, Debiprasad Priyabrata Acharya - Writing original draft preparation, reviewing and editing, Prakash Kumar Rout - Validation and overall correction.

Availability of data and material

The authors confirm that the data supporting the findings of this study are available within the article, its supplementary materials or below mentioned references.

Compliance with ethical standards

This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to participate

All authors freely agreed and gave their consent to participate on this work.

Consent for Publication

All authors freely agreed and gave their consent for the publication of this paper.

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