Slot-Die-Printed Sodium-Embedded Alumina Enables High-Performance, Wafer-Scale MoS2 Electronics

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Abstract

Two-dimensional nanomaterials offer a promising new avenue in the forthcoming era of Beyond Moore electronics, due to their unique feasibility for forming van der Waals contacts alleviating detrimental interfacial electronics losses. However, their scalable production *via* solution processing compels the competition between achieved material quality and scalability, leaving them incompetent for practical electronics applications. Here, we, for the first time, have realized a large-scale solution-processed MoS_2 transistor arrays *via* slot-die printing, in which devices exhibited exceptionally high average electronic mobility exceeding 100 $cm^2 V^{-1} s^{-1}$. A set of comprehensive temperature-dependent and spatial-distribution characteristics analyses revealed that the use of sodium-embedded alumina (SEA) as the gate dielectric enabled the charge transport on MoS_2 through long-range charge percolations among low density deep charged-traps, allowing transistor performance to be dramatically boosted. Furthermore, we have successfully demonstrated various functional logic gates, NOT, NOR, NAND and SRAM, *via* wafer-scale homogeneous slot-die printing of both MoS_2 and SEA.

Background

Solution-based processing of low-dimensional materials has been considered as a promising route toward scalable synthesis for their use in practical electronics in a cost-effective manner[1-5]. In general, desired nanomaterials are stabilized in a solvent as an ink form via wet chemistry[6-8], and subsequently deposited on a target substrate using readily available coating techniques (e.g., spin coating, spray coating, vacuum filtration, and inkjet printing)[9,10]. Among various candidates, two-dimensional (2D) nanosheets have been considered as promising solution-processable materials for use in large-scale electronics[11-13]. In particular, the possibility of having atomically clean, dangling bonds-free surfaces renders them uniquely feasible for forming van der Waals (vdW) contacts with neighboring nanosheets, which enables minimized charge transport loss at the interfaces when they form thin-film network structures[14,15]. Furthermore, in the similar manner to 0D quantum dots and 1D CNTs, a wide range of 2D nanomaterials possessing various electronic properties can be exfoliated from their bulk crystals and dispersed in a solvent as a stable ink.[16,17]

Among the 2D family, semiconducting molybdenum disulfide (MoS_2) has been most intensively studied as a potential candidate for next-generation electronics due to their intriguing physical, chemical, and optical properties[18-20]. However, MoS_2 has not been fully implemented in practical demonstrations yet due to difficulties in minimizing the trade-off between scalable synthesis and material quality. For example, the liquid-phase exfoliation enabled a large-scale production of dispersed MoS_2 nanosheets, but the small lateral size (< 100 nm) of exfoliated nanosheets hindered effective formation of an electrically conductive thin-film structure. Instead, molecular intercalation-based electrochemical exfoliation method offered an alternative scalable route for the homogeneous production of relatively large (>1 μm) few-layered MoS_2 nanosheets, but the field-effect mobility of their wafer-scale transistor arrays has been

limited to 10 $cm^2 V^{-1} s^{-1}$ at room temperature[13]. Although this value was comparable to those of micromechanically-exfoliated MoS_2 devices fabricated on conventional oxidized silicon substrates, it still lags far behind the phonon-scattering-limited field-effect mobility of bulk MoS_2 placed in the range of 200–500 $cm^2 V^{-1} s^{-1}$ at room temperature[21]. One possible solution to maximize the field-effect mobility of solution-processed MoS_2 thin-film is employing high-k dielectric layers such as HfO_2 and Al_2O_3[22-25]. In the previous report, for example, the average field-effect mobility of micromechanically exfoliated MoS_2 nanosheets has been significantly improved more than two orders of magnitude by introducing HfO_2 grown by atomic layer deposition (ALD) as a high-k gate dielectric[11]. Although ALD can produce dielectric layers over large areas in high quality, the process is limited by slow deposition rate and difficulties achieving controlled doping because the reactions between the precursors are complicated.[26,27]

In this work, we demonstrate a wafer-scale solution-processed MoS_2 thin-film transistor array with average field-effect electron mobility exceeding 100 $cm^2 V^{-1} s^{-1}$ at room temperature. The consecutive slot-die printings of sodium-embedded alumina (SEA) and MoS_2 nanosheet inks were employed for the scalable construction of gate dielectric and semiconducting layers on wafer, respectively. A comprehensive suite of analyses based on temperature-dependent charge transport behavior and scanning probe microscopy revealed that the exceptionally high electron mobility of MoS_2 on SEA was attributed to the low-density incursion of deep charged impurities with reduced shallow electronic fluctuations, which allowed the predominance of long-range percolation of charges. Finally, as a demonstration of scalable thin-film formation with extremely low operational cost at room temperature, various functional logic gates including NOT, NOR, NAND, and SRAM are presented in wafer scale.

Device fabrication based on slot-die coating

To realize wafer-scale fabrication of MoS_2-based field-effect transistor (FET) arrays, both sodium-embedded alumina (SEA) precursor solution and MoS_2 flake dispersion are sequentially coated on an arbitrary rigid substrate *via* a slot-die coating method as illustrated in **Figure 1a** (photographs of as-prepared dispersions, MoS_2 flake morphology, and films coated on transparent glass substrates are shown in **Supplementary Figs. 1** and **2**). An optical image of the slot-die coater for preparing wafer-scale electronics is shown in **Figure 1b**. First, SEA precursor solution was carefully injected into the head at a constant rate of 2.5 mL min^{-1} and ejected through the nozzle placed at the bottom of the head. While the solution is ejecting, the slot-die head is simultaneously moving in x-y directions at a constant rate of ~10 mm s^{-1} for homogeneous coating of SEA on the substrate. Subsequently, MoS_2 dispersion was coated in the similar manner to form a semiconducting layer on the SEA layer (**Supplementary Video 1**). For successful formation of the semiconducting layer, MoS_2 dispersion was prepared by molecular intercalation-driven electrochemical exfoliation followed by a mild bath sonication in a solvent. Photographs taken after each layer coating on a 5-inch Si wafer are shown in **Figure 1c**. The resulting MoS_2/SEA layers were subjected to fabricate a conventional FET structure as illustrated in **Figure 1d**, where the corresponding atomic structures of MoS_2 flake and SEA are represented. Based on the

structure, a representative electrical transfer curve on a semi-logarithmic scale (red curves) and a linear scale (blue curve) is shown in **Figure 1e**. As the gate voltage sweeps to the positive values, the drain current turns on abruptly at $V_G \approx 0$ V with a high on/off ratio (>10^5) and a negligible hysteresis loop during the forward and reverse sweeps. The corresponding output curve exhibit a typical n-type FET behavior having the drain current increase and eventually saturate as the drain voltage increases (**Supplementary Fig. 3**). From the transfer characteristics, field-effect carrier mobility values are extracted based on the equation, $I_D = C_i \mu W (V_G - V_{th})/L$,

where I_D is the drain current; C_i is the effective capacitance of gate insulator; V_G and V_{th} are the gate voltage and threshold voltage, respectively; L and W are the channel length and width, respectively. The carrier mobilities of 49 transistors in a fabricated array are shown in **Figure 1f** as a two-dimensional (2D) color mapping, which shows high spatial homogeneity with an average value of ~112 ± 4.6 $cm^2 V^{-1} s^{-1}$ at room temperature (the transfer curves for all 49 FETs are shown in **Supplementary Fig. 4**). This is the record-high mobility among wafer-scale MoS_2-based FETs reported to date, and the processing temperature for MoS_2 channel formation (250 ℃) is much lower compared to CVD-based devices (**Supplementary Fig. 5** and **Supplementary Table 1**). Color maps and statistics of carrier mobility, turn-on voltage, and current on/off ratio are shown in **Supplementary Figs. 6** and **7**. To elucidate the origin of high carrier mobilities, effective capacitance values of the slot-die coated SEA dielectric layer were measured by forming a metal-insulator-metal (MIM) structure with thermally deposited Cr/Au electrodes placed on top. The resulting frequency-dependent capacitance and phase angle measured by an impedance spectroscopy are shown in **Figure 1g**. Notably, the specific capacitance measured at 1 Hz is ~0.9 μF cm^{-2}, which is 18 times higher than that of an Al_2O_3 dielectric with a comparable thickness (~0.05 μF cm^{-2})[28]. To understand the origin of the high capacitance, we explored frequency dependence. The capacitance is nearly constant until the frequency increases up to 100 Hz, and then gradually decreases as the frequency further increases. For the same frequency range, the measured phase angle also goes toward 0° and gradually returns to -90° when the frequency increases, which implies that the dominant working mechanism changes from capacitive (-90°) to resistive (toward 0°) and back to capacitive operation.[29-32] These frequency-dependent capacitance and phase angle changes are mainly attributed to the displacement of Na^+ ions embedded in alumina and their limited polarization response time.[33-36] Eventually, the measured capacitance values become close to ~0.1 μF cm^{-2}, which is similar to the reported capacitance of the pristine Al_2O_3. **Figure 1h** shows the distribution of 49 capacitance measurements, where the color intensity indicates the value of measured capacitance and x and y axis designate spatial positions. Based on the spatial mapping, an average capacitance value of 0.907 ± 0.002 μF cm^{-2} was shown with high spatial uniformity (0.055 μF cm^{-2}).

Based on the SEA layer possessing a high average capacitance, we further explored solution-processed MoS_2-based electronics to investigate the origin of the working principle and maximize the device performance. As we illustrated in **Figure 1**, SEA and MoS_2 layers are sequentially coated via slot-die

coating, and subsequently the MoS_2 layer is subjected for chemical doping by exposure to bis(trifluoromethane) sulfonimide (TFSI) followed by heat treatment (**Figure 2a**). The resulting electrical transfer characteristics are shown in **Figure 2b** after each step (i.e., MoS_2 coating, TFSI treatment, and heat treatment). First, the MoS_2 ink concentrations are varied from 1 mg mL^{-1} to 3 mg mL^{-1} to optimize the slot-die-coated channel thickness (**Supplementary Fig. 8**). Based on the electrical characteristics of each thickness, we decided to use 2 mg mL^{-1} for the rest of the device fabrication (**Supplementary Fig. 9**). While the as-coated MoS_2 thin-film shows a current on/off ratio of ~7×10^2, subthreshold swing (SS) of 1.58 V dec^{-1}, and threshold voltage (V_{th}) of 0.16 V with a heavily n-doped electrical behavior due to the sulfur vacancies formed during the processing (gray line), the unintentional doping is significantly recovered by TFSI-assisted chemical treatment (black line). After the chemical treatment, the transfer characteristics significantly changed with the current on/off ratio of ~10^5, SS of 0.32 V dec^{-1}, and positively shifted V_{th} of 3.23V. As previously reported, TFSI molecules play a role to passivate sulfur vacancies on the basal plane of MoS_2 nanosheets, which act as carrier trapping sites[13]. Also, the charge density of MoS_2 is reduced because the TFSI molecules serve as a Lewis acid to withdraw electrons[37]. Therefore, as the resulting transfer characteristic curve shows, the TFSI-treated MoS_2 device shows SS improved ~5 times and V_{th} shifted toward a positive direction compared to those of as-coated MoS_2 thin-film counterpart. The electrical characteristics corresponding to the TFSI treatments with various concentrations are shown in **Supplementary Fig. 10**. A comprehensive suite of characterizations including Kelvin probe force microscopy (KPFM), Raman spectroscopy, Photoluminescence (PL) spectroscopy and x-ray photoelectron spectroscopy (XPS) is also performed to reveal the effect of TFSI concentration on the properties of the MoS_2 thin-film (**Supplementary Fig. 11–13**). Following the chemical treatment, an additional annealing process further improves MoS_2 nanosheet-to-nanosheet contact and removes residual solvent, and then the resulting current level improves at least one order of magnitude at the applied gate voltage of 5 V (red line). Transfer characteristics at various annealing temperatures (100 °C, 150 °C, 200 °C, 250 °C, and 300 °C) are plotted in **Supplementary Fig. 14a**. As the annealing temperature increases up to 250 °C, on current increases and V_{th} shifts to negative, and then the device performance is slightly degraded after annealing at 300 °C. The corresponding carrier mobility and current on/off ratio as a function of annealing temperature are plotted in **Supplementary Fig. 14b,** and the corresponding work function distribution are plotted in **Supplementary Fig. 15.** The decreased carrier mobility and increased off current of the device annealed at 300 °C are possibly due to the partial oxidation of MoS_2 to MoO_x[38].

To elucidate the origin of the ultrahigh carrier mobility (>100 $cm^2 V^{-1} s^{-1}$) of our solution-processed MoS_2-based transistors, thorough analysis has been performed on the SEA dielectrics along with alumina (Al_2O_3) dielectrics without sodium, which we used as control samples for comparison in depth. The alumina dielectric layers were prepared in two conventional ways: atomic layer deposition (ALD) and solution processing (spin-coated). MoS_2 FETs fabricated on both alumina dielectrics show an average carrier mobility of ~10 $cm^2 V^{-1} s^{-1}$, which is comparable to the previously reported value[13]. To reveal

charge transport mechanisms, we further investigated electrical characteristics of the devices as a function of temperature. Frequency-dependent dielectric properties of the SEA at different temperatures are shown in **Supplementary Fig. 16**. Transfer curves of MoS_2 FETs based on SEA and control alumina dielectrics were also measured as a function of temperature (**Supplementary Figs. 17** and **18**). **Figure 2c** shows temperature-dependent electrical conductivity (σ) of MoS_2 FETs fabricated on the SEA dielectric layer at different gate voltages extracted from the temperature-dependent transfer curves (**Supplementary Fig. 17**). The resulting curves are well-fitted with the 2D variable range hopping (2D VRH) model below 280 K with an equation $\sigma \sim \exp\left[-\left(\frac{T_1}{T}\right)^{\frac{1}{3}}\right]$, where σ is the conductivity of semiconductor channel, T is the temperature, T_1 is a constant related to the size of 2D localized states (a, $T_1 \sim a^2$).[39,40] In **Supplementary Fig. 19**, both control samples fabricated on solution-processed and ALD alumina dielectrics are also fitted using the 2D VRH model extracted from the temperature-dependent transfer curves (**Supplementary Fig. 18**). **Figure 2d** shows the equivalent carrier concentrations extracted from an equation $n = C_i(V_G - V_{th})$ and the corresponding T_1 values. SEA-gated MoS_2 FETs show higher T_1 values compared to alumina-gated counterparts, which implies wider localization length for the case with SEA[41]. At high temperatures, electrical conductance of the Al_2O_3-gated MoS_2 FETs show stronger temperature dependence, which is possibly attributed to the transition from variable-range hopping to nearest-neighbor hopping (NNH) mechanism[40,42]. The NNH can be fitted by the Arrhenius equation $\sigma \sim \exp\left[-\left(\frac{T_0}{T}\right)\right]$,

where σ is the conductivity of semiconductor channel, T is the temperature, T_0 represents the activation energy for carrier. The T_0 values extracted from the equation are plotted in **Figure 2e**. Higher T_0 values of MoS_2 FETs on the SEA layer indicate that deep trap states exist in the SEA. These results suggest that the charge transport in MoS_2 on SEA is largely governed by the long-range percolation through deep traps, assuming the constant density of states near the Fermi edge. Moreover, considering that the ratio of characteristic temperatures ($\gamma = T_1/T_0$) reflects the ratio between intersite distance (d_{NN}) and a, higher γ along with higher a indicates that the density of traps in SEA-gated MoS_2 devices is lower compared to the alumina-gated MoS_2 cases **(Supplementary Fig. 20)**. In this sense, we further clarified the origin of 2D VRH behavior based on the KPFM analysis[43].

The top image of **Figure 2f** shows the work function distribution of SEA surface measured using KPFM. Slightly bright and dark spots were observed throughout the whole plane, while no such distribution was observed on Al_2O_3 (**Supplementary Fig. 21a**). To obtain more detailed spatial distribution of work functions on our dielectric film, we performed 2D fast Fourier transform (2D FFT) of the measured work function distribution (**Figure 2f**, bottom image). The yellow/green spots visible on the 2D FFT plot imply that regions with more than 10 meV difference in work functions compared to the surrounding areas are periodically appearing. In the case of SEA, the yellow/green spots in the 2D FFT images are observed at

frequencies close to 0.1 nm^{-1}. For Al_2O_3 (**Supplementary Fig. 21b**), the yellow/green spots are highly concentrated at frequencies close to 0.8 nm^{-1}. The distribution of work function was fitted by gaussian plot and shown in **Figure 2g**, which showed a slight broadening in the distribution of work function in SEA dielectric compared to Al_2O_3. On the other hand, the distribution of amplitudes from the 2D FFT images (**Figure 2h**) clearly demonstrates larger densities in Al_2O_3 than SEA for the local fluctuations with low amplitudes (<10^{-3} eV). At higher amplitudes (>10^{-3} eV), SEA showed larger densities. It can be reasonably deduced that Al_2O_3 has a strong oscillating work function distribution with high frequencies but small amplitudes, and SEA shows a weak oscillating work function distribution with low frequencies but large amplitudes. Also, oscillating work function distribution with small amplitudes exists much less in SEA (**Figure 2h**). By summing up the information, we can roughly estimate the density of state (DOS) as well as their spatial distribution for Al_2O_3-gated and SEA-gated MoS_2 devices, as schematically illustrated in **Figure 2i**. The low-density incursion of deep trap states along with reduced shallow electronic fluctuations explains the large temperature dependence of SEA-gated MoS_2 transistors as well as the dominance of long-range percolations, which agrees with the highly boosted charge carrier mobility achieved in our system.

Applicability to large-area logic circuits

In order to verify the applicability of our transistors to large area electronics, various logic circuits were fabricated and tested: NOT, NOR, NAND, and SRAM **(Figure 3a)**. The circuit diagram of a NOT gate (inverter) is illustrated in **Figure 3b**. Two identical MoS_2 transistors were used as both driver and load transistor. Voltage transfer characteristics at different supply voltages (V_{DD}) and the resulting signal gain are shown in **Figure 3c**. An output voltage equal to the supply voltage was measured at low input voltages (close to 0 V), which corresponds to the logic state “1”. The output voltage decreased to 0 V as the input voltage increased, which corresponds to the logic state “0”. This clear inversion of voltage confirms good NOT gate operation. Signal gain (absolute value of dV_{OUT}/dV_{IN}) higher than 7 was achieved. **Figure 3d** shows circuit diagrams of NAND and NOR gates. Both NOR and NAND gates utilize three identical MoS_2 transistors; two in parallel and one in series for NOR gate, all three in series for NAND gate. In a NAND gate, the output voltage is 2 V (logic sate “1”) when at least one of the input voltages are 0 V (logic state “0”). And the output is at logic state “0” only when both of the inputs are at logic state “1”. For a NOR gate, the output is at logic state “1” only when both inputs are at logic state “0”. For the rest of the possible input logic combinations (i.e. (1,0), (0,1), (1,1)), output logic state is at “0”. Output voltages for both NAND (top) and NOR (bottom) gates are plotted in **Figure 3e**. Both NAND and NOR gates steadily exhibited correct output logic states for all possible input logic combinations over few repetitions. SRAM is composed of two cross connected inverters, which contain two transistors each (**Figure 3f**). In an SRAM cell, each output of an inverter is connected to the input of the other. When an initial input voltage (low or high) is applied to an inverter, the resulting output voltage (logic state 1 or 0) is fed to the input of the cross connected inverter. Then, the output logic state of the cross connected inverter is equal to the initially applied input, which is looped back into the initially operated inverter. Thus, a SRAM cell can

maintain its output level even after the input is completely opened. **Figure 3g** display the operation of SRAM at various input voltages and time span, where the shaded regions represent completely open input states. Complete maintenance of output states at open input states (shaded regions) confirms excellent operation of our fabricated SRAM cell.

Conclusion

To summarize, we have realized large-scale, solution-processed and high performance MoS_2 electronics on a 5-inch wafer by employing consecutive slot-die printings of MoS_2 nanosheet and SEA inks for semiconducting and insulating layers, respectively. The solution-processed MoS_2 FETs on the SEA layer exhibited an exceptionally high field-effect mobility exceeding 100 $cm^2 V^{-1} s^{-1}$, which is more than 10 times higher than the previously reported values[13]. The origin of such high carrier mobility was thoroughly elucidated by a comprehensive suite of analysis with respect to temperature dependence of electronic characteristics as well as spatial distribution of surface characteristics. Furthermore, the high spatial uniformity of the device performance successfully enabled to demonstrate logic circuits including NOT, NAND, NOR, and SRAM. Thus, this work can provide a new pathway for high-performance, large-area electronics based on solution-processed low dimensional materials.

Methods

Device fabrication

To prepare sodium-embedded alumina (SEA) precursor solutions, aluminum nitrate nonahydrate (98%, Sigma-Aldrich) and sodium hydrogen sulfate (Sigma-Aldrich) mixed at a molar ratio of 10:2 was dissolved in a binary solvent of ethanol (anhydrous, Sigma-Aldrich) and acetone (99.5%, Sigma-Aldrich) (volume ratio = 6:1). The final concentration was 0.6 M. Precursor solutions for Al_2O_3 dielectrics were prepared by dissolving aluminum nitrate nonahydrate (98%, Sigma-Aldrich) in 2-methoxyethanol (anhydrous, 99.8%, Sigma-Aldrich) at a concentration of 0.5 M. Both solutions were stirred with a magnetic bar for 24 h at 65 ℃. MoS_2 dispersion was prepared by electrochemical exfoliation with molecular intercalants. First, we constructed a two-electrode electrochemical cell using 50 mg of MoS_2 crystal (HQ graphene) and graphite rod as cathode and anode, respectively. Tetraheptylammonium bromide (THAB, 99.0%, Sigma-Aldrich) dissolved in acetonitrile (anhydrous, 99.8%, Sigma-Aldrich) served as an electrolyte (concentration: 5 mg mL^{-1}). To intercalate the THA^+ ions into the MoS_2 crystal, a negative voltage of 7 V was applied to the cell for 1 h. After the electrochemical reaction, as-intercalated crystal was rinsed with ethanol before sonication in polyvinylpyrrolidone (PVP, 40,000 g mol^{-1}, Sigma-Aldrich) solution in dimethylformamide (DMF) (5 mL; 22.2 mg mL^{-1}) for 30 min. To remove un-exfoliated crystals, the dispersion was centrifuged at 4,000 rpm. The supernatant was subsequently centrifuged and washed twice with isopropanol (IPA) to remove residual PVP. After rinsing, the MoS_2 flakes were redispersed in IPA at an optimized concentration.

For SEA layer printing, the precursor solution was injected by a syringe pump at a rate of 2.5 mL min^{-1} into the slot die head and out of the slot at the bottom. To slot-die coat the solution on desired substrates (p-doped 5-inch silicon wafer and ITO/glass), the stage of the slot die coater was transported at a constant rate of 10 mm s^{-1}, followed by sintering for 2 h at 500 ℃ in a furnace. To prepare Al_2O_3 samples, the precursor solution was spin coated onto UV-treated p-doped Si wafers (4,000 rpm, 30s) followed by thermal annealing for 2 h at 500 ℃ in a furnace. ALD-deposited Al_2O_3 was prepared by standard atomic-layer deposition at a processing temperature of 100 ℃.

MoS_2 flake dispersion solutions were slot-die coated on top of dielectric layers with syringe pump injection rate of 2.5 mL min^{-1} and stage transport speed of 10 mm s^{-1}. After MoS_2 flake solutions were successfully coated, procedures to enhance the electrical properties of the semiconductor film were taken; a soft baking process of 60 ℃ for 2 min, chemical doping by 10 mg mL^{-1} of bis(trifluoromethane)sulfonimide (TFSI, Sigma-Aldrich) in 1,2-dichloroehtane (Sigma-Aldrich) solvent for 30 min and thermal annealing at 250 ℃ for 30 min. Both chemical doping by TFSI and thermal annealing were proceeded in an argon-filled glove box. To form channel arrays, MoS_2 films were covered by a photoresist mask (AZ 5214E) patterned by conventional photolithography and then processed with reactive ion etching followed by photoresist lift-off. Source/drain electrodes were created by sequential thermal deposition of Cr (3 nm) and Au (30 nm) metal layers through a photolithographically patterned photoresist layer. Afterwards, a lift-off process was applied. To fabricate logic gates, an additional photolithography patterning of ITO local gate electrodes and sodium-embedded alumina were conducted before and after coating the sodium-embedded alumina.

Characterization

The surface topography and work function of the MoS_2 thin-film were characterized using atomic force microscope and kelvin probe force microscope, respectively (Park Systems NX10). The elemental composition and chemical structure were investigated using x-ray photoelectron spectroscopy (ESCALAB 250 XI, Thermo Fisher Scientific) and Raman/photoluminescence spectroscopy (MAPLE-II). Electrical impedance of sodium-embedded alumina, solution-processed Al_2O_3 and ALD-deposited Al_2O_3 was measured using VersaSTAT 4 potentiostat based on the metal-insulator-metal structure. Electrical properties for FETs and logic gates were characterized by using a vacuum probe station (under 10^{-4} Torr) and Keithley 4200 semiconductor electrometer.

Declarations

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Author Contributions

J.H.Cho and J.Kang initiated and supervised all the research. Yh.A.Kwon and Ji.K carried out and designed most of the experimental work and data analysis. D.G.Roe, D.Rhee and D.W.Kim assisted in the manuscript writing. S.B.Jo assisted in the data analysis. All authors discussed the results and contributed to the writing of the manuscript.

Conflicts of interest

There are no conflicts to declare.

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Figures

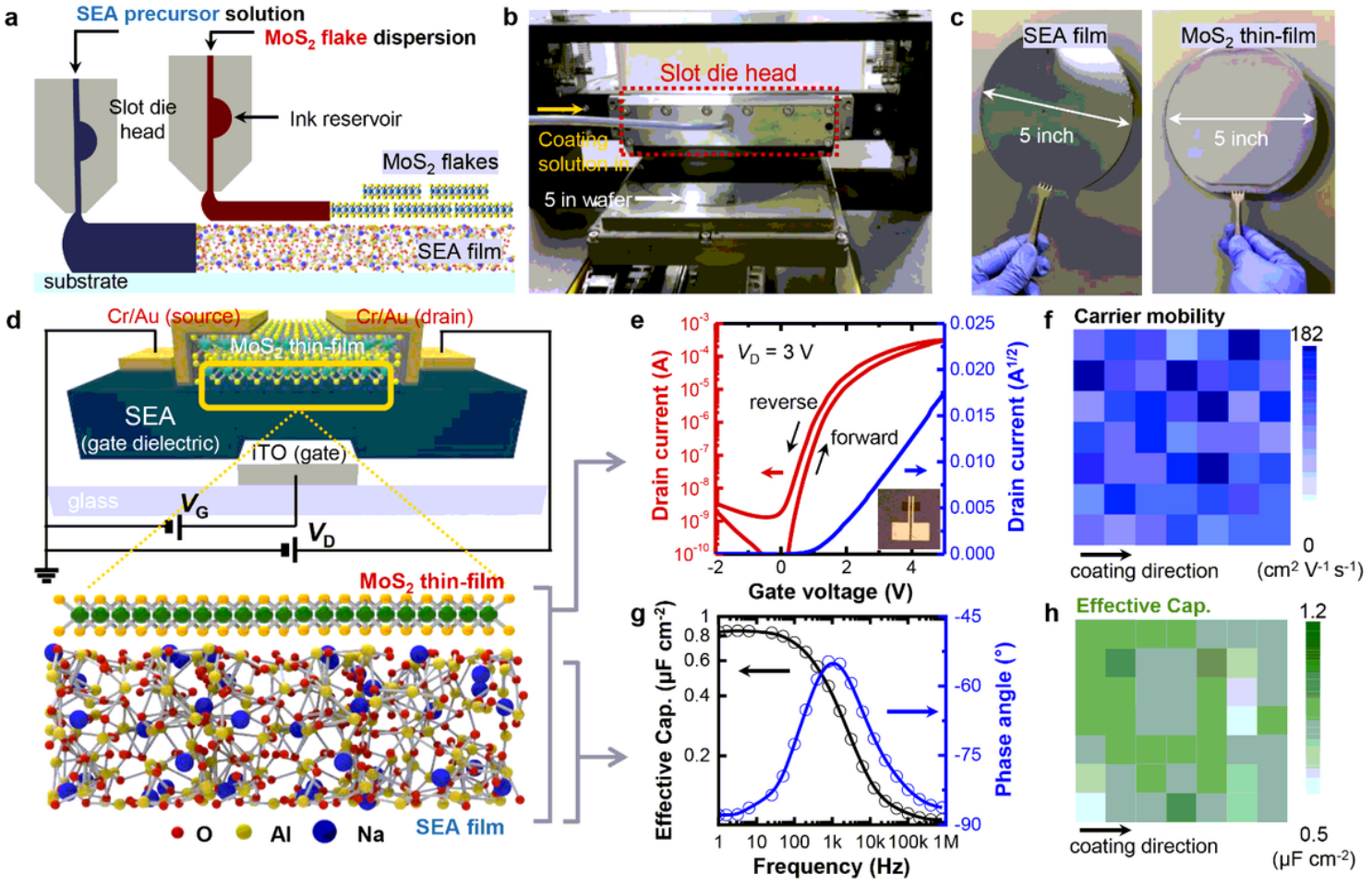

Figure 1

Device fabrication based on slot-die coating. (a) Schematic illustration of slot-die-coating of SEA and MoS_2. (b) Optical image showing the slot-die coating setup for consecutive wafer-scale coating. (c) Image of slot-die-coated SEA and MoS_2 on a 5-inch Si wafer. (d) Schematic illustration of MoS_2/SEA transistor and atomic structure of MoS_2 thin-film and SEA layer, respectively. (e) Transfer characteristics and OM image (inset) of MoS_2/SEA FET. (f) Color map of carrier mobility distribution. (g) Capacitance (left) and phase angle (right) properties of SEA with different frequencies. (h) Color map of effective capacitance distribution.

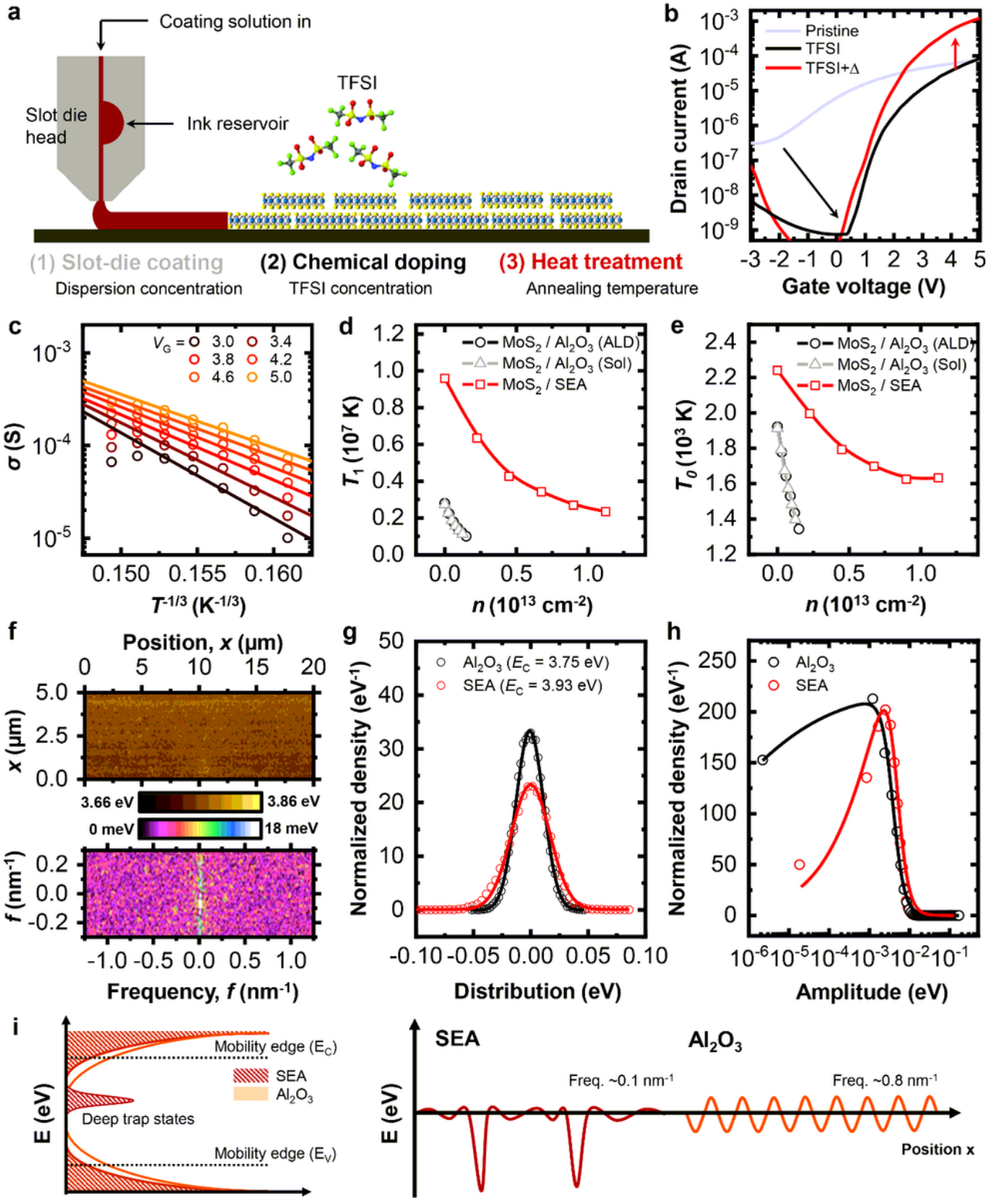

Figure 2

Device optimization and origin of high carrier mobility. (a) Schematic illustration of optimizing process of MoS_2 semiconductor film. (b) Engineering of transfer characteristics by TFSI-treatment and thermal annealing on MoS_2 transistor. (c) Conductivity (σ) plotted against $T^{-1/3}$ for sodium alumina gated devices measured at different gate voltages. 2D VRH fitted lines are shown for each gate voltage. (d) T_1 and (e)

T_0 values extracted from 2D VRH model and Arrhenius plot, respectively. (f) KPFM image (top) representing spatial distribution of work function in sodium-embedded alumina film. 2D fast Fourier transform (bottom) of the KPFM image, which visualizes the oscillating amplitude in the x and y directions. (g) Gaussian fit of work function distribution for SEA and Al_2O_3. (h) Amplitude distribution of 2D FFT image for SEA and Al_2O_3. (i) Schematic illustration of density of states (DOS) (left) and line profile of energy (right).

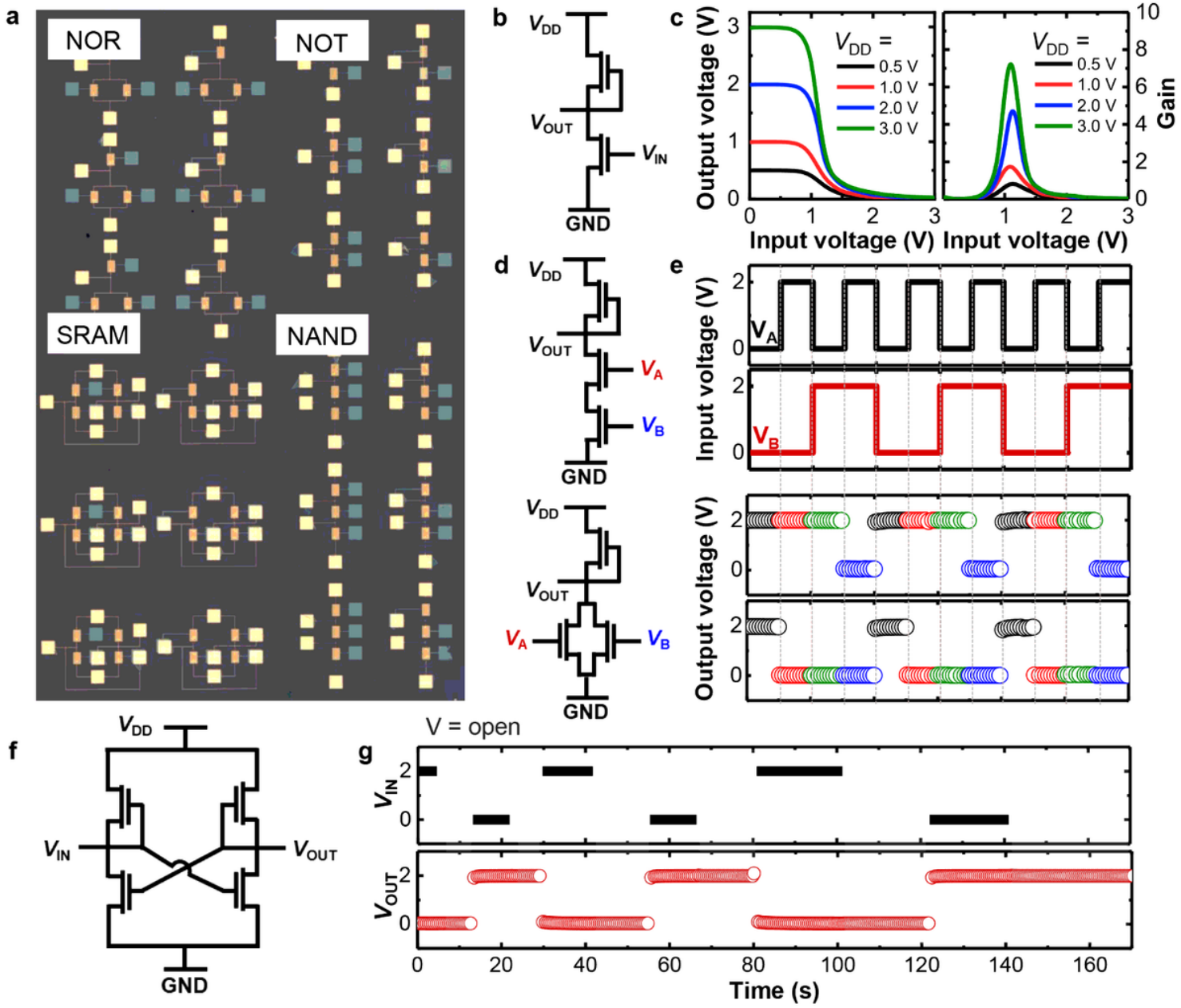

Figure 3

Applicability to large-area logic circuits. (a) Optical image of NOR, NOT, NAND, and SRAM logic gates. (b) Circuit diagram of NOT gate (inverter). (c) Voltage transfer characteristics (left) and resulting voltage gain (right) of NOT gate. (d) Circuit diagrams of NAND (top) and NOR (bottom) gates. (e) Input voltage signals (top) and the corresponding output voltage signals (bottom) of NAND and NOR gates. (f) Circuit diagram

and (g) input voltage signals and the corresponding output voltage signals of SRAM gate. The shaded regions indicate completely open input signals.

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