Modeling and Dynamics Analysis of a Universal Interface for Constructing Floating Fractional Order Mem-Elements

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Research Article

Keywords: Memory element emulators, Fractional-order circuits, Fractioanal-order capacitor, Memristor, Memcapacitor, Meminductor

Posted Date: November 30th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-1083725/v1

Noname manuscript No.
(will be inserted by the editor)

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Received: date / Accepted: date

Abstract Fractional-order systems generalize classical differential systems and have empirically shown to achieve fine-grain modeling of the temporal dynamics and frequency responses of certain real-world phenomena. Although the study of integer-order memory element (mem-element) emulators has persisted for several years, the study of fractional-order memory elements (FOMEs) has received little attention. To promote the study of the characteristics and applications of mem-element systems in fractional calculus (FC) and memory systems, in this paper, we propose a novel universal interface for constructing floating FOMEs. When the topological structure of the interface remains unchanged, the floating fractional-order memristor (FOMR), fractional-order memcapacitor (FOMC) and fractional-order meminductor (FOMI) emulators

Acknowledgments This work was supported by the Young Scientists Fund of the National Natural Science Foundation of China Grant (No. 62101142); the Guangzhou Science and Technology Plan Research Project under Grant (No. 202102020874); and the Featured Innovation Foundation of the Education Department of Guangdong Province under Grant (Nos. 2021KTSCX062, 2021ZDZX1079).

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can be realized by using the impedance combinations of different passive elements, without any mem-element emulators and mutators. When compared with previously proposed FOMEs, the proposed fractional-order mem-element emulators based on a universal interface not only feature the characteristics of floating terminals and simpler circuit structures, but can also realize all three different types of FOMEs. To explore the dynamical relationships between the mem-elements and the fractional order, we mathematically derive and analyze the maximum and minimum possible values of memductance, memcapacitance and inverse meminductance which accounts for practical design considerations when building FO systems. The memory characteristics of FOMEs are analyzed by varying their orders and stimuli frequencies. The consistency of theoretical analysis, numerical calculation and simulation results validates the correctness of our proposed emulators.

Keywords Memory element emulators · Fractional-order circuits · Fractioanal-order capacitor · Memristor · Memcapacitor · Meminductor

1 Introduction

Fractional calculus (FC) is a generalization of ordinary differential systems to an arbitrary, real order [1]. FC has been used to model real-world physical and quantum phenomena across a variety of domains which could not be achieved using integer-order dynamics alone [2–5]. Fractional derivatives have shown to successfully model the fine-grain memory and hereditary characteristics of the temporal dynamics and frequency responses of various systems. Several promising examples of the progress FC has made in applied domains include oscillators [6, 7], filters [8, 9], controllers [10, 11], sub-atomic phenomena [12], and biological systems [13, 14].

In 1971, Leon Chua theoretically predicted the existence of the 'missing fourth fundamental circuit element', namely the memristor [15]. Several decades later, in 2008, researchers from Hewlett Packard (HP) Labs discovered the link between devices exhibiting resistive switching characteristics with the memristor (MR) [16]. Such memory elements (mem-elements) have since been generalized to the memcapacitor (MC) and the meminductor (MI) [17]. Despite the significant resources pooled into undertaking memristive research, their accessibility remains limited. Most demonstrations of experimental results using memristors depend upon specialized fabrication processes [18, 19], and presently available discretely packaged memristors are extremely sensitive exhibiting significant variation [20, 21], with endurance that limits their practical application to prototypical experiments [22, 23]. This motivates the need for emulators that facilitate the exploration and design space of mem-elements, until experimental usage of memristors and resistive random access memories (RRAM) are made more broadly accessible. Mem-element emulators can be subdivided into grounded and floating types. With respect to two-terminal emulators, floating mem-elements are more broad in potential applications as one

of their terminals are not constrained to being grounded. For example, a high-frequency floating memristor emulator was presented in [24], where one terminal of the emulator is connected to the voltage source, and the other terminal is connected to an amplifier in a high-frequency modulation scheme, which cannot be achieved by grounded MR emulators. In general, mem-element emulators have accelerated memristive research that can be adopted by device researchers for future on-chip integration. In the past, emulators have been used to build adjustable relaxation oscillators [25–27], digital modulation [28], adaptive learning circuits [29], chaotic systems [30–34], and neuromorphic circuits [35–37].

The potential ability of fractional-order models in simulating a more generalized range of systems than corresponding integer-order counterparts [38] has driven research in memory systems using FC, where a mathematical paradigm for describing the behavior of FOMEs was proposed in [39]. Later, researchers proposed individual FOMR emulators [40], and in [41], a FOMR is realized on the basis of a floating integer-order memristor emulator circuit. More recently, multiple types of FOMEs have been emulated within the same circuit structure, where in [43], the FOMC and FOMI emulators are proposed based on fractional-order capacitors (FOC) and integer-order memristor emulators. A limitation of these approaches are that the constructed FOMC and FOMI emulators depend on the characteristics of the memristor emulators they are originally based upon, and the circuit structure thus becomes unnecessarily complex and difficult to simplify. Generalized grounded and floating FOMEs emulators that can emulate FOMR and FOMC are proposed by using different impedance combinations in [44], but these emulators cannot implement FOMI emulation, and are limited to the functionality of FOMR and FOMC. In [45], a fractional higher-order FOMR, FOMC and FOMI emulator was implemented by using a current conveyor (CCII) and analog voltage multiplier (AVM), but these FOMEs only have one free port, which does not enable flexible usage. While all of these emulators have helped researchers to explore the characteristics and potential applications of FOMEs, they all have their own specific drawbacks. Driven by the above shortcomings, we propose a novel floating universal interface, based on which floating FOMR, FOMC and FOMI emulators can be realized, without depending on a mem-element emulator or mutator as the basis of the design. In doing so, we address the flexibility and simplicity challenges that plague fractional-order mem-element emulators.

In this paper, three types of floating FOME emulators are realized by using different impedance combinations, verified using SPICE simulations. Compared with other similar research work, the universal interface can implement three types of FOME emulators with three key benefits: 1) the use of floating terminals and thus, enhanced flexibility, 2) without added circuit complexity over prior designs. 3) simpler circuit structure for easier implementation. The structure of this paper is as follows. In Sect. 2, we provide a theoretical analysis of FOMEs. In Sect. 3, three different fractional order mem-element emulators are presented on the basis of the theoretical analysis of the second section, which leads to the proposal of a novel universal interface, which uses FOCs to

achieve fractional-order integration. In Sect. 4, we verify three different FOME emulators using both SPICE and MATLAB, with an accompanying analysis of the results obtained of the FOMR, the FOMC and the FOMI emulators. In Sect. 5 concludes the paper.

2 Theoretical analysis of FOMEs

The fundamental operator of fractional calculus ${}_mD_t^\alpha$ can be defined as [46]:

$$ {}_mD_t^\alpha = \begin{cases} \frac{d^\alpha}{dt^\alpha}, & \alpha > 0 \\ 1, & \alpha = 0 \\ \int_m^t (d\tau)^{-\alpha}, & \alpha < 0 \end{cases} \tag{1} $$

where $\alpha \in R$, and m and t are the bounds of the operation. The theoretical analysis of each of the FOMR, FOMC and FOMI circuits are presented below.

2.1 Theoretical analysis of FOMR

The constitutive relationship between q and φ of the integer-order memristive system [47] is given as follows:

$$ q = \hat{q}(\varphi), \tag{2} $$

where q and φ are the time-domain integrals of current i and voltage v.

By differentiating both sides of equation (2), the i-v relationship of MR can be expressed as:

$$ \frac{dq}{dt} = i(t) = \frac{\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G_m v(t), \tag{3} $$

where G_m is the memductance (the reciprocal of memristance).

The Taylor expansion of (2) is

$$ q = \sum_{k=1}^{\infty} g_k \varphi^k. \tag{4} $$

By substituting (4) into (3), the expression of the flux-controlled memductance [48] can be obtained:

$$ G_m(\varphi) = g_1 + \sum_{k=2}^{\infty} k g_k \varphi^{k-1}. \tag{5} $$

Introducing the fractional-order integral from equation (1), the corresponding expression of the fractional-order integral of voltage is derived:

$$\begin{aligned}\varphi_\alpha(t) = \int_{-\infty}^{t} v(t)dt^\alpha &= \int_{-\infty}^{0} v(t)dt^\alpha + \int_{0}^{t} v(t)dt^\alpha \\ &= \varphi_\alpha(0) + \int_{0}^{t} v(t)dt^\alpha \\ &= \varphi_\alpha(0) + {}_0D_t^{-\alpha} v(t) \quad (0 < \alpha < 1).\end{aligned} \tag{6}$$

Assuming the initial value of $\varphi_\alpha(t)$, $\varphi_\alpha(0) = 0$ results in:

$$\varphi_\alpha(t) = {}_0D_t^{-\alpha} v(t) = {}_0J^\alpha v(t), \tag{7}$$

where ${}_0J^\alpha v(t)$ is the fractional-order integral of voltage $v(t)$, and the notation of fractional-order integral using Riemann-Liouville's definition [49] is given by:

$$J^\alpha f(t) = \frac{1}{\Gamma(\alpha)} \int_0^t (t-\tau)^{\alpha-1} f(\tau) d\tau. \tag{8}$$

By taking $k = 2$ in equation (5), and substituting $J^\alpha v(t)$ into equation (5), one of possible equations of fractional-order memductance is derived using:

$$G_m(\varphi_\alpha) = a_1 J^\alpha v(t) + b_1. \tag{9}$$

where a_1 and b_1 are a scaling constant and the initial value of $G_m(\varphi_\alpha)$, respectively.

2.2 Theoretical analysis of FOMC

The memcapacitor model based on its constitutive relationship was proposed in [50], and the constitutive relationship between σ and φ of a memcapacitative system [47, 51] is given as:

$$\sigma = \hat{\sigma}(\varphi), \tag{10}$$

where σ and φ are the time-domain integrals of charge q and voltage v. By differentiating both sides of equation (10), the q - v relationship of MC can be obtained:

$$\frac{d\sigma}{dt} = q(t) = \frac{\hat{\sigma}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = C_m v(t), \tag{11}$$

where C_m is the memcapacitance.

The Taylor expansion of (10) is

$$\sigma = \sum_{k=1}^{\infty} r_k \varphi^k. \tag{12}$$

The memcapacitance is obtained by substituting equation (12) into equation (11):

$$C_m(\varphi) = r_1 + \sum_{k=2}^{\infty} k r_k \varphi^{k-1}. \tag{13}$$

Substituting $J^\alpha v(t)$ of equation (7) into equation (13), and setting $k = 2$ leads to one possible equation characterizing a fractional-order memcapacitance:

$$C_m(\varphi_\alpha) = a_2 J^\alpha v(t) + b_2. \tag{14}$$

where a_2 is a scaling constant and b_2 is the initial value of $C_m(\varphi_\alpha)$.

2.3 Theoretical analysis of FOMI

The constitutive relationship between q and ρ of the meminductive system [47] is given as follows:

$$q = \hat{q}(\rho), \tag{15}$$

where q and ρ are the time-domain integrals of current i and of flux φ. By differentiating both sides of (15), the i-φ relationship can be expressed as:

$$\frac{dq}{dt} = i(t) = \frac{\hat{q}(\rho)}{d\rho}\frac{d\rho}{dt} = L_m^{-1}\varphi(t), \tag{16}$$

where L_m^{-1} is the inverse meminductance. The Taylor expansion of (15) is

$$q = \sum_{k=1}^{\infty} l_k \rho^k. \tag{17}$$

By utilizing equations (16) and (17), the inverse meminductance [51] can be given as:

$$L_m^{-1}(\rho) = l_1 + \sum_{k=2}^{\infty} k l_k \rho^{k-1}. \tag{18}$$

The expression for fractional-order integral of flux is:

$$\begin{aligned} \rho_\alpha(t) = \int_{-\infty}^{t} \varphi(t) dt^\alpha &= \int_{-\infty}^{0} \varphi(t) dt^\alpha + \int_{0}^{t} \varphi(t) dt^\alpha \\ &= \rho_\alpha(0) + \int_{0}^{t} \varphi(t) dt^\alpha \\ &= \rho_\alpha(0) + {}_0D_t^{-\alpha}\varphi(t), \end{aligned} \tag{19}$$

where $\varphi(t)$ is the integer-order integral of voltage $v(t)$. Assuming the initial value of $\rho_\alpha(t)$, $\rho_\alpha(0) = 0$, leads to the following result:

$$\rho_\alpha(t) = {}_0D_t^{-\alpha}\varphi(t) = {}_0J^\alpha\varphi(t), \tag{20}$$

where ${}_0J^\alpha\varphi(t)$ is fractional-order integral of the flux $\varphi(t)$.

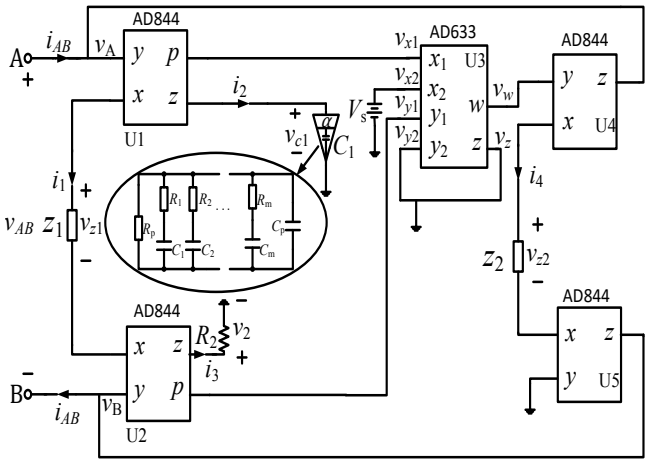

Fig. 1 Universal interface for building FOME emulators.

When the parameter k in equation (18) is set to '2', and equation (20) is substituted into equation (18), one possible equation for the fractional-order of the inverse meminductance can be given as:

$$L_m^{-1}(\rho_\alpha) = a_3 J^\alpha \varphi(t) + b_3. \tag{21}$$

where, analogous to the FOMC case, a_3 is a scaling constant and b_3 is the initial value of $L_m^{-1}(\rho_\alpha)$.

In this section, we have commenced with the theoretical analysis of integer-order mem-elements, and transitioned to FOMEs analysis.

3 Circuit design of FOME emulators based on a universal interface circuit and fractional-order capacitor

Before building FOME emulators, we first design a universal interface circuit. Following that, we will demonstrate the design of the corresponding emulators.

3.1 Design of a universal interface circuit

As shown in Fig. 1, the universal interface is made up of four current-feedback operational amplifiers AD844 (CFOAs, labeled U1, U2, U4 and U5), one voltage multiplier AD633 (U3), one resistor (R_2), two impedance elements that can be either a resistor, capacitor or inductor (Z_1 and Z_2), a DC voltage source V_s and one FOC (C_1). A and B act as floating terminals of FOME emulators based on the universal interface, enabling emulators to be connected in series with other components, and the input voltage is applied between A and B. There are an unbounded number of ways to model FOMR, FOMC and

FOMI, and different emulators can be designed by using various combinations of impedance elements to the interface terminals.

The AD844 behaves as a current conveyor and voltage follower in the universal interface circuit, where the port characteristics of AD844 can be expressed as:

$$i_x = i_z, i_y = 0, \tag{22}$$

$$v_y = v_x, v_p = v_z. \tag{23}$$

According to equations (22) and (23), the expressions of current i_1, i_2, i_3 and i_{AB} of this universal interface in the complex frequency domain are:

$$\dot{I}_1 = \dot{I}_2 = -\dot{I}_3 = \frac{\dot{V}_{AB}}{Z_1}, \tag{24a}$$

$$\dot{I}_4 = -\dot{I}_{AB} = \frac{\dot{V}_w}{Z_2} = \frac{\dot{V}_{z2}}{Z_2}, \tag{24b}$$

where $\dot{I}_1$ and $\dot{I}_2$ are the complex frequency domain current responses from terminals x and z of $U1$, respectively, $\dot{V}_{z2}$ is the complex frequency domain voltage across impedance Z_2, and $\dot{V}_w$ is the output voltage of AD633 in the complex frequency domain.

As shown in Fig. 1, the FOC C_1 is the equivalent energy-storage element adopted in proposed emulators to provide the fractional-order integral operation. Due to the commercial unavailability of a two-port FOC device on the market, Valsa proposed a helpful method for calculating comparable FOC values [52], and according to the principle of calculation, different combinations of resistance and capacitance can be calculated when the FOC takes different values. According to the analysis of the fractional-order capacitance state [53], the voltage and current flowing through FOC can be expressed as:

$$v(t) = \frac{1}{C}\int_0^t i(t)dt^\alpha \equiv \frac{1}{C}{}_0D_t^{-\alpha}i(t) \tag{25}$$

$$i(t) = C\frac{d^\alpha v(t)}{dt^\alpha} \equiv C_0D_t^\alpha v(t), \tag{26}$$

where $0 < \alpha < 1$.

According to the characteristics of FOC in equation (25), and the characteristics of AD844 in equations (22) and (23), voltage v_{c1} is transmitted to the output v_{x1} of terminal p of the AD844-U1 via an internal voltage follower. Thus, v_{x1} and v_{c1} in the complex frequency domain can be calculated by:

$$\dot{V}_{x1} = \dot{V}_{c1} = \frac{\dot{I}_2}{C_1 s^\alpha} = \frac{\dot{V}_{AB}}{C_1 Z_1 s^\alpha}, \tag{27}$$

where $\dot{V}_{AB}/s^\alpha$ shows the complex frequency domain response of $J^\alpha v_{AB}(t)$.

From equation (24a), and the combination of the characteristics of the AD844 in equations (22) and (23), the voltage of R_2 in the complex frequency domain can be described as:

$$\dot{V}_2 = \dot{V}_{y1} = \dot{I}_3 R_2 = -\dot{I}_1 R_2 = -\frac{\dot{V}_{AB}}{Z_1} R_2. \tag{28}$$

According to equations (27) and (28), and the input-to-output function of U3 (AD633), v_w in the complex frequency domain can be calculated by:

$$\dot{V}_w = -\dot{V}_{AB} \frac{R_2}{10 Z_1} \left(\frac{1}{C_1 Z_1} \frac{\dot{V}_{AB}}{s^\alpha} - V_s \right), \tag{29}$$

where V_s is an adjustable direct-current voltage.

Equations (24b) and (29) are combined to derive the relationship between the input voltage v_{AB} and the input current i_{AB} in the complex frequency domain:

$$\dot{I}_{AB} = -\dot{I}_4 = -\frac{\dot{V}_w}{Z_2} = \dot{V}_{AB} \frac{R_2}{10 Z_1 Z_2} \left(\frac{1}{C_1 Z_1} \frac{\dot{V}_{AB}}{s^\alpha} - V_s \right). \tag{30}$$

This concludes the theoretical characterization of the proposed universal interface circuit in Fig. 1. In the following sections, we present our design of the FOMR, FOMC and FOMI based on the universal interface circuit.

3.2 Design of a fractional-order memristor

When the impedance elements Z_1 and Z_2 in Fig. 1 are resistors R_1 and R_3 respectively, according to equation (30), the emulator is a FOMR. The relationship between the input voltage v_{AB} and the current i_{AB} in the time domain can be described as:

$$i_{AB} = v_{AB} \frac{R_2}{10 R_1 R_3} \left(\frac{1}{C_1 R_1} J^\alpha v_{AB}(t) - V_s \right). \tag{31}$$

The emulator is simulated as a flux-controlled FOMR. According to equations (9) and (31), the memductance $G_m(\varphi_\alpha)$ of FOMR can be expressed as:

$$G_m(\varphi_\alpha) = \frac{i_{AB}}{v_{AB}} = a_1 J^\alpha v_{AB}(t) + b_1. \tag{32}$$

From equations (31) and (32), a_1 and b_1 can be expressed as:

$$a_1 = \frac{R_2}{10 C_1 R_1^2 R_3}, \quad b_1 = -\frac{R_2}{10 R_1 R_3} V_s. \tag{33}$$

Equation (32) shows the relationship between the value of the memductance of the FOMR emulator and the fractional-order integration of the input voltage v_{AB}. Thus, the internal state of the FOMR emulator is dynamically varying in accordance with the fractional-order integration of the terminal input voltage v_{AB}.

3.3 Design of a fractional-order memcapacitor

The emulator is a FOMC when the impedance elements Z_1 and Z_2 in Fig. 1 are a resistor R_1 and a capacitor C_2. By inserting circuit parameters R_1 and C_2 into equation (30), in the complex frequency domain, the relationship between input voltage v_{AB} and the current response i_{AB} is as follows:

$$\dot{I}_{AB} = \dot{V}_{AB} \frac{R_2 s C_2}{10 R_1} \left(\frac{1}{C_1 R_1} \frac{\dot{V}_{AB}}{s^\alpha} - V_s \right). \tag{34}$$

The emulator is simulated as a flux-controlled FOMC. According to equation (34), the q-v relationship in the time domain can be written as:

$$q_{AB} = v_{AB} \frac{R_2 C_2}{10 R_1} \left(\frac{1}{C_1 R_1} J^\alpha v_{AB}(t) - V_s \right). \tag{35}$$

According to equations (14) and (35), the memcapacitance of the FOMC $C_m(\varphi_\alpha)$ can be written as:

$$C_m(\varphi_\alpha) = \frac{q_{AB}}{v_{AB}} = a_2 J^\alpha v_{AB}(t) + b_2. \tag{36}$$

From equations (35) and (36), a_2 and b_2 can be written as:

$$a_2 = \frac{C_2 R_2}{10 {R_1}^2 C_1}, \quad b_2 = -\frac{C_2 R_2}{10 R_1} V_s. \tag{37}$$

The relationship between the value of the FOMC emulator's memcapacitance and $J^\alpha v_{AB}(t)$ is shown in equation (36). From this equation, there is an explicit relationship between the internal state of the FOMC emulator and the fractional-order integration of the terminal input voltage v_{AB}.

3.4 Design of a fractional-order meminductor

The emulator is a FOMI when the impedance elements Z_1 and Z_2 in Fig. 1 are consist of an inductor L_1 and resistor R_1. By substituting L_1 and R_1 into equation (30), in the complex frequency domain, the following relationship links input voltage v_{AB} and the current response i_{AB}:

$$\dot{I}_{AB} = \dot{V}_{AB} \frac{R_2}{10 s L_1 R_1} \left(\frac{1}{C_1 L_1} \frac{\dot{V}_{AB}}{s^{\alpha+1}} - V_s \right), \tag{38}$$

where $\dot{V}_{AB}/s^{\alpha+1}$ indicates $J^\alpha \varphi_{AB}(t)$ in the complex frequency domain.

The emulator is simulated as a ρ-controlled FOMI. According to equation (38), the i-φ relationship in the time domain can be given as:

$$i_{AB} = \varphi_{AB} \frac{R_2}{10 L_1 R_1} \left(\frac{1}{C_1 L_1} J^\alpha \varphi_{AB}(t) - V_s \right). \tag{39}$$

Table 1 FOME emulators realized by different impedance combinations

Z_1	Z_2	Types of FOMEs	The expression of FOMEs
R_1	R_3	FOMR	$G_m(\varphi_\alpha) = \frac{R_2}{10R_1R_3}\left(\frac{1}{C_1R_1}J^\alpha v_{AB}(t) - V_s\right)$
R_1	C_2	FOMC	$C_m(\varphi_\alpha) = \frac{R_2C_2}{10R_1}\left(\frac{1}{C_1R_1}J^\alpha v_{AB} - V_s\right)$
L_1	R_1	FOMI	$L_m^{-1}(\rho_\alpha) = \frac{R_2}{10L_1R_1}\left(\frac{1}{C_1L_1}J^\alpha \varphi_{AB}(t) - V_s\right)$

According to equations (21) and (39), the inverse meminductance $L_m^{-1}(\rho_\alpha)$ of FOMI can be given as:

$$L_m^{-1}(\rho_\alpha) = \frac{i_{AB}}{\varphi_{AB}} = a_3 J^\alpha \varphi_{AB}(t) + b_3. \tag{40}$$

From equations (39) and (40), a_3 and b_3 can be expressed as:

$$a_3 = \frac{R_2}{10R_1{L_1}^2C_1}, \quad b_3 = -\frac{R_2}{10L_1R_1}V_s. \tag{41}$$

The relationship between the value of the FOMI emulator's meminductance and $J^\alpha\varphi_{AB}(t)$ is seen in equation (40). The equation reveals that the internal state of the FOMI emulator is affected by the fractional-order integration of the terminal flux φ_{AB}.

Table 1 lists different types of FOMEs and their corresponding expressions when Z_1 and Z_2 are selected as different impedance elements.

From the above analysis, it is clear that only the impedance elements Z_1 and Z_2 need to be changed to either resistor, capacitor or inductor to realize corresponding FOMR, FOMC and FOMI elements.

4 Circuit implementation and simulation results

In this section, we provide SPICE and MATLAB simulation results in order to verify the circuit design of the proposed fractional-order mem-element emulators in Sect. 3.

The construction of FOMR, FOMC and FOMI emulators is based on a universal interface, shown in Fig. 1, according to different impedance combinations in Table 1. As charge q and flux φ are not directly measurable, instead, they can be measured by using internal voltages in the FOME emulators as proxy variables, that are proportional to q or φ.

For the FOMR emulator, the impedance elements Z_1 and Z_2 are resistors R_1 and R_3, respectively. According to equation (27), the fractional-order integral of voltage v_{AB} is proportional to v_{c1} in the time domain, therefore, v_{c1} can be used to replace the $J^\alpha v_{AB}(t)$ equivalently. Thus, the corresponding memductance $G_m(\varphi_\alpha)$ of FOMR can be calculated according to (32) by using v_{c1}.

For the FOMC emulator, the impedance elements Z_1 and Z_2 are a resistor R_1 and capacitor C_2, respectively. The charge q_{AB} is proportional to the voltage $(-v_{C2})$ in the time domain, as can be seen from equation (24b). As a result, the voltage $(-v_{C2})$ can be substituted for q_{AB}. Based on the FOMR analysis above, the voltage v_{c1} can be used to replace the $J^{\alpha}v_{AB}(t)$ equivalently. Thus, utilizing the voltage v_{c1}, the memcapacitance $C_m(\varphi_\alpha)$ of FOMC can be determined according to equation (36).

For the FOMI emulator, the impedance elements Z_1 and Z_2 are an inductor L_1 and resistor R_1, respectively. It is known from equation (24a) that flux φ_{AB} is proportional to the current i_1 in the time domain. Therefore, flux φ_{AB} can be replaced by i_1. In addition, the equation (27) shows that the fractional-order integral of the flux φ_{AB} is directly proportional to v_{c1} in the time domain. Hence, the inverse meminductance $L_m^{-1}(\rho_\alpha)$ of the FOMI can be computed by using v_{c1} based on equation (40).

4.1 Fractional-order memristor circuit response

Here, we apply a sinusoidal waveform $v_{AB}(t) = A\sin(2\pi ft) = A\sin(\omega t)$ (V) to drive the FOMR. As the frequency f increases, the angular frequency ω increases accordingly. The emulator is a flux-controlled FOMR when Z_1 and Z_2 are R_1 and R_3, respectively. According to equation (8), the fractional-order integral of the sinusoidal waveform in the steady-state response [1] can be expressed as:

$$J^{\alpha}\left(v_{AB}(t)\right)|_{ss.} = A\omega^{-\alpha}\left(\sin\left(\omega t - \frac{\alpha\pi}{2}\right) + \sin\left(\frac{\alpha\pi}{2}\right)\right). \tag{42}$$

To explore the effect of fractional-order parameter α on the fractional-order memductance variation range, we substitute equation (42) into equation (32), where the steady-state response for memductance of the FOMR can be written as:

$$G_m(\varphi_\alpha)|_{ss.} = \frac{a_1 A}{\omega^{\alpha}}\left(\sin\left(\omega t - \frac{\alpha\pi}{2}\right) + \sin\left(\frac{\alpha\pi}{2}\right)\right) + b_1, \tag{43}$$

where A is the amplitude of the input voltage, and b_1 is the initial value of the fractional-order memductance. In addition, when A and α are constant, with an increase of the angular frequency ω, the memductance of FOMR shifts closer to its initial value b_1.

According to equation (43), the maximum value, minimum value and the variation range of the memductance of FOMR are given by the following equa-

tions under different conditions:

$$\text{when } t = \frac{\pi(1+\alpha)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$
$$G_{\max} = \frac{a_1 A}{\omega^{\alpha}}\left(\sin\left(\frac{\pi}{2}\alpha\right) + 1\right) + b_1, \tag{44a}$$
$$\text{when } t = \frac{\pi(\alpha-1)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$
$$G_{\min} = \frac{a_1 A}{\omega^{\alpha}}\left(\sin\left(\frac{\pi}{2}\alpha\right) - 1\right) + b_1, \tag{44b}$$
$$\Delta G = G_{\max} - G_{\min} = \frac{2a_1 A}{\omega^{\alpha}}, \tag{44c}$$

where Z belongs to the integer set.

Through the analysis of equations (44c), when the fractional-order α and the amplitude of the input voltage remain constant, the value of ΔG decreases with an increase of the angular frequency ω. In addition, when the amplitude A and the angular frequency ($\omega > 1$) are constant, the value of ΔG increases with the decrease of α.

In reality, the value of the fractional-order memductance must be positive, restricting the value of ω as:

$$\omega > \sqrt[\alpha]{\frac{a_1 A(1 - \sin(0.5\pi\alpha))}{b_1}}. \tag{45}$$

In our SPICE simulations (conducted in PSPICE), the power supply voltages of chips AD844 and AD633 are ±15 V. A FOC can be electronically realized with an RC (resistive-capacitive) network as shown in Fig. 2. In the simulation experiment, a Valsa constant phase element (CPE) implementation circuit with $m = 5$ stages is used to emulate the FOC. Resistor and capacitor values of the FOC for $C_1 = 18.335$ nF/sec$^{1-\alpha}$ are summarized in Table 2 for fractional orders of $\alpha = 0.95$ and $\alpha = 0.90$, and the circuit parameters are $A = 1$ V, $R_1 = 10$ kΩ, $R_2 = 100$ kΩ, $R_3 = 10$ kΩ, $V_s = -6$ V. By substituting the set of parameters into equation (33), coefficients a_1 and b_1 are calculated as 0.545 Ω^{-1} V^{-1} s$^{-\alpha}$ and 6×10^{-4} Ω^{-1}, respectively.

Fig. 3 shows the evolution of memductance over time of the FOMR across several different fractional orders. When the amplitude A and the frequency f remain constant, the smaller the fractional-order α is, the larger the variation range of the fractional-order memductance is, which is consistent with the analysis of equation (44c).

Fig. 4 shows that the pinched hysteresis loop (PHL) of the FOMR emulator passes through the first and third quadrants in the v_{AB}-i_{AB} plane. In the v_{AB}-i_{AB} plane, the slope of the PHL is equivalent to the memductance of the FOMR. When the amplitude A and the angular frequency ω (ω¿1) of the excitation signal are constant, the variation range of the slope of the PHL increases with a decrease of α. Thus, the area within the PHL lobes becomes larger as the value of the fractional-order α decreases when $\omega > 1$. Fig. 4

Table 2 Resistor and capacitor values of Valsa FOC ($C_1 = 18.335\text{nF/sec}^{1-\alpha}$) approximation circuit realizations at fractional order $\alpha = 0.95$ and $\alpha = 0.90$

Circuit element	$\alpha = 0.95$	$\alpha = 0.90$
R_1 (MΩ)	7.5350	4.8086
R_2 (MΩ)	1.3213	0.92412
R_3 (kΩ)	231.69	177.60
R_4 (kΩ)	40.628	34.131
R_5 (kΩ)	7.1242	6.5593
R_p (MΩ)	35.435	20.213
C_1 (nF)	1.3271	2.0796
C_2 (nF)	1.2109	1.7314
C_3 (nF)	1.1049	1.4415
C_4 (nF)	1.0082	1.2001
C_5 (nF)	0.91990	0.99914
C_p (nF)	9.5865	4.9678

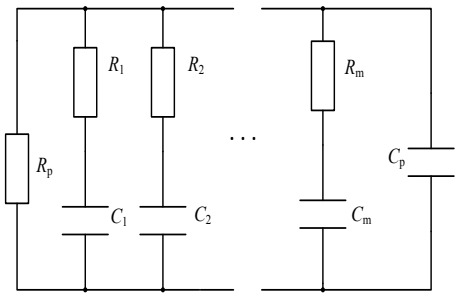

Fig. 2 m-stage Valsa CPE schematic.

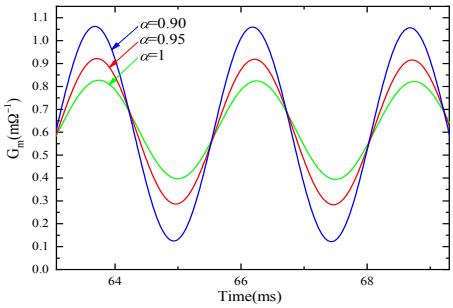

Fig. 3 SPICE simulation results of fractional-order memductance at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 1$ V, $f = 400$ Hz, $a_1 = 0.545\ \Omega^{-1}\ \text{V}^{-1}\ \text{s}^{-\alpha}$ and $b_1 = 6 \times 10^{-4}\ \Omega^{-1}$.

shows that the simulation results are consistent with the theoretical analyses of equation (44c).

Fig. 5 shows that when the order is 0.95 and the amplitude A of the excitation signal are constant, the value of ΔG decreases with the increase of frequency f. Therefore, the PHL decreases with the increase of frequency f. The simulation results in Fig. 5 are consistent with the theoretical analysis

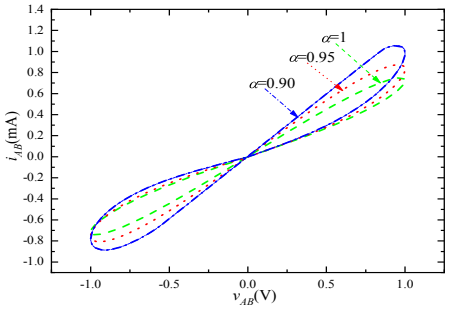

Fig. 4 SPICE simulation results of v_{AB}-i_{AB} hysteresis curves at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $f = 400$ Hz , $A = 1$ V, $a_1 = 0.545\ \Omega^{-1}\ \mathrm{V}^{-1}\ \mathrm{s}^{-\alpha}$ and $b_1 = 6 \times 10^{-4}\ \Omega^{-1}$.

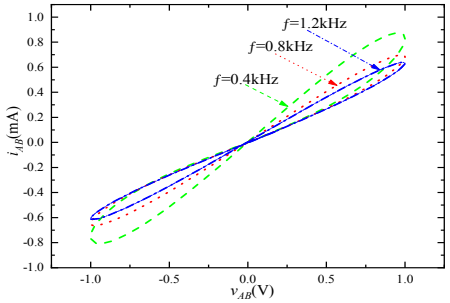

Fig. 5 PSPICE simulation results of v_{AB}-i_{AB} hysteresis curves at $f = 0.4$ kHz, $f = 0.48$ kHz and $f = 1.2$ kHz when $\alpha = 0.95$, $A = 1$ V, $a_1 = 0.545\ \Omega^{-1}\ \mathrm{V}^{-1}\ \mathrm{s}^{-\alpha}$ and $b_1 = 6 \times 10^{-4}\ \Omega^{-1}$.

of equation (44c), which proves the correctness of the FOMR emulator constructed by our novel universal interface.

To clearly express the behavioral relationship between the maximum and minimum fractional-order memductance values, and ω in equations (44a) and (44b), Fig. 6 was simulated using MATLAB. Fig. 6(a), (b) shows the change of the maximum and minimum of fractional-order memductance values with a changing applied frequency f for varying values of α. The maximum/minimum fractional-order memductance values decreases/increases as the frequency approaches infinity, respectively, towards the initial of value of the fractional-order memductance b_1, which adheres to the relations found in equations (44a) and (44b). But according to equation (44b), the minimum of the fractional-order memductance value remains unchanged with a change of the frequency when $\alpha = 1$. In other cases, the larger the value of α, the faster the decrease of the fractional-order memductance's variation range. In other words, low fractional orders can be utilized to emulate hysteresis behavior at high frequencies.

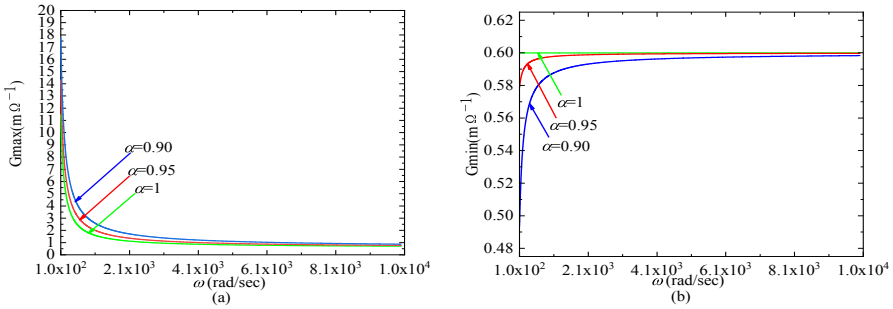

Fig. 6 MATLAB simulation results of (a) the maximum and (b) minimum of fractional-order memductance values at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$, respectively when $A = 1$ V, $a_1 = 0.545\ \Omega^{-1}\ \mathrm{V}^{-1}\ \mathrm{s}^{-\alpha}$ and $b_1 = 6 \times 10^{-4}\ \Omega^{-1}$.

4.2 Fractional-order memcapacitor circuit response

Here, we intend to use a sinusoidal wave $v_{AB}(t) = A\sin(2\pi ft) = A\sin(\omega t)$ (V) to drive the FOMC, and when the frequency f is increased, the angular frequency ω also increases. When Z_1 and Z_2 are set to R_1 and C_2, respectively, the emulator is a flux- controlled FOMC. In order to analyze the influence of the value of fractional-order α on the dynamics of the FOMC, equation (42) is substituted into the equation (36) and the memcapacitance $C_m(\varphi)$ of FOMC can be expressed by the following equation:

$$C_m(\varphi_\alpha)|_{ss.} = \frac{a_2 A}{\omega^\alpha}\left(\sin\left(\omega t - \frac{\alpha\pi}{2}\right) + \sin\left(\frac{\alpha\pi}{2}\right)\right) + b_2, \tag{46}$$

where b_2 is the initial value of the memcapacitance of FOMC. When the fractional-order α and the amplitude of the excitation signal v_{AB} are constant, the equivalent memcapacitance of the FOMC approaches b_2 with an increase of the driving frequency.

In order to explore the influence of the fractional-order α on the FOMC memcapacitance $C_m(\varphi_\alpha)$, by analyzing equation (46), the maximum value, minimum value and the variation range can be obtained:

$$\text{when } t = \frac{\pi(1+\alpha)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$

$$C_{\max} = \frac{a_2 A}{\omega^\alpha}\left(\sin\left(\frac{\pi}{2}\alpha\right) + 1\right) + b_2, , \tag{47a}$$

$$\text{when } t = \frac{\pi(\alpha-1)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$

$$C_{\min} = \frac{a_2 A}{\omega^\alpha}\left(\sin\left(\frac{\pi}{2}\alpha\right) - 1\right) + b_2, \tag{47b}$$

$$\Delta C = C_{\max} - C_{\min} = \frac{2a_2 A}{\omega^\alpha}, \tag{47c}$$

where Z belongs to the integer set.

Table 3 Resistor and capacitor values of Valsa FOC ($C_1 = 1\text{nF/sec}^{1-\alpha}$) approximation circuit realizations at fractional order $\alpha = 0.95$ and $\alpha = 0.90$

Circuit element	$\alpha = 0.95$	$\alpha = 0.90$
R_1 (MΩ)	138.16	88.167
R_2 (MΩ)	24.226	16.944
R_3 (MΩ)	4.2481	3.2563
R_4 (kΩ)	744.92	625.79
R_5 (kΩ)	130.62	120.27
R_p (MΩ)	649.71	370.61
C_1 (pF)	72.382	113.42
C_2 (pF)	66.045	94.429
C_3 (pF)	60.262	78.617
C_4 (pF)	54.986	65.453
C_5 (pF)	50.171	54.493
C_p (pF)	522.85	270.94

It can be seen from equation (47c) that ΔC is proportional to A/ω^{α}. Thus, when the value of fractional order α and the input voltage amplitude A remain constant, the value of ΔC decreases with the increase of the angular frequency ω. Furthermore, when the amplitude A and the angular frequency ω ($\omega > 1$) of the input signals are constant, a decrease in α causes ΔC to also drop.

To keep the fractional-order memcapacitance $C_m(\varphi_\alpha)$ positive, a the following condition is imposed upon the applied angular frequency:

$$\omega > \sqrt[\alpha]{\frac{a_2 A(1-\sin(0.5\pi\alpha))}{b_2}}. \tag{48}$$

A SPICE analysis is used for simulation verification. Fractional-order capacitance $C_1 = 1$ nF/sec$^{1-\alpha}$, and the corresponding values of equivalent circuit RC components for fractional orders $\alpha = 0.95$ and $\alpha = 0.90$ are shown in Table 3. The power supply voltages of chips AD844 and AD633 are ± 15 V, while circuit parameters are set to $A = 1$ V, $R_1 = 50$ kΩ, $R_2 = 100$ kΩ, $C_2 = 1$ nF and $V_s = -6$ V. Substituting these circuit parameters into equation (37), coefficients a_2 and b_2 can be calculated as 4 uFV$^{-1}s^{-\alpha}$ and 1.2 nF, respectively.

Fig. 7 shows the transient response of the fractional-order memcapacitance value changing for a given excitation voltage, across several different fractional orders. The corresponding PHLs in Fig. 8 show that the smaller the fractional order, the larger the variation range of the fractional-order memcapacitance $C_m(\varphi_\alpha)$. Equation (47c) highlights the trend of the range of the fractional-order memcapacitance $C_m(\varphi_\alpha)$ with a change of the fractional-order parameter α.

On the v_{AB}-q_{AB} plane in Fig. 8, the slope of the PHL is equivalent to the memcapacitance of the FOMC. When the excitation signal amplitude A and the angular frequency ω are both constant, the variable range of the slope of the PHL increases as the value of fractional-order α decreases. As a result, the area of the PHL lobes grow in size as the value of fractional order α drops

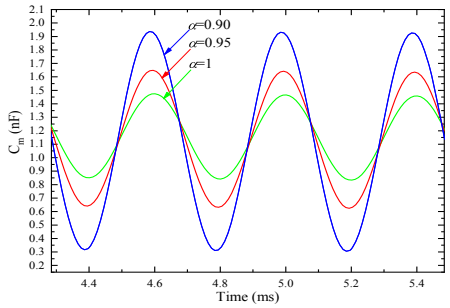

Fig. 7 SPICE simulation results of the fractional-order memcapacitance $C_m(\varphi)$ at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 1$ V, $f = 2.5$ kHz, $a_2 = 4$ uFV$^{-1}s^{-\alpha}$ and $b_2 = 1.2$ nF.

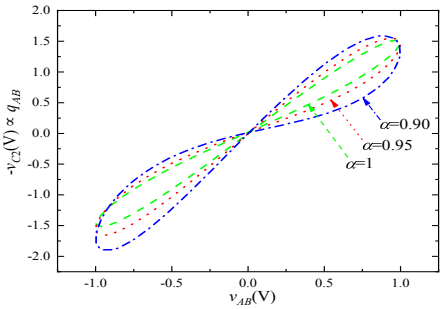

Fig. 8 PSPICE simulation results of v_{AB}-q_{AB} hysteresis curves at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 1$ V, $f = 2.5$ kHz, $a_2 = 4$ uFV$^{-1}s^{-\alpha}$ and $b_2 = 1.2$ nF.

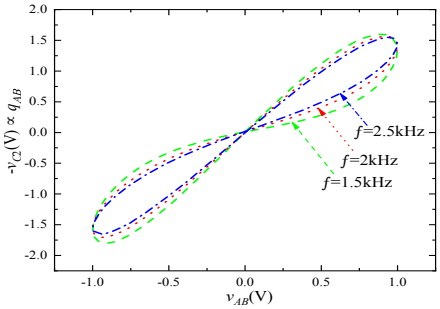

Fig. 9 PSPICE simulation results of v_{AB}-q_{AB} hysteresis curves at $f = 1.5$ kHz, $f = 2$ kHz and $f = 2.5$ kHz when $A = 1$ V, $\alpha = 0.95$, $a_2 = 4$ uFV$^{-1}s^{-\alpha}$ and $b_2 = 1.2$ nF.

when $\omega > 1$. The simulation results are consistent with the theoretical analysis of equation (47c), as seen in Fig. 8.

The slope of the PHL on the v_{AB}-q_{AB} plane is equivalent to the memcapacitance of the FOMC. When the order is 0.95 and the amplitude A of the excitation signal remains constant, the value of ΔC decreases as the frequency f increases. Thus, as the frequency f increases, the PHL shrinks. The simulation findings in Fig. 9 are consistent with the derived equation (47c).

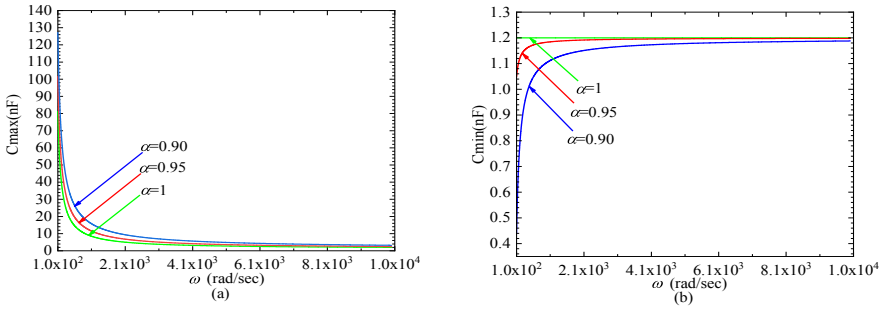

Fig. 10 MATLAB simulation results for the FOMC with $A = 1$ V, $a_2 = 4$ uFV$^{-1}s^{-\alpha}$ and $b_2 = 1.2$ nF: (a) the maximum fractional-order memcapacitance values, (b) the minimum fractional-order memcapacitance values at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$.

The maximum and minimum values of fractional-order memcapacitance are illustrated using functional simulations in MATLAB according to the equations (47a) and (47b). Fig. 10 shows that the maximum and minimum fractional-order memcapacitance values approach infinity as the excitation frequency increases, other than for the case where $\alpha = 1$ in Fig. 10(b). It can be seen from Fig. 10 that the smaller the value of order α, the slower the maximum and minimum values of fractional-order memcapacitance reach the initial memcapacitance. Therefore, in a higher frequency range, a smaller fractional-order α can better emulate the hysteresis behavior of the FOMC.

4.3 Fractional-order meminductor circuit response

In this section, we apply a cosine wave $v_{AB}(t) = A\cos(2\pi ft) = A\cos(\omega t)$ (mV) to drive the FOMI, and the angular frequency ω grows in lockstep with the increase of the frequency f. The construction of the FOMI emulator circuit is based on the universal emulator circuit. When Z_1 and Z_2 are L_1 and R_1 respectively, the emulator is a ρ - controlled FOMI. The integer integration of a cosine wave $v_{AB}(t)$ can be written as:

$$\varphi_{AB}(t) = \int v_{AB} = \frac{A}{\omega}\sin(\omega t). \tag{49}$$

According to equation (8), the fractional-order integral of the flux $\varphi_{AB}(t)$ in the steady-state response can be obtained as:

$$\begin{aligned}\rho_\alpha(t) &= J^\alpha\left(\varphi_{AB}(t)\right)\big|_{\text{ss.}} \\ &= \frac{A}{\omega^{\alpha+1}}\left(\sin\left(\omega t - \frac{\pi}{2}\alpha\right) + \sin\left(\frac{\alpha\pi}{2}\right)\right).\end{aligned} \tag{50}$$

In order to obtain the specific expression of the inverse meminductance of the FOMI, equation (50) is substituted into equation (40) to obtain:

$$L_m^{-1}(\rho_\alpha)\big|_{ss.} = \frac{a_3 A}{\omega^{\alpha+1}}\left(\sin\left(\omega t - \frac{\pi}{2}\alpha\right) + \sin\left(\frac{\alpha\pi}{2}\right)\right) + b_3. \tag{51}$$

From equation (51), when the fractional order α and the amplitude A of the excitation signal are constant, the inverse fractional-order meminductance will become infinitely close to the initial value b_3 with an increase of the angular frequency ω. Therefore, the PHL of the FOMI will approach a straight line in the limit of an increasing frequency f.

According to equation (51), the maximum, minimum and variation range of the inverse meminductance of FOMI are given by:

$$\text{when } t = \frac{\pi(1+\alpha)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$
$$L^{-1}_{\max} = \frac{a_3 A}{\omega^{\alpha+1}}\left(\sin\left(\frac{\pi}{2}\alpha\right) + 1\right) + b_3, \tag{52a}$$
$$\text{when } t = \frac{\pi(\alpha-1)}{2\omega} + \frac{2k\pi}{\omega}(k \in Z),$$
$$L^{-1}{}_{\min} = \frac{a_3 A}{\omega^{\alpha+1}}\left(\sin\left(\frac{\pi}{2}\alpha\right) - 1\right) + b_3, \tag{52b}$$
$$\Delta L^{-1} = L^{-1}{}_{\max} - L^{-1}{}_{\min} = \frac{2a_3 A}{\omega^{\alpha+1}}, \tag{52c}$$

where Z belongs to the integer set.

By observing equation (52c), when the amplitude A of the input voltage and the value of fractional order α are fixed, the value of ΔL^{-1} decreases as the angular frequency ω increases. Besides, the value of ΔL^{-1} increases as the value of fractional order α decreases when the amplitude A and the angular frequency ω are unchanged.

In order to make the inverse fractional-order meminductance positive, the following condition must be satisfied:

$$\omega > \sqrt[\alpha+1]{\frac{a_3 A(1-\sin(0.5\pi\alpha))}{b_3}}. \tag{53}$$

In order to verify the correctness of the above theoretical analysis, SPICE is used to simulate the analog circuit. Fractional-order capacitance $C_1 = 1$ nF/sec$^{1-\alpha}$, and the corresponding value of the equivalent circuit of resistors and capacitors is shown in Table 3. The power supply voltages of chips AD844 and AD633 are ± 15 V, and other corresponding circuit parameters are $A = 5$ mV, $L_1 = 1$ mH, $R_1 = 50$ kΩ, $R_2 = 10$ kΩ and $V_s = -12$ V. By substituting these given parameters into equation (41), $a_3 = 2 \times 10^{13}$ H^{-1} Wb^{-1} s$^{-\alpha}$ and $b_3 = 240$ H^{-1} can be obtained.

Through the comparison of different orders in Fig. 11, it can be seen that under the same frequency f and amplitude A of the excitation signal, the variation range of the inverse fractional order meminduction will increase with a decrease of fractional order. This result is consistent with the theoretical analysis of equation (52c).

From the $\varphi_{AB} - i_{AB}$ plane in Fig. 12, the slope is equivalent to the inverse meminductance of the FOMI. When the excitation signal amplitude A and angular frequency ω are both constant, the variable range of the slope of the

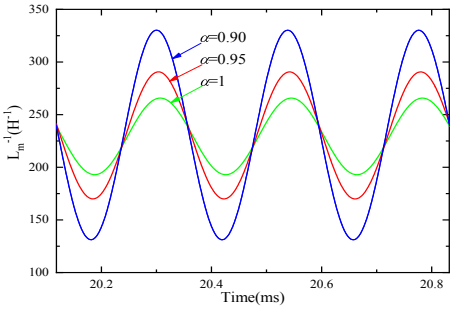

Fig. 11 PSPICE simulation results waveforms of the inverse fractional-order meminductance at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 5$ mV, $f = 4.2$ kHz, $a_3 = 2 \times 10^{13}$ H^{-1} Wb^{-1} $\mathrm{s}^{-\alpha}$ and $b_3 = 240$ H^{-1}.

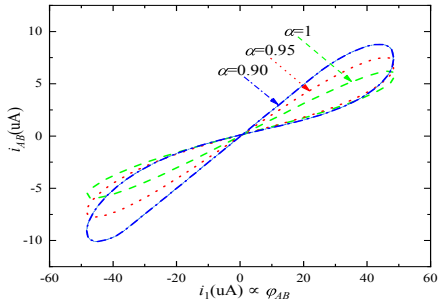

Fig. 12 PSPICE simulation results of $\varphi_{AB} - i_{AB}$ hysteresis curves of FOMI at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 5$ mV, $f = 4.2$ kHz, $a_3 = 2 \times 10^{13}$ H^{-1} Wb^{-1} $\mathrm{s}^{-\alpha}$ and $b_3 = 240$ H^{-1}.

PHL increases as the value of the fractional-order α decreases. Hence, as the fractional-order α declines and $\omega > 1$, the area within the PHL lobe increases. As shown in Fig. 12, the simulation findings are consistent with the theoretical analysis of equation (52c).

On the $\varphi_{AB} - i_{AB}$ plane in Fig. 13, the slope of the PHL is equivalent to the inverse meminductance of the FOMI. From equation (49), the flux $\varphi_{AB}(t)$ is proportional to A/ω. Therefore, the amplitude of the flux $\varphi_{AB}(t)$ decreases with an increase of the frequency f when the amplitude A of the input signal is constant. In addition, when $A = 5$ mV and $\alpha = 0.95$, the value of ΔL^{-1} decreases with an increasing frequency f. As a consequence, this fact causes the PHL of FOMI to shrink inward as the frequency increases. Furthermore, the theoretical analysis of equation (52c) also well illustrates the influence of the frequency f on the variation range of the slope of the PHL in Fig. 13.

In order to intuitively express equations (52a) and (52b), Fig. 14 was illustrated using MATLAB. The maximum and the minimum values of the inverse fractional-order meminductance are infinitely close to the initial value b_3 as the frequency increases, shown in Fig. 14. In Fig. 14, the maximum and the minimum value of the inverse fractional-order meminductance will reach the

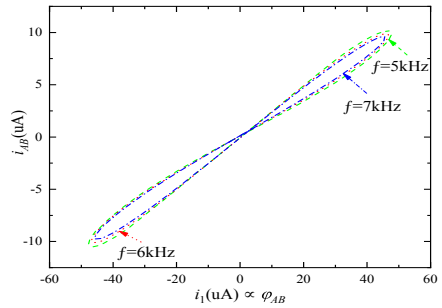

Fig. 13 SPICE simulation results of $\varphi_{AB} - i_{AB}$ hysteresis curves at $f = 5$ kHz, $f = 6$ kHz and $f = 7$ kHz when $A = 5$ mV, $\alpha = 0.95$, $a_3 = 2 \times 10^{13}$ H^{-1} Wb^{-1} $\mathrm{s}^{-\alpha}$ and $b_3 = 240$ H^{-1}.

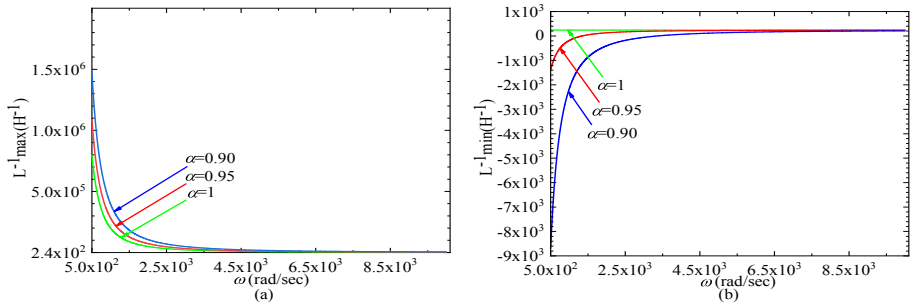

Fig. 14 MATLAB simulation results of (a) the maximum value of the inverse fractional-order meminductance, (b) the minimum value of the inverse fractional-order meminductance at $\alpha = 0.90$, $\alpha = 0.95$ and $\alpha = 1$ when $A = 5$ mV, $a_3 = 2 \times 10^{13}$ H^{-1} Wb^{-1} $\mathrm{s}^{-\alpha}$ and $b_3 = 240$ H^{-1}.

Table 4 Comparison of different emulators of the FOMEs

	Reference	Number of active elements	Number of passive elements excluding FOC	Type of mutator/emulator
Floating emulator	[41]	5(AD844×5)	3(R×3)	FOMR
	[42]	8(AD844×5, AD633×3)	8(R×8)	FOMR
	[44]	6(CCII×5, multiplier×1	4(R×4)	FOMR
			4(R×3, C×1)	FOMC
	proposed	5(AD844×4, AD633×1)	3(R×3)	FOMR
			3(R×2, C×1)	FOMC
			3(R×2, L×1)	FOMI

initial value faster by increasing the fractional order α. In particular, for $\alpha = 1$, the value of $L^{-1}{}_{\min}$ is constant. Therefore, the lower the value of order α, the more evident the PHL behavior of FOMI is at the same frequency.

To summarize, these simulation results have shown consistency with the theoretical analysis, which effectively proves that the proposed novel universal interface for constructing floating fractional order mem-elements is valid.

Table 4 provides comparisons among the proposed FOME based on a universal interface and prior floating FOME emulators, in the aspects of a) the

number of active elements, b) the number of passive elements excluding FOC and c) the ability to realize different types of FOMEs. These several aspects of the comparison are crucial, because the fewer number of active and passive elements, the simpler the structures of FOME emulators will have; and the more types of FOMEs for implementation, the broader application prospects the FOME emulators should have. As for the number of active and passive elements, the proposed FOME emulators based on a universal interface obviously possess fewer active elements and passive elements excluding FOC, ensuring circuits structures of the proposed FOME emulators simpler and easier to implement. Regarding the ability to realize different types of FOMEs, only single FOMR emulators are proposed in [41] and [42]. In addition, FOMI emulator cannot be realized in [44]. However, the proposed FOME emulators have the ability to flexibly realize three types of FOMEs, which is more functional. Therefore, the proposed FOME emulators provide a new idea for the realization of simple and useful FOME emulators in the future.

5 Conclusion

This paper presented a novel universal interface circuit. The emulators of FOMR, FOMC and FOMI may be realized when Z_1 and Z_2 are selected using different impedance elements. Theoretical analyses are undertaken to verify the operation of these designed FOME emulators. SPICE simulations are undertaken in PSPICE to perform circuit analyses, and MATLAB simulations are used for dynamical analyses, presenting the influence of fractional-order parameters and excitation frequencies on the PHL of the FOME emulators, as well as the range of the fractional-order memductance, the fractional-order memcapacitance and the inverse fractional-order meminductance. From the consistency between our theoretical analyses and simulation results, we can see that the fractional-order parameter provides an extra degree of freedom and increases the controllability on memory-based systems. The newly proposed floating universal interface will facilitate further FOMR, FOMC and FOMI-based research by providing a method to emulate three types of FOMEs. Compared with other similar research work, the FOME emulators based on the proposed universal interface in this paper have the following advantages: 1) have floating terminals; 2) have reconfigurability among the three types of FOMEs that are not based on any other mem-emulators; 3) simpler circuit structure. Our proposed interface provides value for the future research, development and application of FOMEs.

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Statements and Declarations

Funding This work was supported by the Young Scientists Fund of the National Natural Science Foundation of China Grant (No. 62101142); the Guangzhou Science and Technology Plan Research Project under Grant (No. 202102020874); and the Featured Innovation Foundation of the Education Department of Guangdong Province under Grant (Nos. 2021KTSCX062, 2021ZDZX1079).

Conflict of interest The authors declare that there are no conflict of interests regarding the publication of this paper.

Data availability All date generated or analyzed during this study are included in this published article.