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Article

Keywords: Van der Waals (vdW), Negative Differential Transconductance (NDT)

Posted Date: November 20th, 2020

DOI: https://doi.org/10.21203/rs.3.rs-108643/v1

Tunable Intermediate-Logic Ternary Circuits based on $MoSe_2$-WSe_2 Heterojunction

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Abstract

Van der Waals (vdW) heterojunctions, which consist of p-type and n-type semiconductors, have provided new features for transition metal dichalcogenides (TMDs). In this work, a negative differential transconductance (NDT) transistor based on a $MoSe_2$-WSe_2 heterojunction ($MoSe_2$-WSe_2 H-TR) is proposed. The $MoSe_2$-WSe_2 H-TR provides desirable device characteristics for ternary circuit operation with a switching behavior of off-state / p-type turn-on / NDT region / p-type turn-on. As a result, a 100% output voltage (V_{OUT}) swing inverter can be achieved in a ternary inverter, which consists of the proposed $MoSe_2$-WSe_2 vdW-H-TR and a MoS_2 floating-gate transistor. Furthermore, a tunable intermediate-logic ternary circuit operation is demonstrated by controlling the threshold voltage (V_{TH}) in a pull-down n-type MoS_2 floating-gate transistor. We also investigated that a light-induced operation on the $MoSe_2$-WSe_2 vdW-H-TR offers control of the V_{OUT} amplitude at the intermediate-logic state. Based on the proposed $MoSe_2$-WSe_2 vdW-H-TR, this work suggests a strategy to obtain a tunable ternary circuit, thus providing a new concept of heterojunction electronics using layered TMDs.

Introduction

Two-dimensional (2D) materials, especially Transition metal dichalcogenides (TMDs) have recently attracted attention due to their great potential in various applications such as field-effect transistors and optoelectronics.[1–10] In addition to their intrinsic properties of the TMDs,[11–14] van der Waals heterostructures (vdW-H), which are constructed by stacking different TMDs materials, have also attracted significant attention in recent years. The ability to form different TMDs material combinations (*e.g.*, MoS_2-WS_2,[15] MoS_2-WSe_2,[16] MoS_2-$MoTe_2$,[17] and MoS_2-BP[18]) offers the possibility of achieving new electronic characteristics. One of the emerging electronic functions arising from the vdW-H is a new switching behavior, which includes negative differential resistance (NDR) or negative differential transconductance (NDT) characteristics.[19–21]

This new switching characteristic does not behave monotonically, i.e., the current does not continuously increase as the applied voltage increases. There is NDT regions, where the current decreases when the applied voltage is in the middle of its range. Due to this unique switching behavior, a new circuit scheme for ternary logic has been proposed. In the complementary circuit consisting of two serially connected transistors, where one transistor is a vdW-H transistor with NDT, the charging pull-up transistor has a comparable resistance region with the discharging pull-down transistor.[22,23] As a result, the vdW-H-based circuit offers an additional output voltage (V_{OUT}) state at which both transistors have a comparable resistance. Thus, ternary logic operation can be achieved. As the ternary circuit has an extra logic state, more efficient logic computing is potentially provided.

However, the transition from binary to ternary logic circuit results in the reduction of the circuit's noise margin. Specifically, the maximum noise margin of a ternary logic circuit is 33% of the V_{DD} (V_{DD} is divided by three logic states), while the maximum noise margin of a binary logic circuit is 50% of the V_{DD} (V_{DD} is divided by two logic states).[24] As a result, it is

very important to accurately control each logic state margin circuit as the number of logic level states increases. However, previously reported vdW-H-based ternary circuits include: (1) incomplete output voltage swing[25–27] and (2) narrow margin for the intermediate-logic state.[28–30] These issues must be addressed to make the ternary circuit suitable to practical applications. Therefore, it is necessary to investigate how to implement vdW-H-based logic more systematically.

Here, we report a new combination of $MoSe_2$-WSe_2 vdW-H, providing desirable electrical properties for ternary circuit operation. As $MoSe_2$ and WSe_2 have n-type dominant and p-type dominant ambipolar charge transport characteristics, respectively, the $MoSe_2$-WSe_2 vdW-H provides desirable switching behavior as follows: off-state / p-type turn-on / NDT region / p-type turn-on. Using a $MoSe_2$-WSe_2 vdW-H, a 100% swing ternary inverter circuit with tunable intermediate-logic state combined with MoS_2 flash memory is demonstrated. The proposed ternary inverter enables its intermediate-logic state to be adjustable by controlling V_{TH} of the pull-down MoS_2 floating-gate transistor. Furthermore, the intermediate V_{OUT} state can be controlled by light irradiation to the $MoSe_2$-WSe_2 vdW-H in the ternary inverter. As the excess current generated by the light irradiation increases I_D in the NDT region, the intermediate V_{OUT} state is enhanced. Through this study, it is noted that the state and margin of the V_{OUT} state can be adjusted. This opens up new opportunities for a new concept TMDs-based vdW-H electronics.

Results and Discussion

First, the $MoSe_2$-WSe_2 vdW-H was fabricated using a polydimethylsiloxane (PDMS) stamp method.[31] WSe_2 was deposited on the top of $MoSe_2$ to form a partial overlap in the middle of the channel between the source and drain electrode. As a result, the one contact electrode makes contact with the $MoSe_2$ only, while the other contact electrode makes contact with the WSe_2 only (Figure 1a and 1b). Details of the $MoSe_2$-WSe_2 vdW-H fabrication steps are given in the Experimental Section.

To investigate the chemical and morphological structure of the fabricated $MoSe_2$-WSe_2 vdW-H, a comprehensive analysis including and scanning electron microscopy (SEM), Raman spectroscopy, X-ray photoelectron spectroscopy (XPS), and atomic force microscopy (AFM) was performed. Figure 1c shows the SEM and EDS mapping images of the $MoSe_2$-WSe_2 vdW-H, indicating the coexistence of $MoSe_2$ and WSe_2 region. The measured Raman spectra show the peaks of WSe_2 (Red curve) at 246.3 and 253.8 cm^{-1} and the peak of $MoSe_2$ (blue curve) at 239.9 cm^{-1}.[32–34] The details of the Raman spectroscopy are explained in the Supporting Information (Figure S1). The coexistence of $MoSe_2$ and WSe_2 is also supported by the binding energy peaks of Mo 3d, W 4f, and Se 3d in the measured X-ray photoelectron spectroscopy (XPS) spectra (Figure S2).[35–37] The measured AFM shows the $MoSe_2$-WSe_2 vdW-H formation structure in the middle of the transistor channel region (Figure S3).

We investigated the electrical characteristics of the fabricated $MoSe_2$-WSe_2 vdW-H-TR. We prepared a baseline $MoSe_2$ and WSe_2 transistors were prepared as baseline n-type and p-type devices, respectively (Figure S4). The measured transfer characteristics of the baseline $MoSe_2$ transistor exhibit n-type dominant ambipolar characteristics with an effective electron and effective hole mobility (Figure 1d and Table S1). In contrast, the baseline WSe_2 transistor exhibits p-type dominant ambipolar characteristics with an effective electron and effective hole mobility (Figure 1d and Table S1). These n-type dominant and p-type dominant ambipolar

characteristics are also supported by the measured output curves, which exhibit a linear current increase due to counterflow (*i.e.*, hole current in the n-type operation and electron current in the p-type operation) (Figure S5 and S6). A total of 40 baseline transistors were fabricated to confirm the uniformity and reliability of the $MoSe_2$ transistor exhibiting n-type dominant ambipolar characteristics and the WSe_2 transistor exhibiting p-type dominant ambipolar characteristics. The 20 baseline $MoSe_2$ and 20 baseline WSe_2 transistors were fabricated with a similar thickness to the sample used for $MoSe_2$-WSe_2 vdW-H-TR, and their electrical properties (V_{TH}, I_{ON}, and I_{OFF}) were observed similarly for the most of them (Figure S7-S9).

Based on the baseline $MoSe_2$ and WSe_2 transistors, the $MoSe_2$-WSe_2 vdW-H-TR was characterized. It was observed that the device does not switch on monotonically as a function of the applied gate voltage bias (V_G). Instead, the device exhibits an abnormal switching behavior as follows: off-state / p-type turn-on / NDT region / p-type turn-on (Figure 1e). Similar behaviors are also observed in the other $MoSe_2$-WSe_2 vdW-H-TRs (Figure S10). In the V_G = 40 V to −7 V range, the WSe_2 p-channel begins to accumulate hole carriers, contributing to I_D increase. In about the middle of the range (V_G = −7 V), both $MoSe_2$ and WSe_2 accumulate hole and electron carriers, contributing to I_D increase. Accordingly, the peak of I_D (the highest I_D value) was observed in this voltage range. In the −47 V < V_G < −7 V range, I_D decreases, since the $MoSe_2$ *n*-channel becomes depleted by the applied negative bias V_G. As the negative V_G increases further, the turn-on of the $MoSe_2$ *p*-channel contributes to I_D increase due to the ambipolar characteristics of the $MoSe_2$. It is worth noting that I_D increases again, when further negative bias is applied (V_G < −47 V). This is because the $MoSe_2$ contributes to electron carrier accumulation due to its ambipolar charge transport properties (Figure 1d, Figure S5). It can be observed that the decrease of I_D (NDT) depends on the applied drain voltage bias (V_D) (Figure 1e and 1f). More negative V_D (*e.g.*, V_D = −40 V) results in a larger electron accumulation in the $MoSe_2$ region of the drain node. Thus, the peak current I_D increases by 9.2 times to 78 μA, the

NDT voltage range widens by 2.1 times to 45 V, and the maximum NDT value increases by 6 times to −1.27 S at V_D = −40 V compared to the baseline values at V_D = −10 V (Figure 1g–i). It is emphasized that the maximum NDT and voltage range values obtained in the $MoSe_2$-WSe_2 vdW-H-TR are larger than in previously reported TMDs-based heterojunction transistors (Table S2).

Next, the ternary circuit was characterized using the proposed $MoSe_2$-WSe_2 vdW-H-TR. The proposed inverter circuit consists of the $MoSe_2$-WSe_2 vdW-H-TR and n-type MoS_2 floating-gate transistor in series (Figure 2a and 2b). The inverter circuit was fabricated by externally connecting the two transistors in different substrates. Details of the floating-gate transistor fabrication process and circuit measurement are given in Experimental Section. Unlike previously reported ternary inverters,[23,26,38,39] the floating-gate transistor is used as a pull-down transistor in this work. The MoS_2 transistor without the floating-gate layer was showed no hysteresis in the transfer characteristics curve (Figure S11). However, the MoS_2 floating-gate transistor was observed a memory window due to the charge traps in the floating gate.[40,41] As shown in Figure 2c, a memory window was originated from a large amount of charge stored in the PEDOT:PSS charge trap layer. When V_{Erase} is swept toward a positive bias, the electron carriers enter the PEDOT: PSS floating-gate through the TDL Al_2O_3 layer by the mechanism of Fowler-Nordheim tunneling (FNT)[42] and trap-assisted tunneling (TAT)[43], resulting in a positive shift of V_{TH}. However, when $V_{Program}$ is swept from the positive to the negative direction, the trapped electrons pass through the energy barrier inside the floating gate, causing a negative shift of V_{TH}. Since the MoS_2 floating-gate transistor provides a controllable threshold voltage (V_{TH}), which depends on the applied programming/erasing voltage bias, tunable inverter characteristics can be obtained. The fabricated MoS_2 floating-gate transistor exhibits a shift of V_{TH} from −20 V to −47 V depending on the applied erasing voltage bias

(V_{Erase} = −20, −30, −40, −50 V) (Figure 2c and 2d). Details of the MoS_2 floating-gate transistor fabrication process and structure are given in Figure S12.

Depending on the programmed/erased states ($V_{Programmed}$ = 30 V, V_{Erase} = −20 V), the proposed inverter exhibits a transition from binary switching to ternary switching (Figure 2e and 2f). When V_{TH} shifts toward positive values (after $V_{Programmed}$ = 30 V), there is no region where pull-up and pull-down resistances can be matched as shown in Figure S13. However, as V_{TH} shifts toward negative values, the inverter has an intermediate-logic state, where the pull-up and pull-down resistances are matched, resulting in three distinct V_{OUT} states: Logic 1 at V_{OUT} = 20 V, Logic 0.5 at V_{OUT} = 3 V, Logic 0 at V_{OUT} = 0 V. We emphasize that the proposed inverter combining with the V_{TH}-controllable floating-gate transistor enables its circuit operation to have binary and ternary logic behavior selectively. While few previous reports control the state of the pull-up transistor though V_{DD} or light irradiation to convert from binary to ternary,[18, 24, 26, 44-46] we believe that this is the first demonstration of selective circuit operation between binary and ternary logic by using the state of the pull-down n-type MoS_2 floating gate transistor.

The proposed inverter exhibits a stable operation with the appropriate ternary logic states (V_{OUT} = 20, 5, and 0 V) in the three-input pulsed measurement (V_{IN} = 20, 0, and −20 V) for V_{DD} = 20 V (Figure 2g and 2h). V_{IN}-V_{OUT} transfer characteristics were also measured for different V_{DD} values (V_{DD} = 10, 20, 30, 40, and 50 V). The measured V_{OUT} value at the intermediate-logic state increases from 0.6 to 6.7 V as the applied V_{DD} (Figure 2i and 2j) increases. It must be emphasized that the proposed inverter exhibits 100% V_{OUT} swing with V_{DD}-to-*GND* (Figure 2k). Since the proposed $MoSe_2$-WSe_2 vdW-H-TR has a well-defined on-state (as shown in Figure 1d), the inverter performs a full pull-up operation, providing 100% V_{OUT} swing. Furthermore, it is demonstrated that the intermediate-logic region can be controlled by controlling the V_{TH} shift in the MoS_2 floating-gate transistor. When a larger V_{Erase}

is applied, V_{TH} shifts to negative values. Therefore, the inverter has a wider region where the pull-up and pull-down resistances are matched (*i,e.*, the intermediate-logic voltage region). As shown in Figure 2l and 2m, the intermediate-logic voltage region increases by 1.7 times from 19 V to 33 V as the applied V_{Erase} decreases from −25 V to −50 V.

We investigated optoelectronic properties of the $MoSe_2$-WSe_2 vdW-H. As a pre-step, the transfer characteristics of the baseline $MoSe_2$ and WSe_2 transistors as well as the $MoSe_2$-WSe_2 vdW-H under light illumination and V_D = −20 V (Figure 3a-3c) were measured. These characteristics were measured as a function of the applied V_G at a fixed excitation wavelength (λ_{ex}) of 638 nm for different incident power densities (P_{inc}). In the measurement of the baseline $MoSe_2$ and WSe_2 transistors, an I_D increase was observed due to photocurrent generation as the applied P_{inc} increased. Furthermore, we extracted a photosensitivity, which is defined by the ratio of the photocurrent to dark current ($S_{ph} = \frac{I_{ph}}{I_{dark}}$) (signal-to-noise ratio).[47–49] Figures 3d and 3e show the S_{ph} of the baseline WSe_2 transistor and baseline $MoSe_2$ transistor, indicating a peak value S_{ph} at the off-state region in both of the WSe_2 and $MoSe_2$ transistors. In the $MoSe_2$-WSe_2 vdW-H-TR, the two peaks of S_{ph} were obtained (Figure 3f), resulting from a superposition form of photosensitivity peaks of the baseline $MoSe_2$ and WSe_2 transistors. Although the S_{ph} of $MoSe_2$-WSe_2 vdW-H-TR is similar to the superposition form of the S_{ph} of the baseline device, the sensitivity values are different because the dark currents (i.e., noise) of $MoSe_2$-WSe_2 vdW-H-TR and baseline devices are different.

In the NDT region, I_D increases as the applied P_{inc} increases. This is shown in the plots of I_{peak} and I_{valley}, which depend on the illumination P_{inc} (Figure 3g and 3h). In the NDT region, an enhancement in I_D under illumination was observed. The NDT results from the depletion of the $MoSe_2$ channel (as described in Figure 1) and the photocurrent generation in the $MoSe_2$ by the light illumination lead to an increase in I_D in this region of the NDT. The peak-to-valley

ratio and maximum negative g_m decrease as the applied P_{inc} increases. This is due to the increase in I_D in the NDT region by light illumination (Figure 3i and 3j). Additional measurements and their analysis of the photoresponsive WSe_2, $MoSe_2$, $MoSe_2$-WSe_2 vdW-H-TR are given in Figure S14-S16. Figure S14a and S14b shows the transfer curves of baseline WSe_2 and $MoSe_2$ transistors under illumination light. These characteristics were measured under the same conditions in Figure 3a and 3b except for V_D of -1 V, which are performed to compare photoresponsive behaviors of the baseline devices depending on V_D of -1 V and -20 V. Figure S14c, S14d, and Figure S15a, S15b show the extracted photoresponsivity (R_{ph}) of the baseline WSe_2 and $MoSe_2$ transistors as a function of V_G under V_D of -1 V and -20 V, respectively. R_{ph} can be calculated using the following equation:

$$R_{ph} = \frac{I_{ph}}{P_{inc} \times A_{ch}} \quad [AW^{-1}]$$

Where, I_{ph} is the photocurrent ($I_{ph} = I_{total} - I_{dark}$) and A_{ch} is the channel area of the device.[50] A maximum R_{ph} of 366 AW^{-1} was obtained for the $MoSe_2$ transistor, which is 3 times larger than the R_{ph} of the WSe_2 transistor for P_{inc} = 0.4 mW cm^{-2}. This indicates that the $MoSe_2$ transistor exhibits more light absorption and photocurrent generation than those of the WSe_2 transistor.

The optoelectronic properties of the proposed $MoSe_2$-WSe_2 vdW-H-TR (Figure S15c) were also characterized. The transfer characteristics of the $MoSe_2$-WSe_2 vdW-H-TR under illumination light at a fixed excitation wavelength (λ_{ex}) of 638 nm and V_D = −20 V were measured. These are the same measurement conditions as those applied in the baseline WSe_2 and $MoSe_2$ transistors characterizations. It was observed that a maximum R_{ph} of 40 AW^{-1} was obtained in the middle of the V_G range (V_G = −20 V). R_{ph} of $MoSe_2$-WSe_2 vdW-H transistor shows the two peaks at V_G = -47 V and -24 V. It is indicated that the R_{ph} peaks of $MoSe_2$-WSe_2 are formed by superposition of R_{ph} of WSe_2 and $MoSe_2$ transistors. The R_{ph} peak at V_G = -47 V is lower than the R_{ph} peak at V_G = -24 V due to the R_{ph} of WSe_2 lower than that of $MoSe_2$. When V_G is V_G < -47 V, the R_{ph} of $MoSe_2$-WSe_2 vdW-H transistor gradually decreased because R_{ph}

of $MoSe_2$ in heterostructure converge to zero. Also, under -24 V < V_G, the R_{ph} of $MoSe_2$-WSe_2 vdW-H transistor gradually decreased because R_{ph} of WSe_2 in heterostructure converge to zero. Further details of the photoresponsivity properties are given in Figure S16a. The specitic detectivity (D^*), such as R_{ph}, is the most representative figures of merit for the evaluation of the optical properties of semiconducting materials, D^* can be calculated using the following equation: $D^* = \frac{\sqrt{A \times \Delta f}}{NEP} = \frac{R_{ph}\sqrt{A}}{S_n}$ (A: area, Δf: bandwidth, NEP: noise equivalent power, Sn: noise spectral density). The calculated D^* of the WSe_2, $MoSe_2$, and $MoSe_2$-WSe_2 vdW-H-TR is shown in Figure S16b, which clearly indicates that the $MoSe_2$-WSe_2 vdW-H-TR exhibits the highest value. This is because it is comparable regardless of the area of the devices.[51] Moreover, the higher D^* of the $MoSe_2$ transistor than that of the WSe_2 transistor demonstrates again that the $MoSe_2$ transistor exhibits superior optical properties than the WSe_2 transistor.

The I_D increase in the NDT region by the observed photoelectric effect allowed the implementation of a controllable intermediate-logic V_{OUT} ternary inverter based on the $MoSe_2$-WSe_2 vdW-H-TR and the MoS_2 floating-gate transistors. The ternary inverter was measured by illuminating the $MoSe_2$-WSe_2 vdW-H-TR at λ_{ex} = 638 nm (Figure 4a). Figure 4b shows the V_{OUT}-V_{IN} characteristics of the ternary inverter with and without illumination light. The illuminated vdW-H pull-up transistor leads to a V_{OUT} increase in the intermediate-logic of the ternary circuit. In the three-V_{IN} pulsed measurements, the inverter showed that the intermediate-logic V_{OUT} increases by 1.5 times to 7.2 V from 4.8 V as the illumination P_{inc} increases (Figure 4c). In the NDT region, which determines the V_{OUT} value of the intermediate-logic, the resistance ratio between the illuminated vdW-H pull-up transistor and the pull-down floating-gate transistor can be adjusted according to the illumination P_{inc}. This results in the V_{OUT} variation of the intermediate-logic state.In summary, we proposed a P-memory that combines a layered MoS_2 thin-film transistor structure with a PEDOT:PSS floating gate. Owing to the

virtues of the MoS_2 and PEDOT:PSS combined structure, the P-memory exhibited high performance including a high switching current ratio > 10^7, large memory window > 50 V, excellent endurance > 1,000 cycles, and long retention time > 2,000 s. These were confirmed by multiple device fabrications and characterizations to evaluate their reproducibility and uniformity (>30 devices). We also proposed a new performance metric, the photo programming responsivity, representing the amount of storage of optical information, which is determined by the light intensity exposed during the programming operation. We also achieved a photo-activated memory operation that combines photodiode and memory functions. Depending on whether the light was illuminated, the P-memory provided a different degree of programming, and thus the degree of light exposure could be stored directly in the device. Furthermore, we demonstrated a flexible P-memory by manufacturing the device on a flexible PI substrate. This indicated that the device maintained its multifunctional memory behaviors even after the 1,000 bending cycles. Through comprehensive experiments, this study showed not only the memory characteristics of the conventional floating-gate-based flash memory but also new versatility such as mechanical flexibility and photoactive memory behaviors. These reported results are expected to be useful guidelines in the development of new electronic device features using new nanomaterials.

In summary, tunable intermediate-logic ternary circuits based on the $MoSe_2$-WSe_2 vdW-H were demonstrated. By combining the illuminated $MoSe_2$-WSe_2 vdW-H as the pull-up device and the MoS_2 flash memory as the pull-down device, tunable intermediate-logic ternary circuits were implemented for the first time. Specifically: (1) a tunable intermediate-logic V_{OUT} region and (2) a tunable intermediate-logic V_{OUT} amplitude were achieved. To the best of our knowledge, this is the first demonstration of the intermediate-logic tunability in both voltage region and amplitude (Table S3). In the transition from the conventional binary to multi-state circuit, the accurate control of V_{OUT} is essential. We believe that this work would provide

helpful guidelines for the development of ternary circuits using TMDs-based vdW-H technology.

Methods

Device Fabrication: The $MoSe_2$ and WSe_2 layers were mechanically exfoliated and transferred onto Si/SiO_2 substrate from bulk crystals using polydimethylsiloxane (PDMS) stamp method. To fabricate the p-n heterojunction consisting of WSe_2 (p-type) and $MoSe_2$ (n-type), the solution of polypropylene carbonate (PPC) in chloroform was spin-coated on Si/SiO_2 substrate. The PDMS was attached on PPC coated WSe_2 flake, and then it was immersed in the DI water for 10 min. The PDMS/PPC/WSe_2 sample was loaded on the $MoSe_2$ flake on heavily p-doped Si wafer covered with 300 nm-thick SiO_2 substrate. The PDMS/PPC/WSe_2/$MoSe_2$ sample was heated at 90 ℃ for 1 min. With cooling at room temperature, the PDMS was slowly disengaged, and the PPC film was removed by acetone cleaning. To fabricate the $MoSe_2$-WSe_2 vdW-H, the WSe_2 flake was partially overlapped with the form of head to tail hybrid on the surface of $MoSe_2$ flake. Next, Ti/Au (5/30 nm) as the source and drain (S/D) electrodes were deposited and patterned by e-beam evaporation and photolithography techniques. The length (L_{ch}) and width (W_{ch}) of the $MoSe_2$-WSe_2 vdW-H channel were 24.1 μm and 13.8 μm, respectively. Finally, $MoSe_2$/WSe_2 vdW-H-TR were annealed 250 ℃ in H_2/Ar condition to reduce the contact resistance between contact electrode and semiconductors.

In order to fabricate the MoS_2 floating gate transistor, PEDOT:PSS as the floating gate was spin-coated on Si/SiO_2 substrate at 4000 rpm for 1 min and annealed at 150 ℃ for 15 min. 80 nm-thick Al_2O_3 was then deposited by atomic layered deposition (ALD) at 200 ℃ for 4 h. After mechanically exfoliated MoS_2 were transferred onto Al_2O_3 floating gate insulator, Ti/Au (20/100 nm) were deposited by e-beam evaporator system. Then, S/D electrodes were patterned by standard photolithography and etching techniques. L_{ch} and W_{ch} of the MoS_2 channel in floating-gate transistor is 9.4 and 10.2 μm, respectively. Finally, 20 nm-thick Al_2O_3 passivation

layer on fabricated the device were deposited by ALD to prevent the effects of O_2 and H_2O. To implement the inverter circuit, we externally connected the drain and gate nodes of the $MoSe_2$-WSe_2 vdW-H and the MoS_2 floating-gate transistors, respectively.

Characterization: A laser confocal microscope (LCM) Raman was conducted with a He-Ar laser (λ_{ex} = 532 nm). The spot diameter of the focused laser beam in the LCM system was approximately 1 μm. AFM image and thickness of $MoSe_2$-WSe_2 vdW-H-TR were measured by an atomic force microscope (XE7, Park Systems) with non-contact mode. SEM images and EDS mapping of $MoSe_2$-WSe_2 vdW-H-TR were obtained by a secondary electron emission from the sample with a 15.0 kV acceleration voltage on top view. The electrical characteristics of the $MoSe_2$-WSe_2 vdW-H-TR were measured using a keithley 4200-SCS semiconductor characterization system connected with a probe station at room temperature in the air under dark condition. The photoresponsive behaviors of the $MoSe_2$-WSe_2 vdW-H-TR were investigated by a multichannel fiber-coupled laser source (MCLS1, Thorlabs) equipped with the single mode fiber optical patch cables (SM600).

Data availability

All data during this project are included in this article and supplementary information.

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Acknowledgment

This research was supported in part by the National Research Foundation of Korea (2018R1A2B2003558).

Author contributions

S.H., H.J.P., and H.Y. performed all experiments. H.W.C. and J.P. contributed to the experiments. H.Y. and S.K. supervised the project. S.H., H.P., H.Y., and S.K. wrote the manuscript. All authors have given approval to the final version of the manuscript.

Competing interests

The authors declare no competing financial interest.

Figures and captions

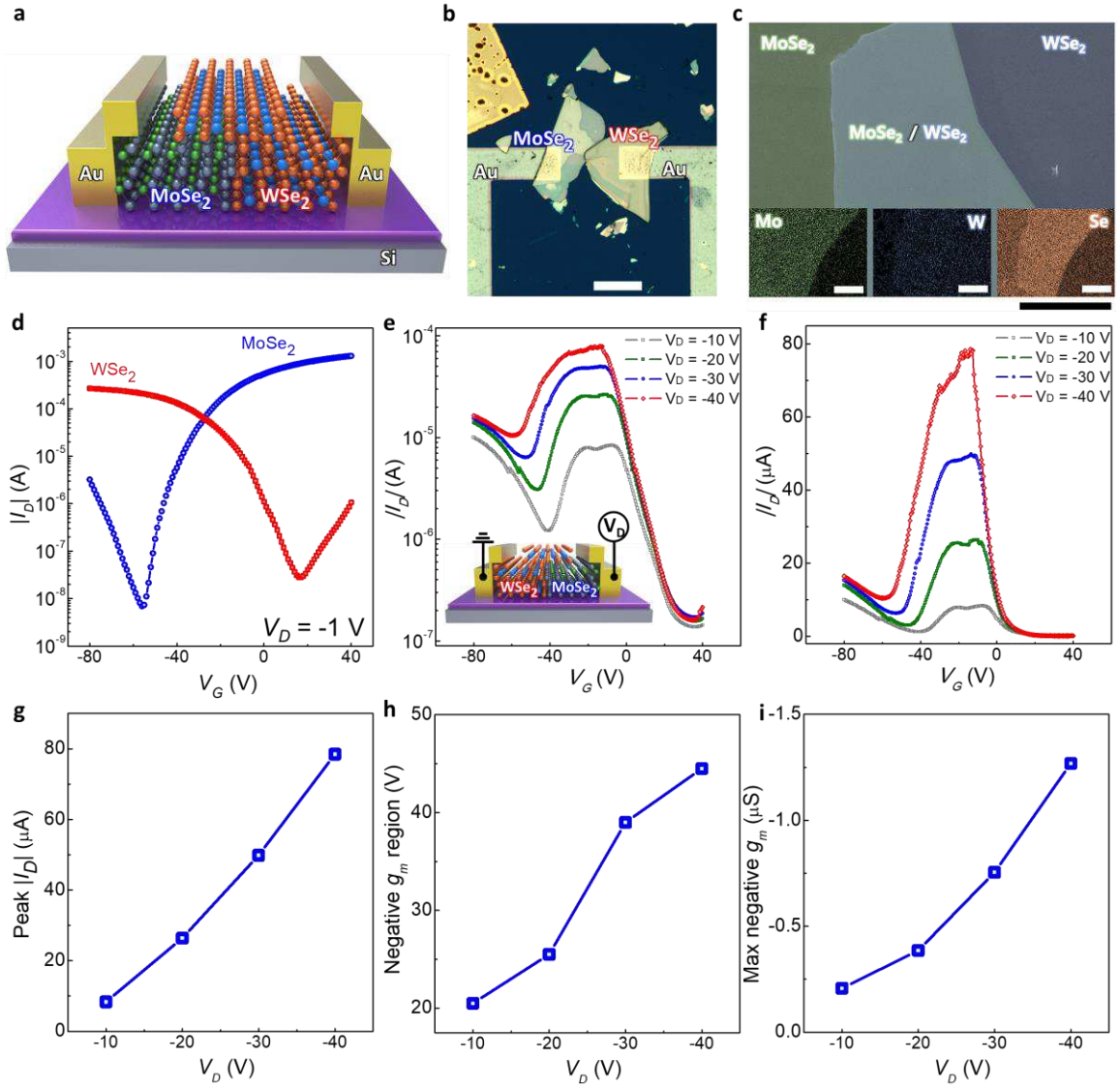

Figure 1. Investigation of the electrical characteristics of the $MoSe_2$–WSe_2 vdW-H-TR. a) 3D Schematic structure of the $MoSe_2$–WSe_2 vdW-H-TR. b) Optical microscopy image of the $MoSe_2$-WSe_2 vdW-H-TR. The scale bar is in 20 µm. c) False-colored SEM image of $MoSe_2$-WSe_2 vdW-H. EDS mapping of the Mo (green dot), W (blue dot), and Se (orange dot) distributions for $MoSe_2$-WSe_2 vdW-H. The length of the scale bar is 5 µm. d) Transfer characteristics of the baseline $MoSe_2$ (blue curve) and baseline WSe_2 (red curve) transistors at V_D= −1 V. e) Transfer characteristics of the $MoSe_2$-WSe_2 vdW-H-TR for V_D = −10, −20, −30, −40 V. f) Transfer characteristics of the $MoSe_2$-WSe_2 vdW-H-TR for different values of V_D in linear scale. Plot of g) peak I_D, h) negative g_m region, and i) maximum negative g_m values as a function of V_D for the $MoSe_2$-WSe_2 vdW-H-TR.

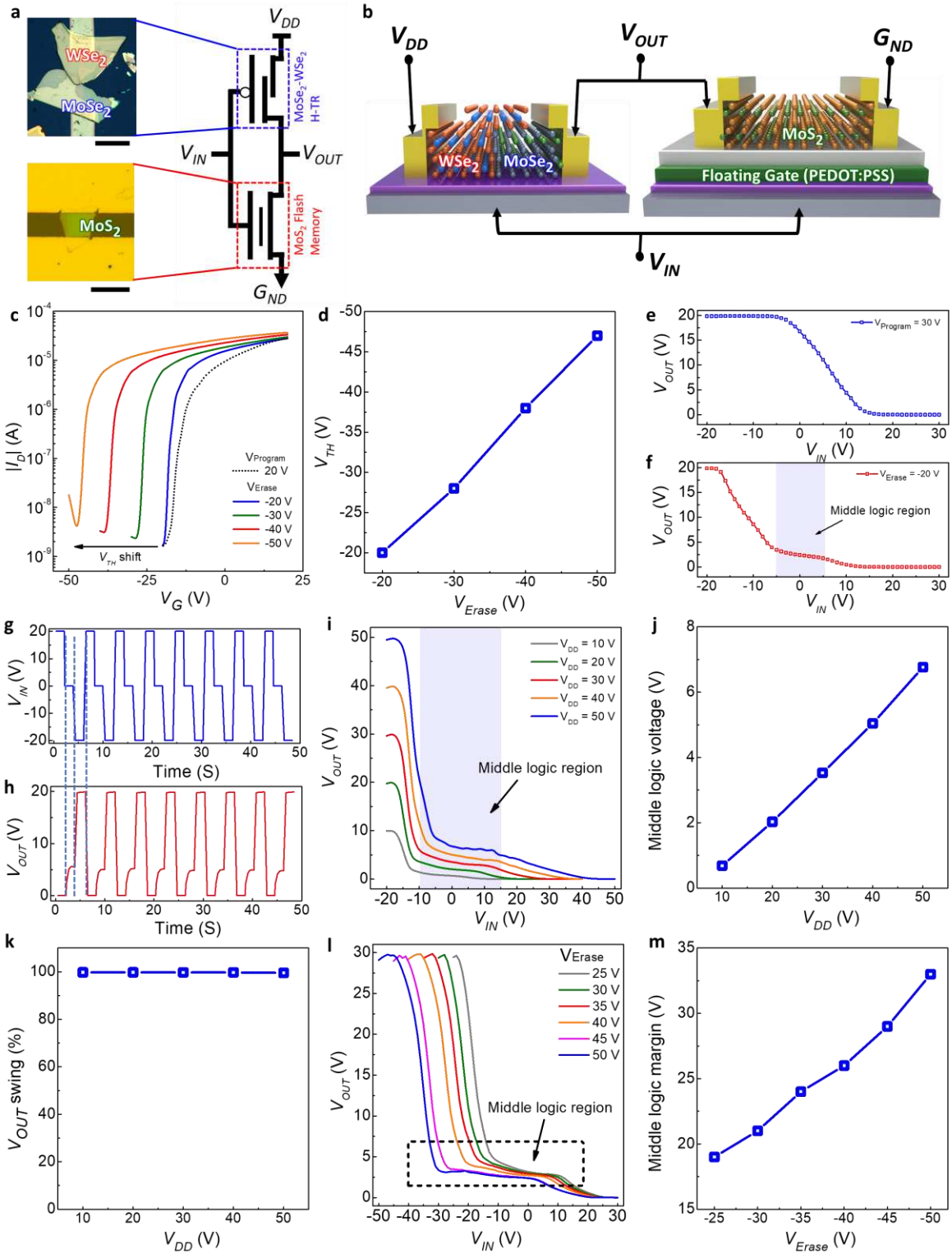

Figure 2. Ternary circuit using the proposed $MoSe_2$-WSe_2 vdW-TR and MoS_2 floating-gate transistor a) Schematic symbol of the ternary inverter using the $MoSe_2$–WSe_2 vdW-H-TR and the n-type floating-gate transistor. b) 3D schematic structure of the ternary inverter. c) Transfer characteristics of the MoS_2 floating-gate transistor depending on the applied erasing voltage

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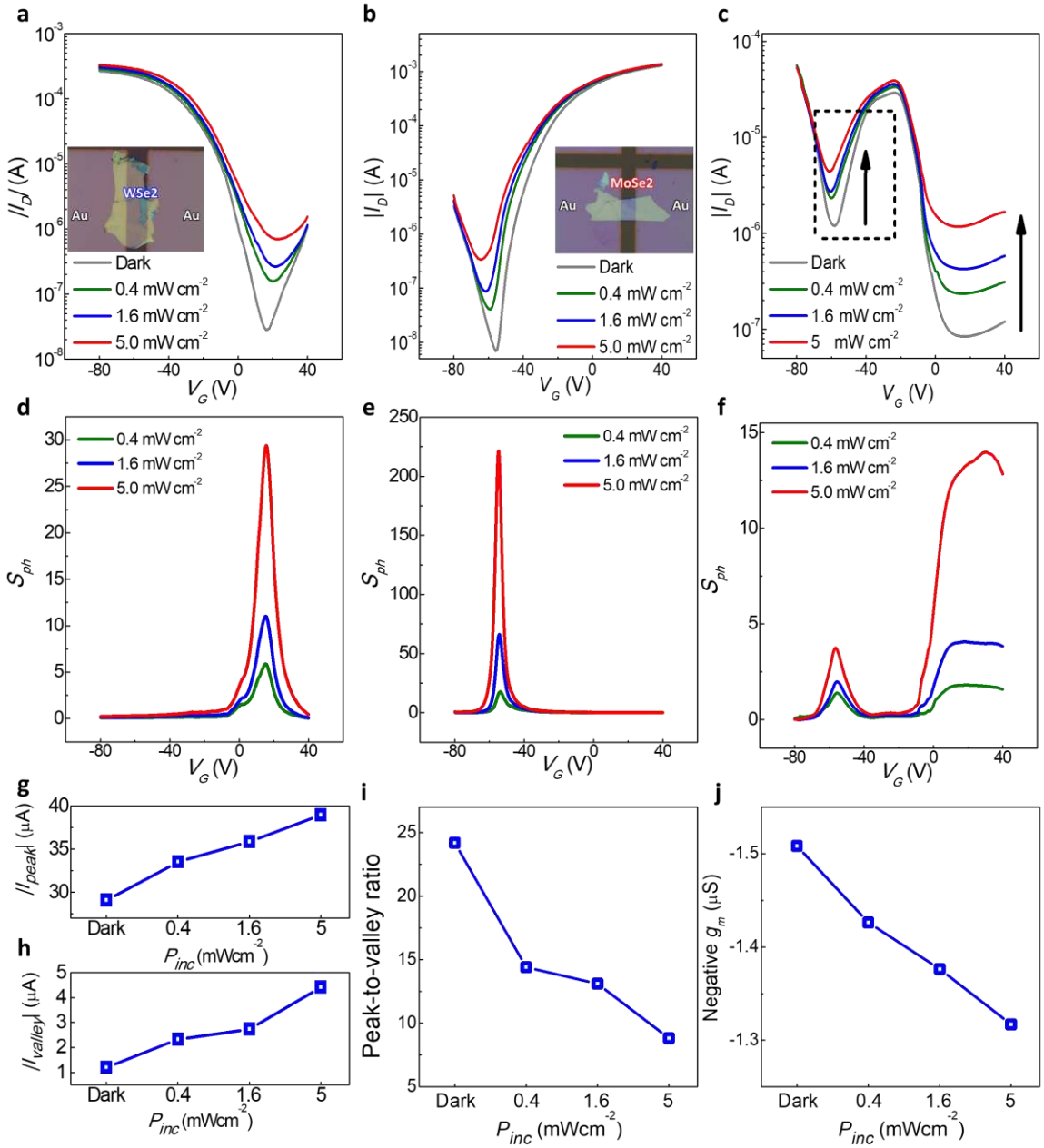

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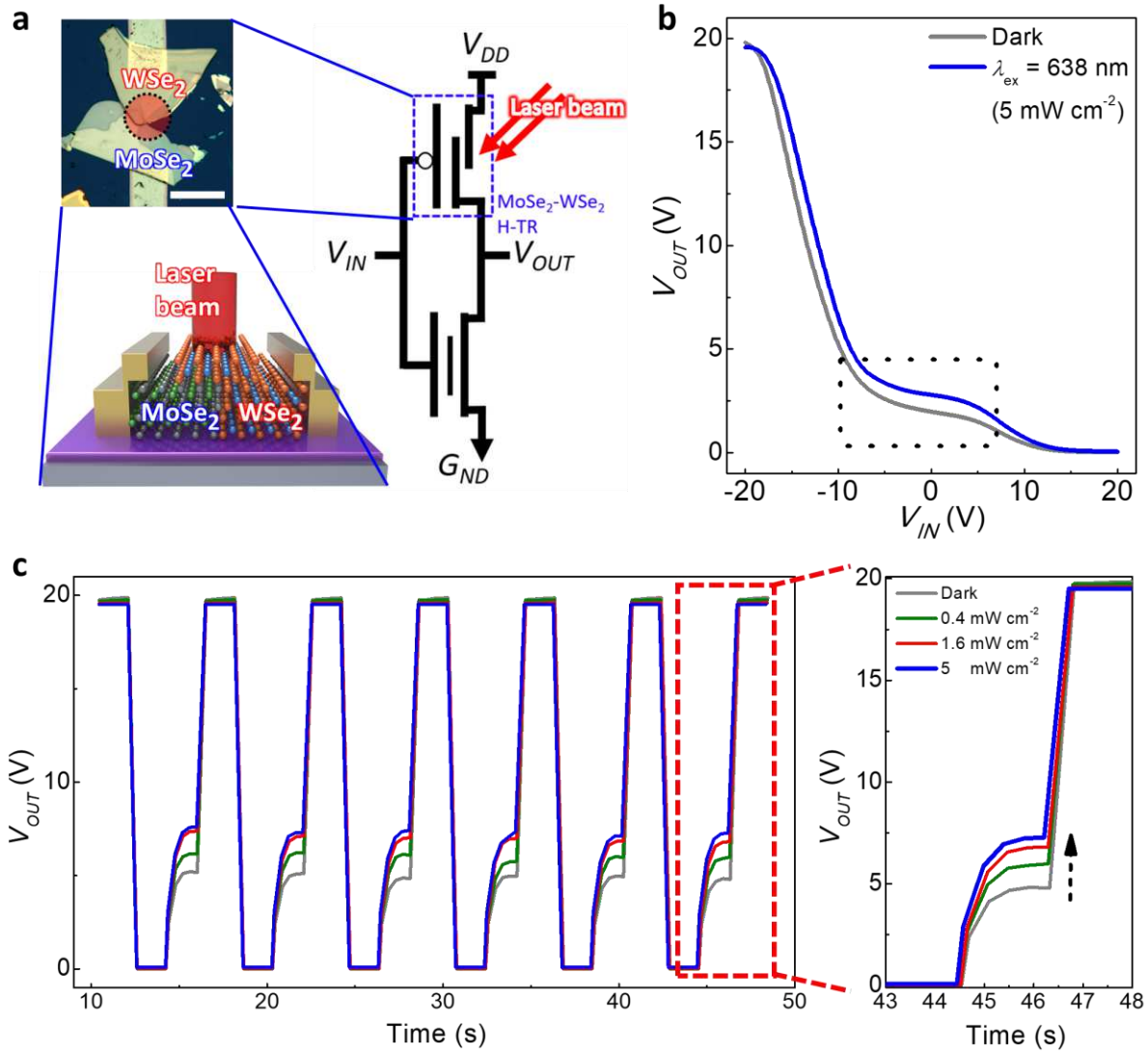

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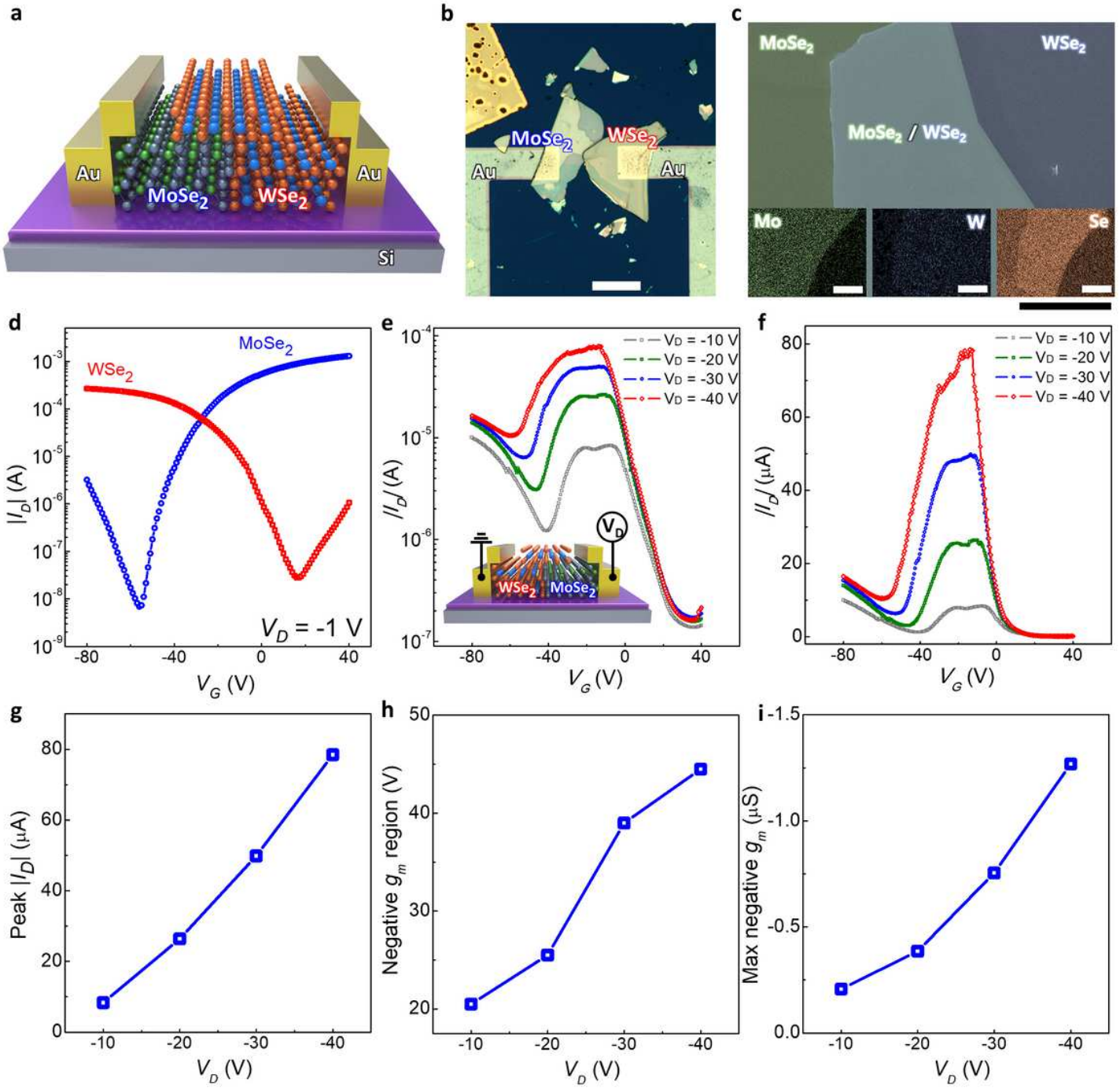
Figures



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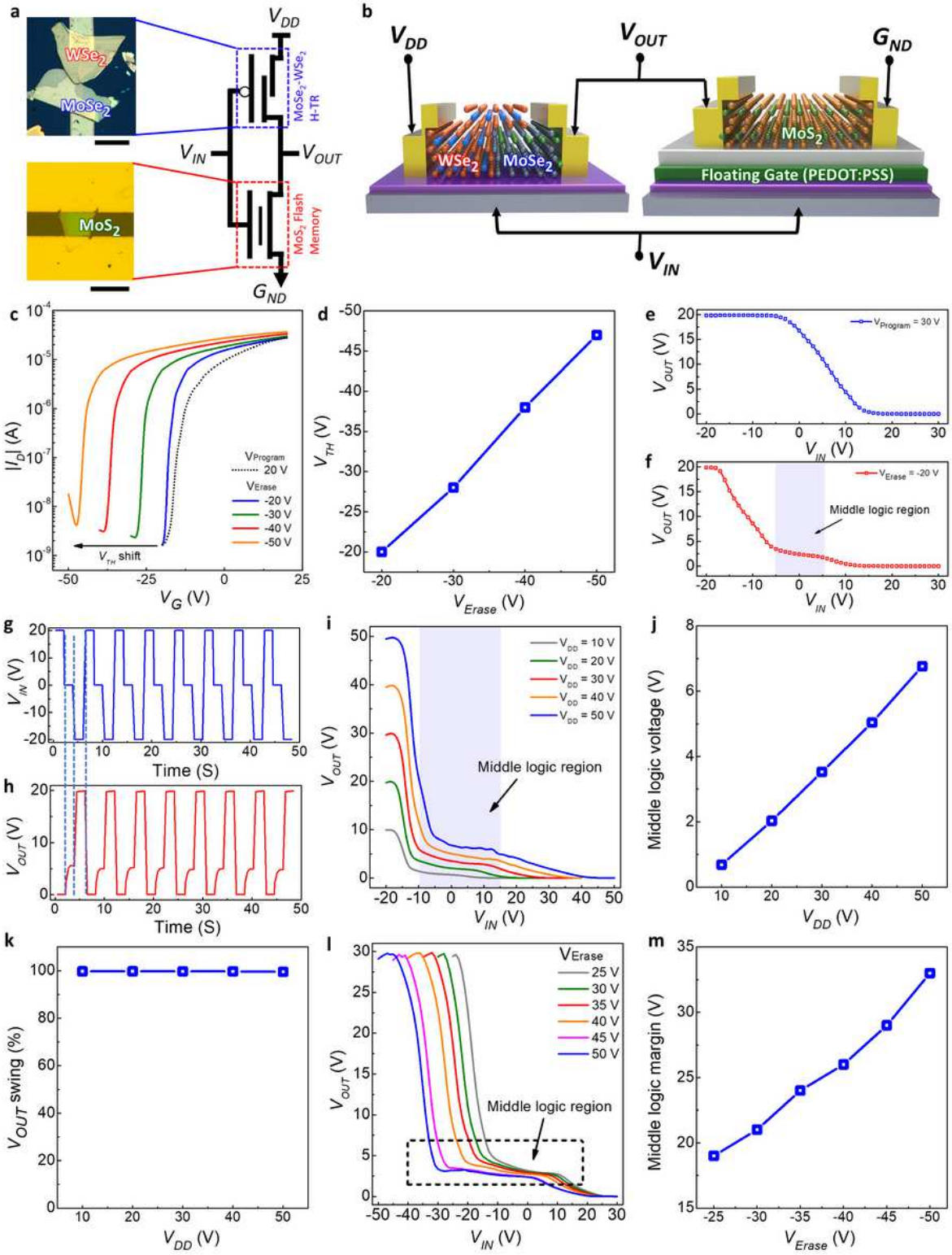

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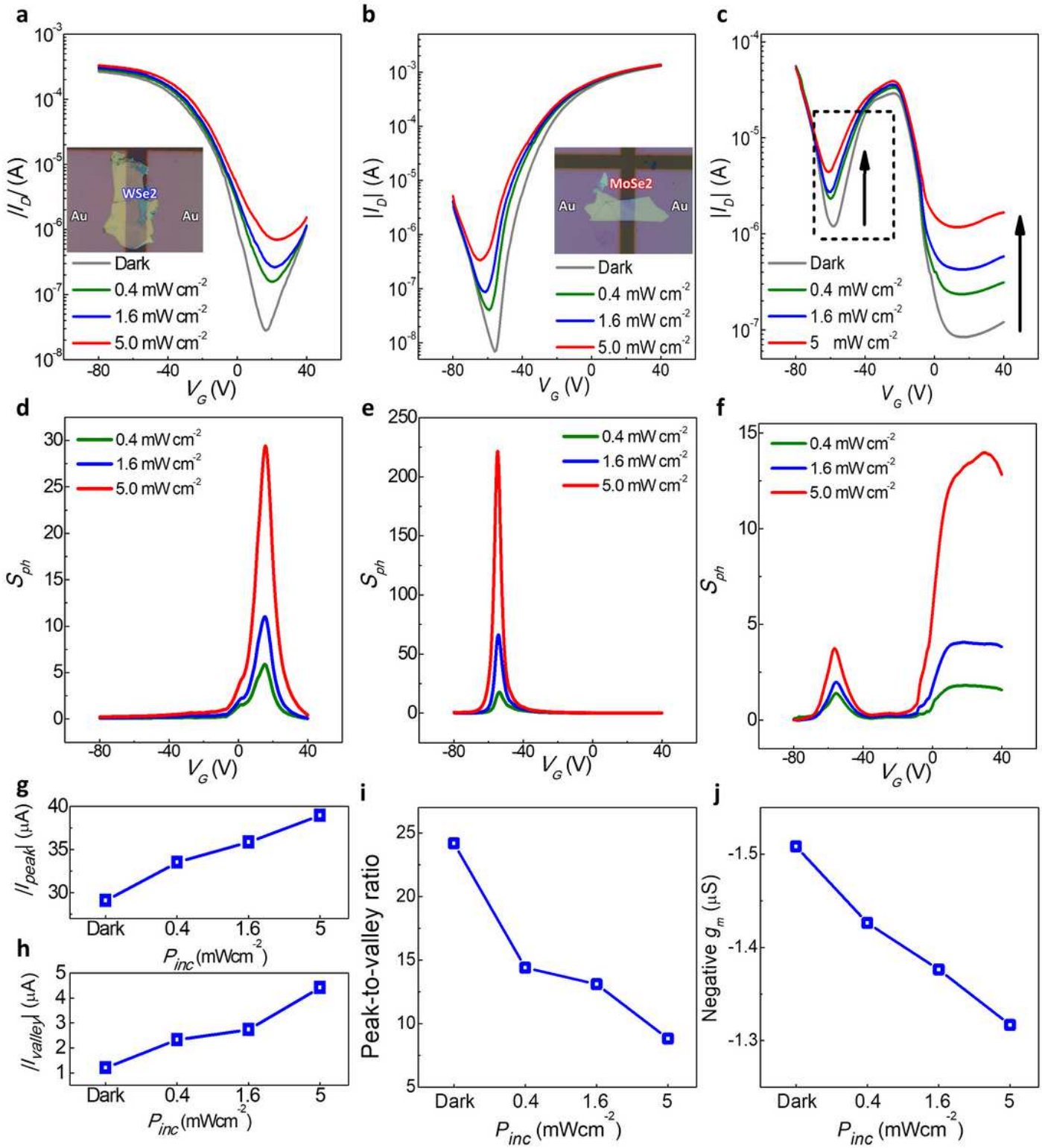

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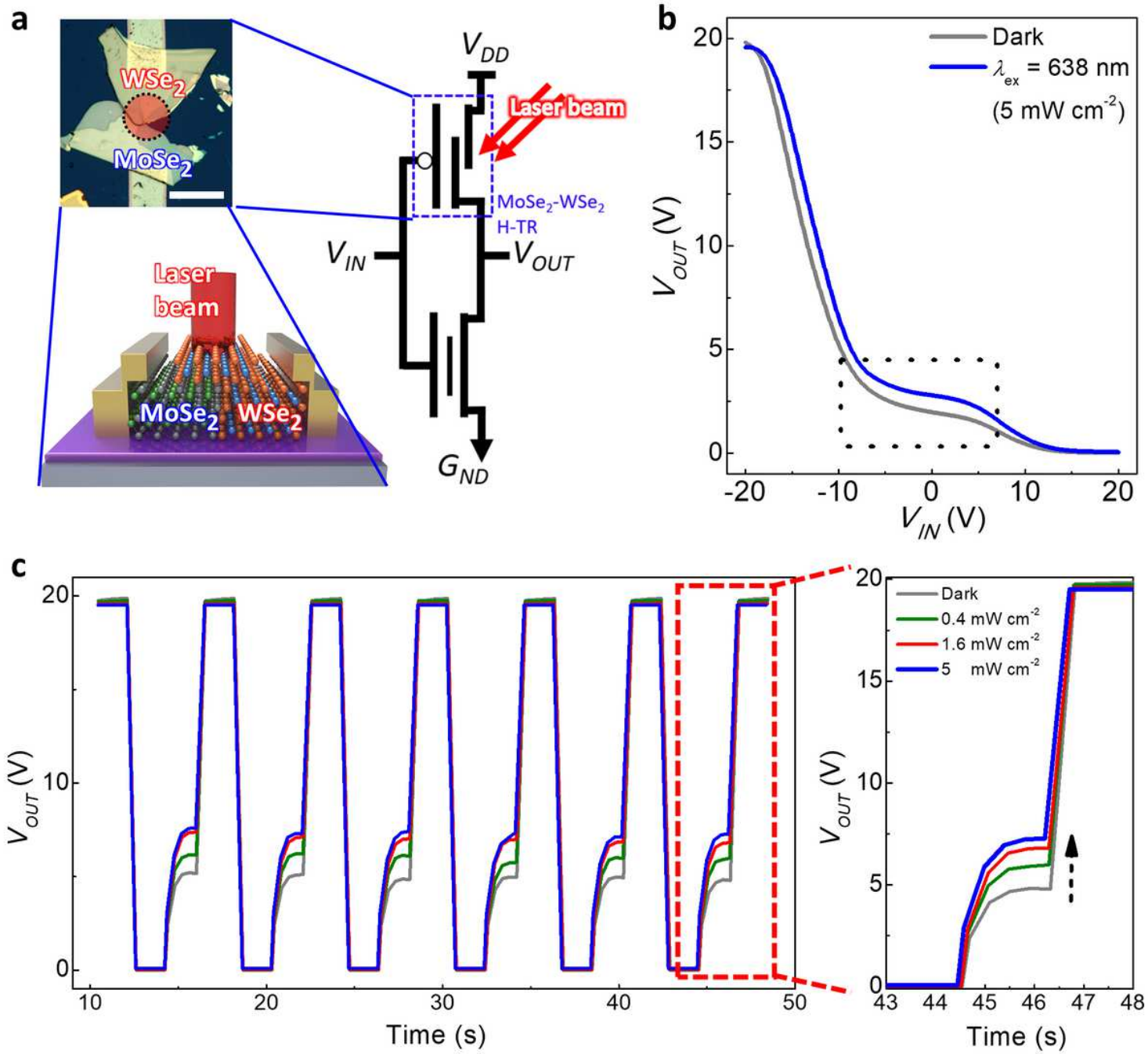

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