A Wide-Band High-Gain Doherty Power Amplifier With Class-AB HEMT Amplifiers

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Research

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A wide-band high-Gain Doherty power amplifier With Class-AB HEMT amplifiers

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Abstract: In this paper, an attempt has been made to design a Doherty power amplifier (DPA) with high-gain and wide-band. For this purpose, two peak amplifiers are used to improve the performance of the main amplifier. Main and auxiliary amplifiers with the same structure to the class-AB type and by using micro-strip lines in place of input/output and load matching networks, transmission lines and inductors of drain and gate, that minimize the losses in the DPA. The current DPA is implemented with GaN_HEMT_CLF1G0530_100v transistor and Rogers4003 substrate, which for 1GHz frequency in 0.5-1.5GHz bandwidth will be able to be at P-1dB point (this point, input power as 30dBm and output power as 47.98dBm) increase Drain efficiency and Power added efficiency (PAE) to 81.95% and 80.73%, respectively. The DPA helps to expand the back-off region and extend the linearity region, so the Peak to average power ratio (PAPR) will be 5.21dB and the Adjacent channel power ratio (ACPR) as 58.7dBc. A gain of 17.06-17.92dB was also obtained, which is significant compared to the results of similar samples.

Keywords: Doherty power amplifier (DPA), P-1dB, Peak to average power ratio (PAPR), Adjacent channel power ratio (ACPR), Output power Back-off (OBO)

1. Introduction

Increasing the rate of applicants for communication systems has led the attention of designers in this field to systems with higher efficiency and durability. The most consumed and costly a component in telecommunication systems is called a power amplifier (or PA for short), which today has significant application in cases such as mobile phones, radio, television, medical equipment, etc. In fact, this block has the task of amplifying the weak DC power and converting it to considerable RF power. Therefore, its output power and high efficiency have become a significant factor. However, due to non-ideal conditions of the circuit, such as stress voltage or Non-ideal devices, it will not always be possible to achieve high output power. For example, as mentioned in [1], by controlling the signal amplitude, as in [2] by controlling the signal phase, High output power and optimal efficiency can be achieved. It should be noted that amplitude and Phase control equipment has a complex design and high implementation costs. It is also possible to increase the output power by installing optimal transformers [3] in the signal transmission ways. Transformers are often heavy components and are not recommended for portable systems. Multi-stage PAs, such as [4, 5] with Series structures in several stages amplify the signal and ultimately increase the gain and efficiency. In Series structures, the design of appropriate matching networks between each stage increased the complexity of the circuit and made it difficult for the designer.

In contrast, Doherty power amplifiers without the need for control equipment, will be able to provide acceptable results for less complexity and cost. DPAs by different circuit structure, such

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as hybrid [6] or multi-way circuits [7], also increase output power and efficiency. The use of switching mode PAs [8] in the position of the main PA is often seen in articles in this field that have improved PA performance. It should be noted that switching mode amplifiers, due to their switching performance, add to the non-ideal circuit conditions, because the existence of non-zero transistor time and non-zero resistance, etc. will always exist.

2. Methods

The DPA presented in this work is made of three similar class-AB PAs, which are arranged as shown in Figure 1, one amplifier as of the main PA and the Peak amplifiers as of the auxiliary PA. The reason for choosing class-AB is its advantages compared to other reinforcement classes. In a fact, simple construction, good gain and efficiency, and no switching problems have always played a role in choosing a designer. The use of passive micro-strip lines maximizes power transmission and reduces recurrent losses, making the circuit more stable against potential losses of RF frequency radiation and fluctuations of stress voltages. The lines used also have excellent power in integration and PCB (printed circuit board), which makes the circuit easier to implement and build. The proposed DPA with optimal power divider design transmits the signal transmission to the PA branches perfectly evenly, which eventually integrates the amplified signals in each branch at the output of the circuit.

In two-circuit circuits, due to phase and impedance changes, the bandwidth is limited. To solve in, the designer controls the process of impedance changes by designing a suitable load matching network according to [9] and has improved the bandwidth. In this work, by observing the construction considerations and selecting the optimal blocks in different parts of the amplifier, the desired efficiency for the circuit has been obtained, which can be clearly seen in the results of the Layout test and its schematic.

In this paper, in the Section 3, the structure of Doherty amplifier is examined. In the Section 4, the operation of the DPA will be described and in the Section 5, it is dedicated to measuring the basic parameters of PA (Layout test and schematic test) and in the Section 6, discusses the results and problems of the work and finally, in the Section 7, while summarizing of the proposed circuit are compared with similar DPAs of other papers.

3. Proposed Structure

The proposed DPA is designed from three classes of same class-AB power amplifiers arranged with HFET transistor. The proposed AB-class (see Figure 2), consists of input resonators, inductor of Gate and drain equivalent lines, coupling capacitors, gate-source voltage (V_{GS}) , and drain-sources voltage (V_{DS}), gate resistors, impedance matching networks at the input and output ports. The input resonator increases the PA stability range by controlling possible fluctuations in the transistor terminals and establishes the isolation gate resistance between the DC and RF signals.

The present class-AB operates with voltages of V_{GS} = 60V and V_{DS} = -1.9V, which are determined according to the information in the transistor datasheet. Inductor Gate and drain equivalent lines are also responsible for establishing and supplying circuit current. In this work, micro-strip

composite lines with length of 31.55mm and width of 0.8mm and 0.7mm have been adjusted for the equivalent line of gate and drain, respectively, with relations 1 and 2 are obtained so that the specified width maintains the maximum current in the circuit and the electrical length is maintained at 90 degrees.

$$A = (t \cdot W \cdot 1.378) \quad (1)$$

$$I_{MAX} = (k \cdot T_{RISE}^{b}) \cdot A^{c} \quad (2)$$

Table 1. *λ/4* line parameters

A	cross-section area [mil^2]
W	Line width [mm]
t	Line thickness [µm]
I_{MAX}	maximum current [Ampere]
T_{RISE}	Maximum desired temperature rise [°C]
k, b, c	constants : k = 0.048, b = 0.44, c= 0.725

The input and output impedance matching networks (Figure 4) are also designed to minimize the return power and transfer the maximum power by matching the impedance obtained in each port with the optimal impedance of 50 ohms by analyzing the load-pull and source-pull and Smith chart (The impedance at the input of the main/Peak PA is 11.7 + j6.83 and its output impedance is 42.8-j23.15). Then, a four-port power divider is designed that transmits the input signal equally to the three main and auxiliary amplifier branches. In the proposed power divider structure (Figure 3), resistors R1 and R2 are used between its output terminals to prevent signal leakage to each port and to establish proper isolation, the results of which are shown in Figures 5 and 6. Finally, after arranging the duplex structure with the help of series blocks of micro-strip lines, the optimal matching load is adjusted at the output, which will control the process of impedance changes. All passive lines used with Rogers4003 substrate with a thickness of 32microns and the specifications mentioned in Table 2 are designed, which is shown in Figure 7 of the final layout of the proposed circuit, which is ready for construction and implementation.

Table 2. Rogers-4003 substrate parameters in the layout of the proposed DPA

Relative Dielectric Constant	Relative Permeability	Conductivity	Cover Height	Conductor Thickness	Dielectric Loss Tangent
3.55	1	5.8E+7	1e+033mm	18 µm	0.0021

4. Performance of Proposed DPA

At first, when the power to the circuit is low, the main PA turns on and amplifies the signal slightly. As a result, the Back-off region is smaller and reaching the P-1dB point is faster. As the input power increases, the working range of the main PA will reach saturation regions. At this stage, the auxiliary amplifiers come into play and with their bias will transfer some power to the output Power of the PA. This will increase the Output power Back-off (OBO) and increase the P-1dB. As result, it reduces the speed of reaching the saturation region. As the output power increases, the efficiency will also increase. It should be noted that according to the principle of active money, loading the current of each branch of PAs will affect the amount of output impedance and the process of rapid changes in impedance and phase at the output will lead to bandwidth limitation. To solve this, a suitable load matching network with the help of micro-strip blocks is designed to adapt the output impedance changes of the circuit to the optimal impedance of 50 ohms and will slow down the process of changes, so bandwidth is improved over a wide bandwidth of 1GHz.

5. Simulation and Layout/Schematic Test

The proposed the DPA test has been performed in two schematic cases and Layout, the necessary explanations of which are given below.

5.1. Availability of device

In this work, two transistors GaN_HEMT_CLF1G0530_100v are used, which are made by Ampleon company, and other components, including resistors and capacitors, are used in the structure, designed at a reasonable price, and a substrate, which is Rogers4003, with PCB capability Becoming excellent can be prepared.

5.2. Information of the DPA Test

By Layout testing the proposed PA at 1GHz and for a 24dBm input power as shown in Figure 8, the circuit stability parameters will be established over a wide frequency range by means of Equations 3 and 4. Also, the design of suitable input/output matching networks in each port of PA minimizes the return power at the input and output ports and is obtained according to Figure 9.

$$K= (1 - |S_{11}|^2 - |S_{22}|^2 + |Beta|^2)*(2|S_{21}\,S_{12}|)^{-1} \quad (3)$$

$$Beta = S_{11}S_{22} + S_{12}S_{21} \quad (4)$$

Also, the output power will reach 49.78dBm at the point P-1dB (Figure 10), which establishes the desired linearity at 6dB in the Back-off (OBO) region, so that PAPR is 5.21dB and ACPR is 58.7dBc is obtained and Gain compression is also evaluated as 0.25dB.

$$PAPR = 10*log(P_{peak} / P_{avg}) \quad (5)$$

$$ACPR = 10*log(P_{total}/P_{adjacent}) \quad (6)$$

Drain efficiency (DE) and PAE (with equations 7, 8) and Gain increased and interest reached 81.95%, 80.73% and 17.92 dB (Figures 11, 12 and 13), respectively, which has increased significantly compared to the results of the class-AB (Figure 14).

$$PAE(\%)= [(P_{out(W)} - P_{In(W)})/P_{dc}]*100 \quad (7)$$

$$DE(\%)= (P_{out(W)})/P_{dc})*100 \quad (8)$$

With Compared the results of the schematic test and the Layout test of the DPA, it is clear that there has always been some loss in the circuit, which has led to a decrease in the Layout test parameters compared to the schematic test results, which is due to losses of ideal devices, RF frequency and stress voltages.

5.3. Competing Interest

Not applicable

5.4. Funding

No organization has played a role in funding the work provided, and the authors have personally borne all the necessary costs.

5.5. Authors Contribution

The authors participated in the proposal in a completely equal way. In this way, Mr. Pouya Jahanian has been involved in simulating the DPA, the translation of the report and reviewing the results, and Ms. Azadeh Norouzi Kangarshahi has played a role in collecting information, classification and reviewing the results.

5.6. Abbreviations

The abbreviated expressions in this work are presented in Table 3.

Table 3. List of abbreviations

PA	Power Amplifier
DPA	Doherty Power Amplifier
PAE	Power Added Efficiency
DE	Drain Efficiency
PAPR	Peak to average power ratio
ACPR	Adjacent channel power ratio
OBO	Output power Back-off
PCB	Printed circuit board
VDS	Drain-sources voltage
VGS	Gate-sources voltage

6. Results and Discussion

In the proposed DPA design, construction considerations have been tried to be observed as much as possible, such as the use of micro-strip lines with measured dimensions or the design of impedance matching networks with excellent accuracy, etc., which have ultimately improved losses and amplifier parameters. However, it should be noted that these measures will not always be able to reduce losses and radiation to zero, because the reflective power at the ports of the circuit

and the effects of colliding substrates with stress voltages, sudden increase in frequency, etc. can cause fluctuations in the circuit, but optimal Instruments such as embedding parallel resonators in the path of the input signal to each branch of the PAs and the load matching network at the output of the DPA and other items mentioned above secure the circuit to an acceptable level that the results and results Highlights the present design.

7. Conclusion

In this work, with the design of a three-stage Doherty power amplifier consisting of a main PA and two peak PAs of a same type of class-AB, the efficiency and gain in the 0.5-1.5GHz bandwidth has increased. So, the Drain efficiency in the linear region of the DPA is up to 81.95% and PAE up to 80.55% and the output power reaches 47.98dBm. In this work, the existence of appropriate matching networks in each port have minimized losses, which reduces energy consumption and makes the use of passive micro-strip lines in different parts of the circuit easier to build; and implement.

Table 4. Comparison of the proposed DPA performance with other works in the literature

Ref	Frequency (GHz)	Pout (dBm)	DE@OBO (%)	Gain (dB)
[10]*	2.8-3.6	43.45	42-61	8-12
[11]**	3.3-4.3	43.2-44.5	46-52	7.2-11.1
[12]**	2.7-3.4	42.2-43.7	36.7-43.2	7.2-11.13
[13]*	1.5-3.8	42.3-43.4	43	9.5-11
[14]**	2.2	43.6	54	9.7
[15]**	1.4-2.4	41.8-43.5	35.5-52	6-13
[16]**	20	42	58	10.2
This work**	**0.5-1.5**	**44-47.98**	**42-81.95**	**17.06-18.3**
This work*	**0.5-1.5**	**44.7-48.1**	**45-88.15**	**17.92-19.27**

*Simulation results, **post-layout results

References

[1] Hwang, Taesong, et al. "Nonlinearity modeling of a Chireix outphasing power amplifier." *IEEE Transactions on Circuits and Systems I: Regular Papers* 62.12 (2015): 2898-2907.

[2] Qureshi, Abdul R., et al. "A 112W GaN dual input Doherty-outphasing power amplifier." *2016 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2016.

[3] Yin, Yun, et al. "A broadband switched-transformer digital power amplifier for deep back-off efficiency enhancement." *IEEE Journal of Solid-State Circuits* 55.11 (2020): 2997-3008.

[4] Trinh, Van-Son, and Jung-Dong Park. "A 25.1 dBm 25.9-dB Gain 25.4% PAE X-band Power Amplifier Utilizing Voltage Combining Transformer in 65-nm CMOS." *IEEE Access* 9 (2021): 6513-6521.

[5] Zhang, Xuexue, et al. "A 39 GHz Power Amplifier with High Output Power and High Efficiency for 5G Communication System." *2020 IEEE MTT-S International Wireless Symposium (IWS)*. IEEE, 2020.
[6] Zhang, Zhiwei, et al. "A broadband Doherty power amplifier with hybrid class-EFJ mode." *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.12 (2020): 4270-4280.
[7]Kang, Hyunuk, et al. "Symmetric three-way Doherty power amplifier for high efficiency and linearity." *IEEE Transactions on Circuits and Systems II: Express Briefs* 64.8 (2016): 862-866.
[8]Hashemi, Mohsen, et al. "A highly linear wideband polar class-E CMOS digital Doherty power amplifier." *IEEE Transactions on Microwave Theory and Techniques* 67.10 (2019): 4232-4245.
[9]Kwon, Jin-hee, et al. "Broadband Doherty power amplifier based on asymmetric load matching networks." *IEEE Transactions on Circuits and Systems II: Express Briefs* 62.6 (2015): 533-537.
[10] Nasri, Abbas, et al. "Design of a Wideband Doherty Power Amplifier with High Efficiency for 5G Application." *Electronics* 10.8 (2021): 873.
[11] Shen, Ce, et al. "A 3.3–4.3-GHz High-Efficiency Broadband Doherty Power Amplifier." *IEEE Microwave and Wireless Components Letters* 30.11 (2020): 1081-1084.
[12] Jia, Pei, Fei You, and Songbai He. "A 1.8–3.4-GHz bandwidth-improved reconfigurable mode Doherty power amplifier utilizing switches." *IEEE Microwave and Wireless Components Letters* 30.1 (2019): 102-105.
[13] Rubio, Jorge Julian Moreno, et al. "Design of an 87% fractional bandwidth Doherty power amplifier supported by a simplified bandwidth estimation method." *IEEE Transactions on Microwave Theory and Techniques* 66.3 (2017): 1319-1327.
[14] Hasin, Muhammad Ruhul, and Jennifer Kitchen. "Optimized load trajectory for finite peaking off-state impedance-based Doherty power amplifiers." *IEEE Microwave and Wireless Components Letters* 29.7 (2019): 486-488.
[15] Hasin, Muhammad Ruhul, and Jennifer Kitchen. "Exploiting phase for extended efficiency range in symmetrical Doherty power amplifiers." *IEEE Transactions on Microwave Theory and Techniques* 67.8 (2019): 3455-3463.
[16] Fang, Xiao-Hu, Hao-Yu Liu, and Kwok-Keung M. Cheng. "Extended efficiency range, equal-cell Doherty amplifier design using explicit circuit model." *IEEE Microwave and Wireless Components Letters* 27.5 (2017): 497-499.

Figure

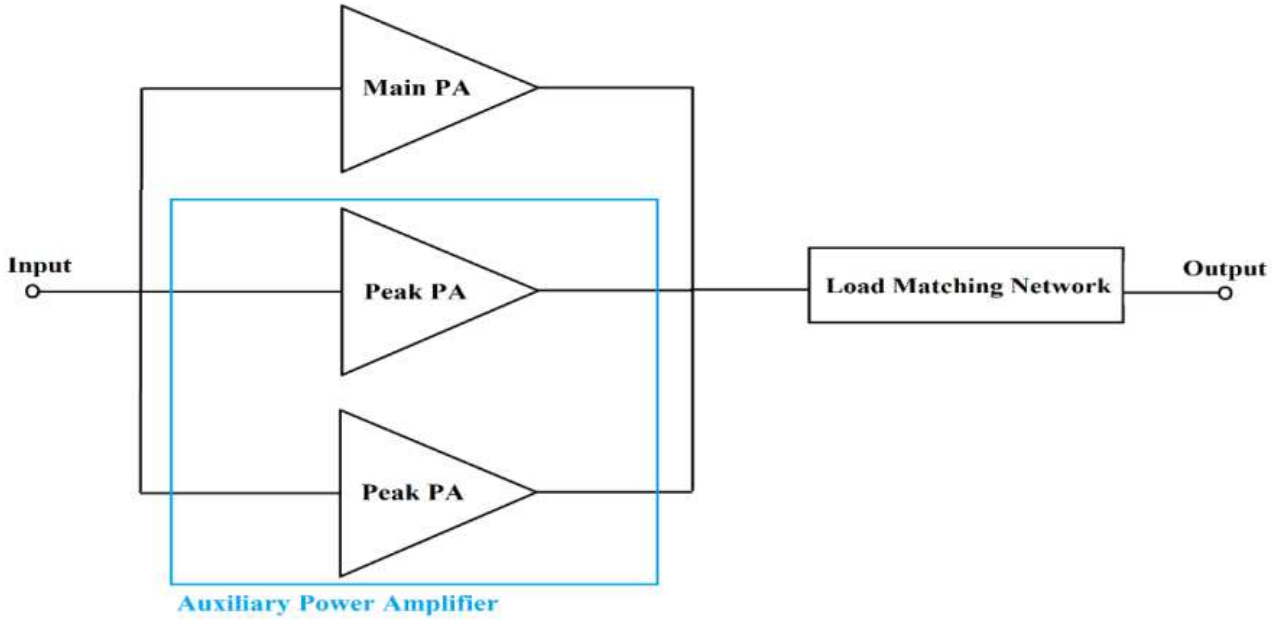


Figure 1. Diagram of the proposed DPA

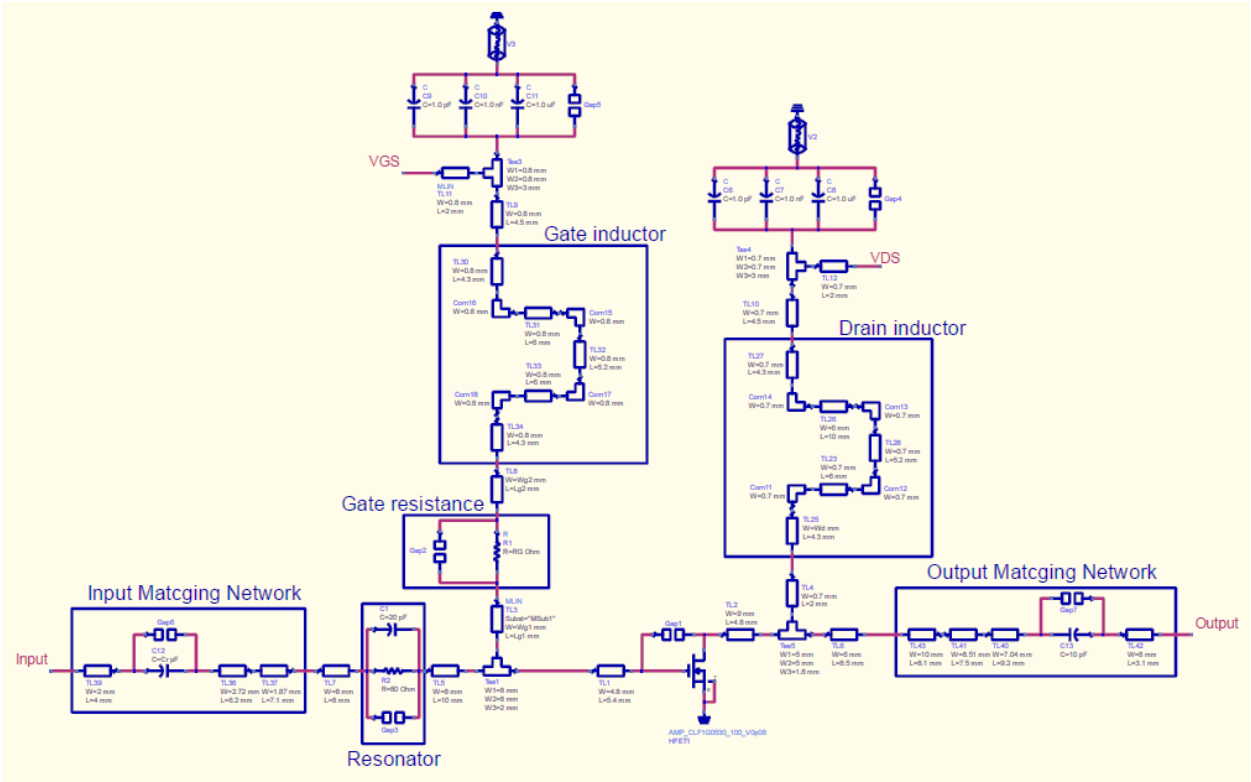


Figure 2. Schematic of the Proposed Class-AB PA

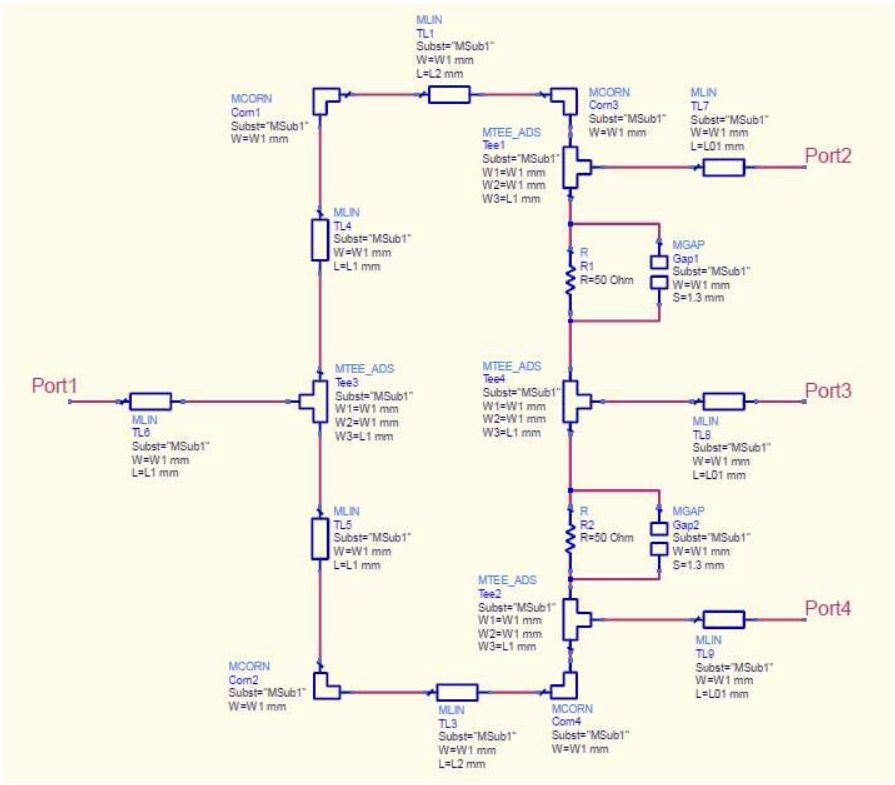
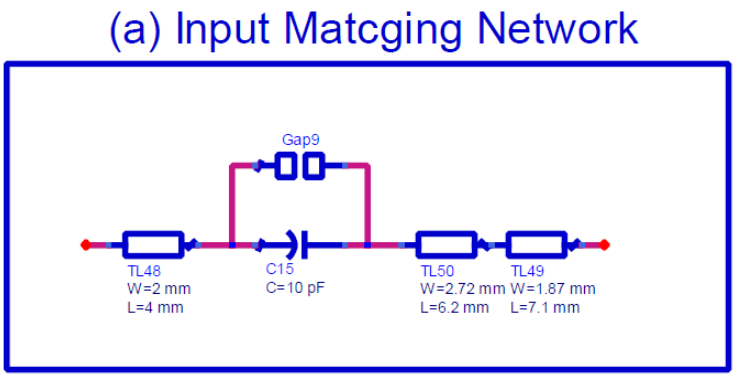
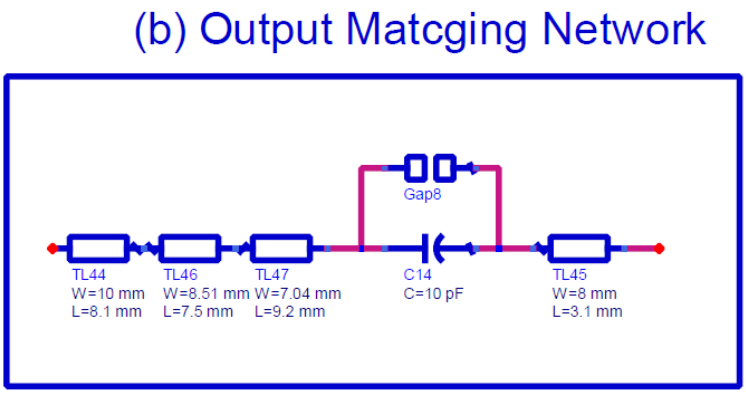


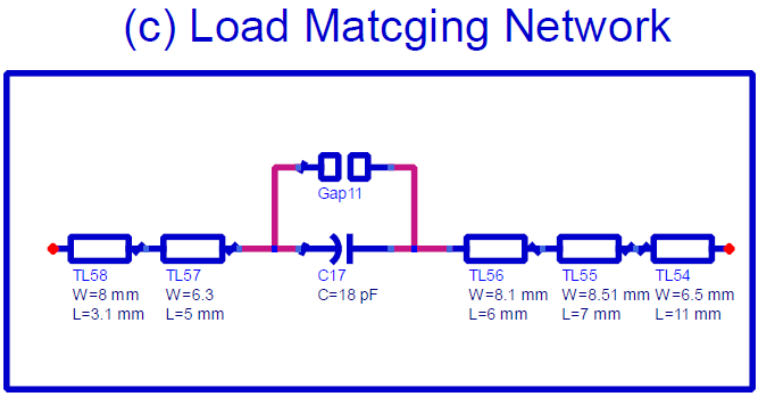
Figure 3. Dividerof the Proposed DPA



(a)



(b)



(c)

Figure 4. Matching Networks for a) input port of Class-AB, b) output port of Class-AB, c) Load port of the DPA

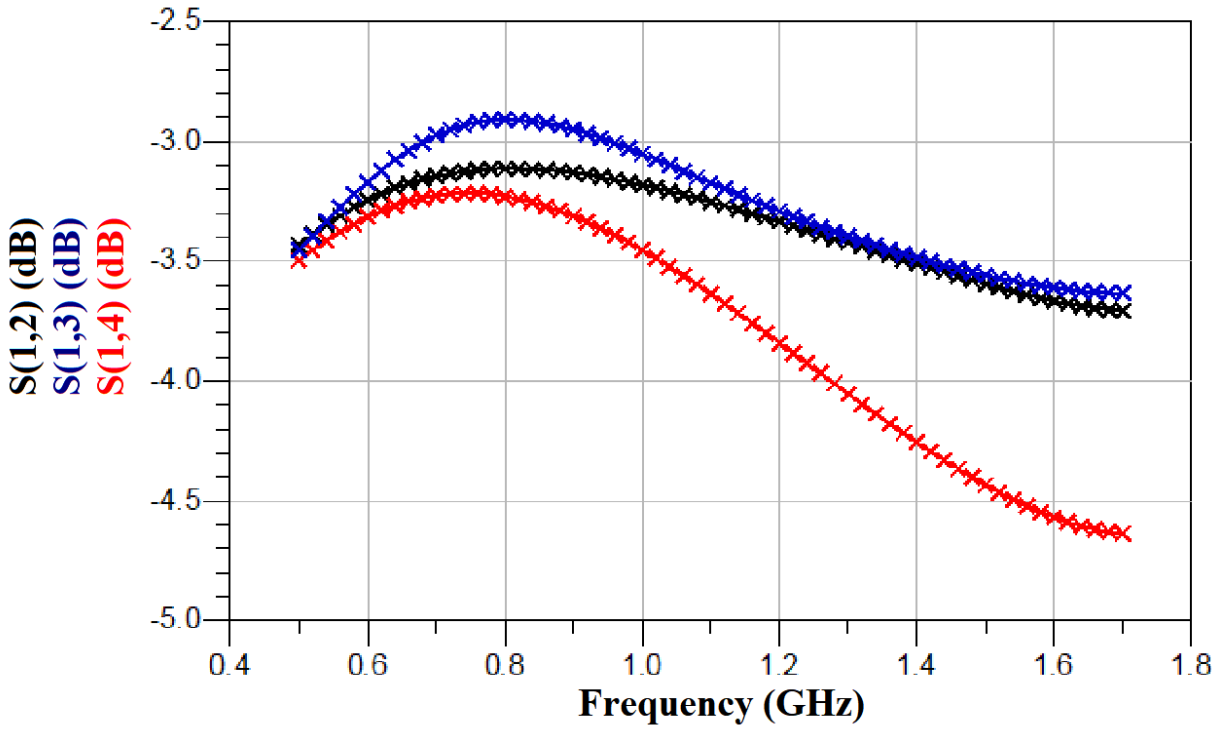


Figure 5. S-Parameters of the proposed divider Power division (S_{12}, S_{13}, S_{14})

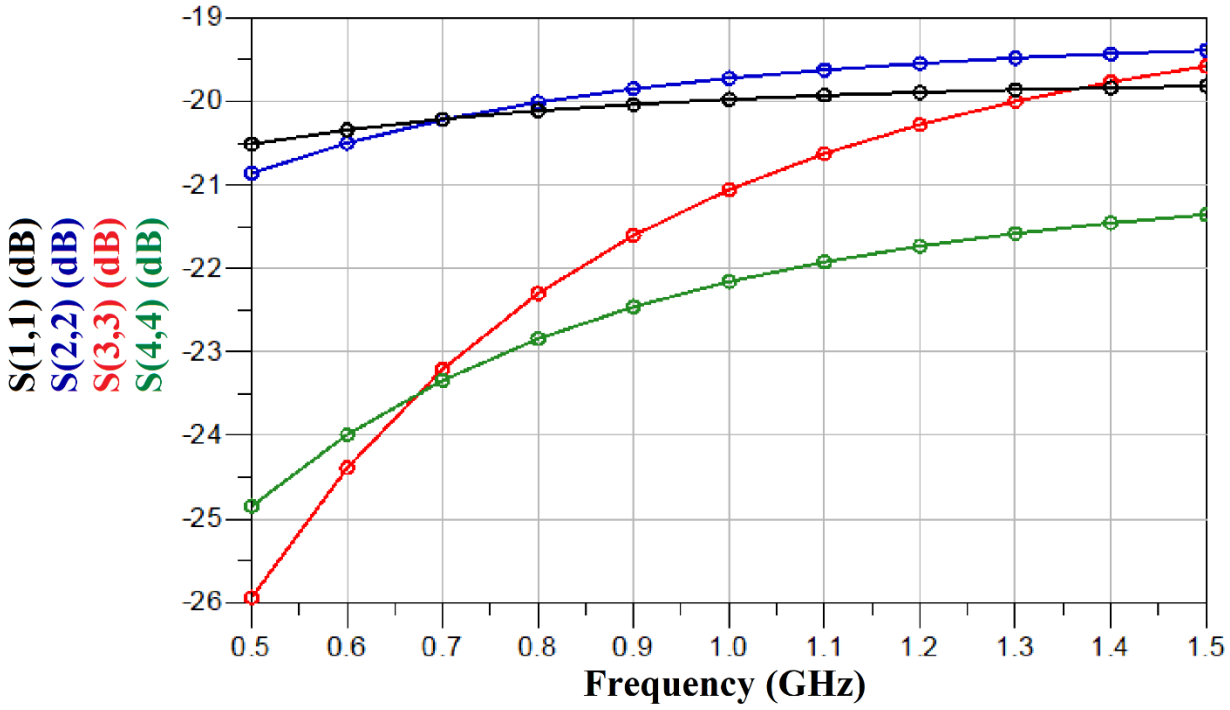


Figure 6. S-Parameters of the proposed divider Reflection (S_{11}, S_{22}, S_{33}, S_{44})

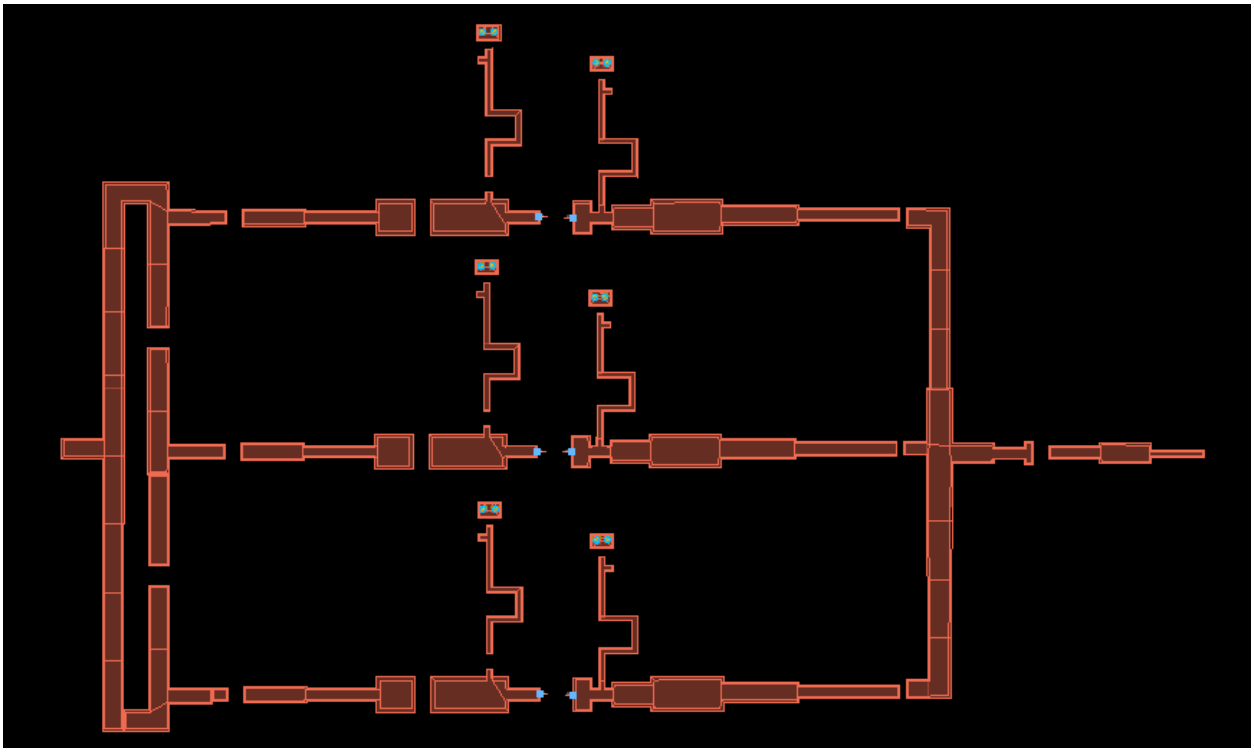


Figure 7. Layout of the proposed DPA

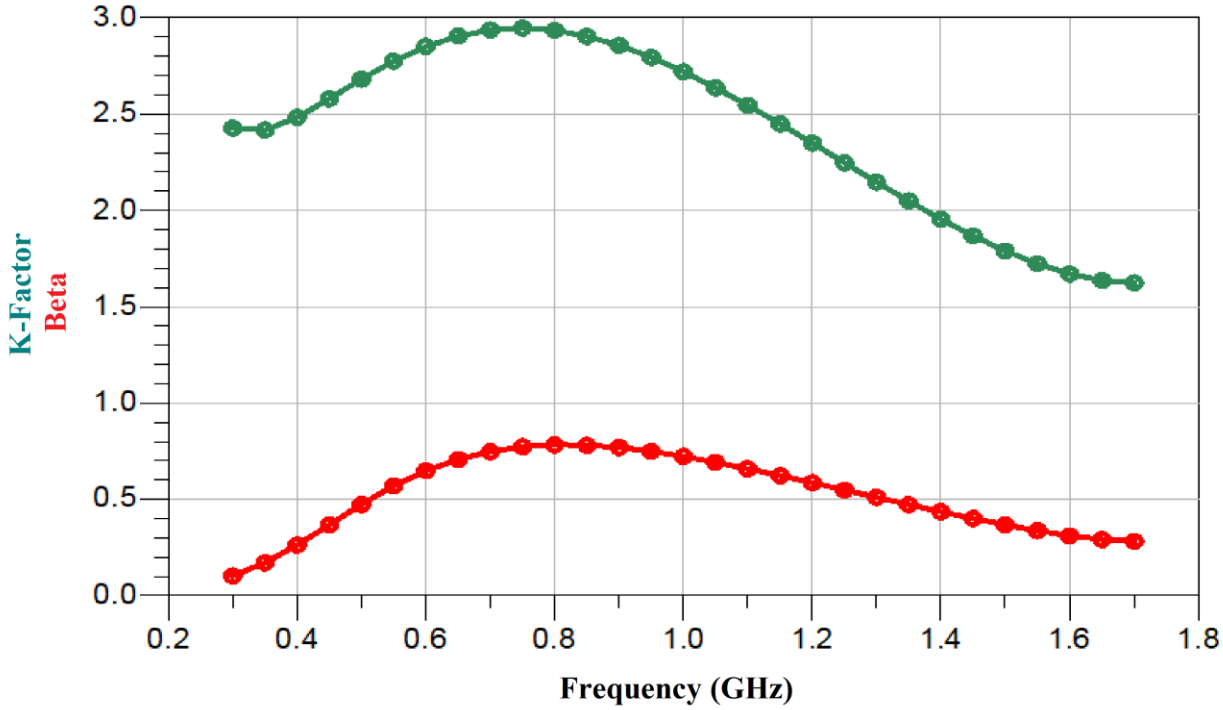


Figure 8. Stability factors of the proposed DPA

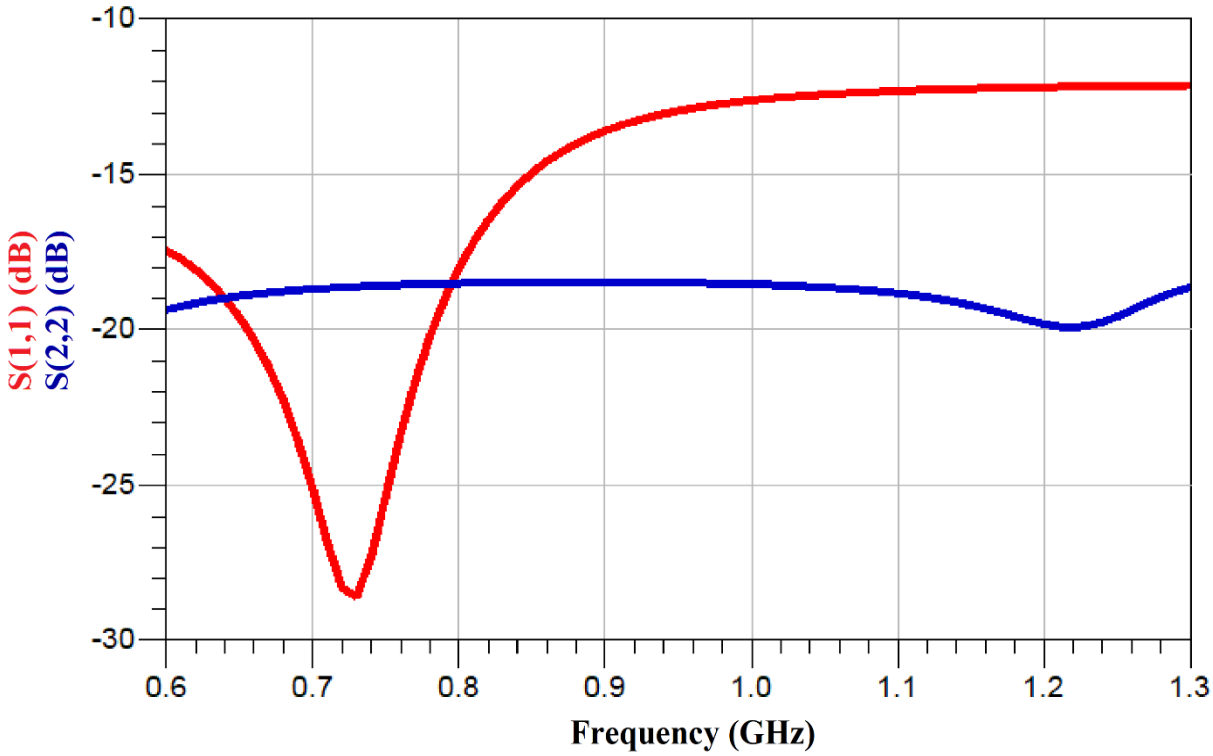


Figure 9. S_{11} and S_{22} of the proposed DPA

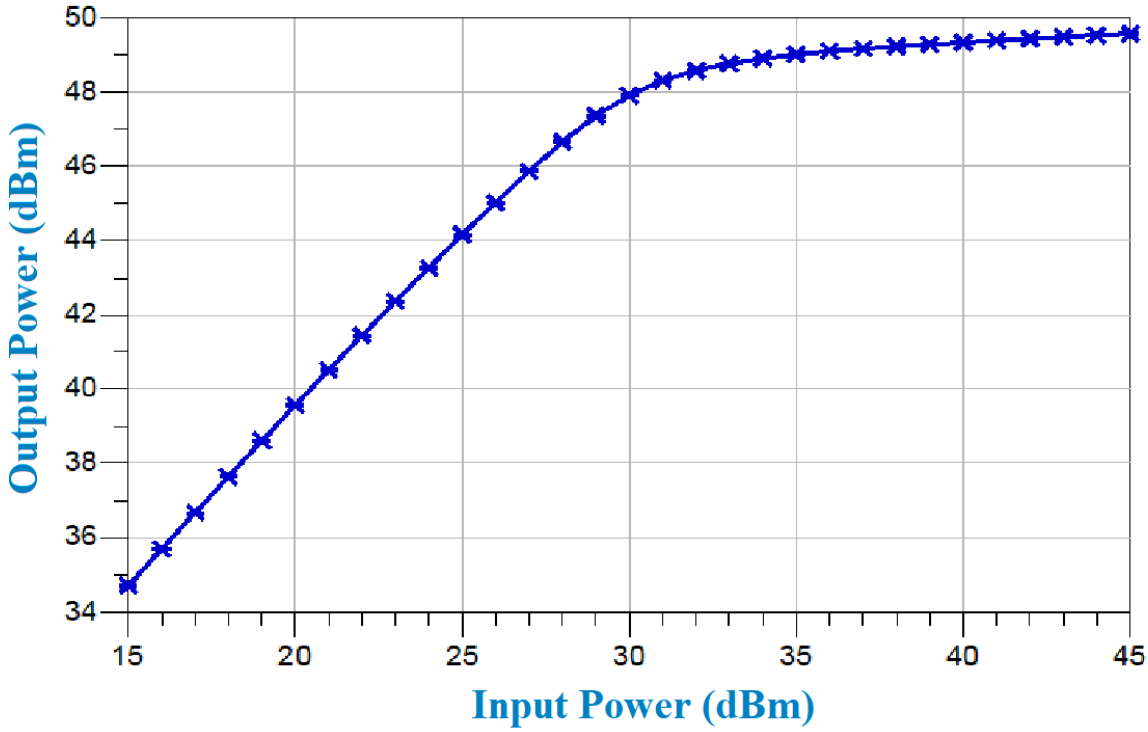


Figure 10. Output power of the proposed DPA (Layout test)

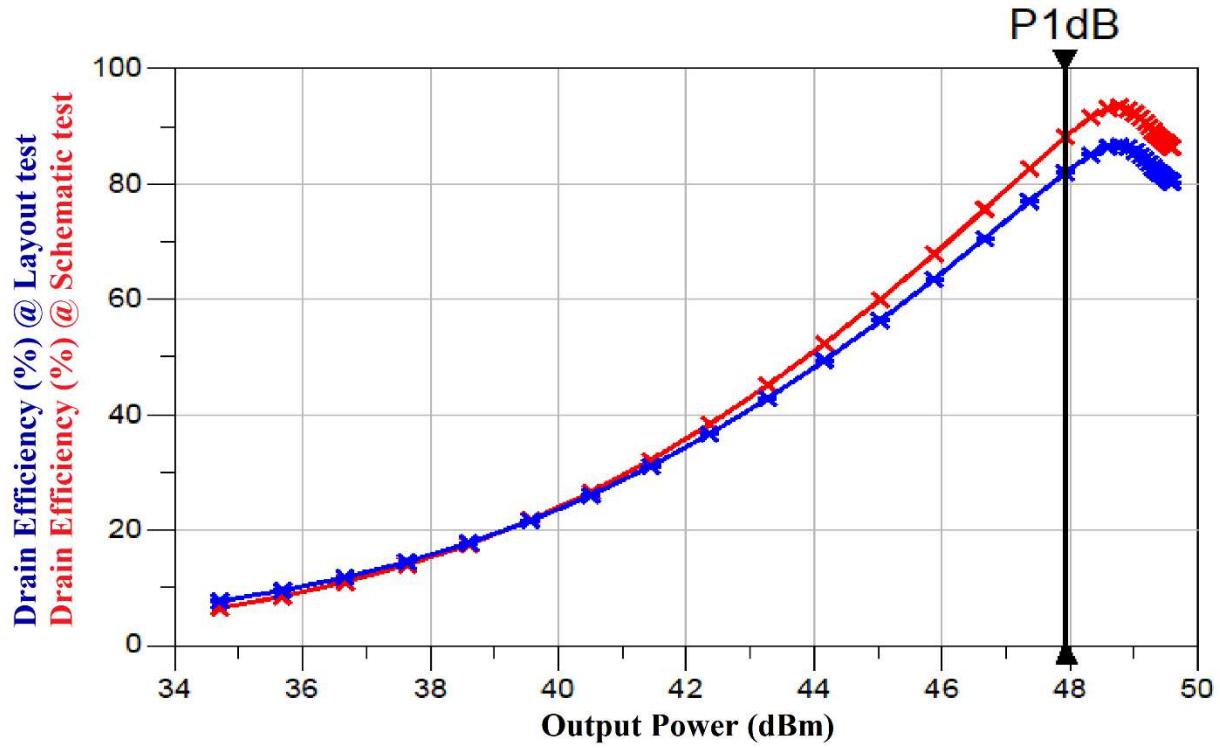


Figure 11. Drain Efficiency of the proposed DPA

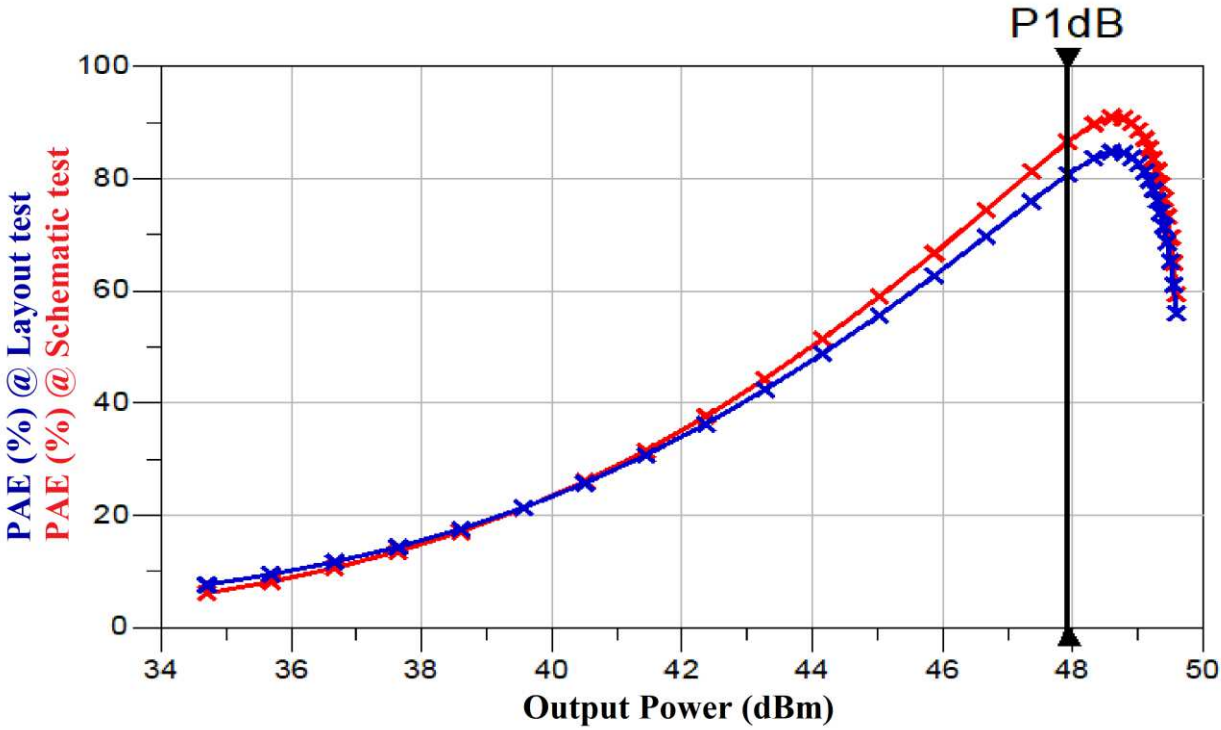


Figure 12. PAE of the proposed DPA

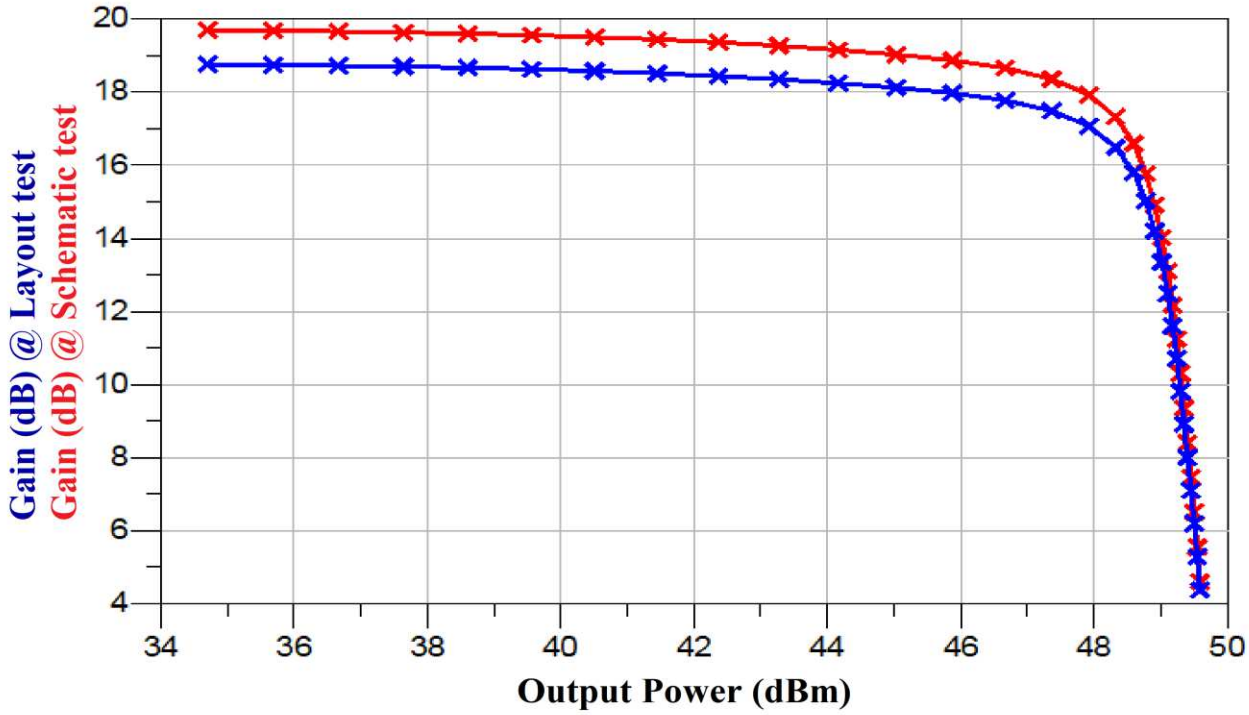


Figure 13. Gain of the proposed DPA

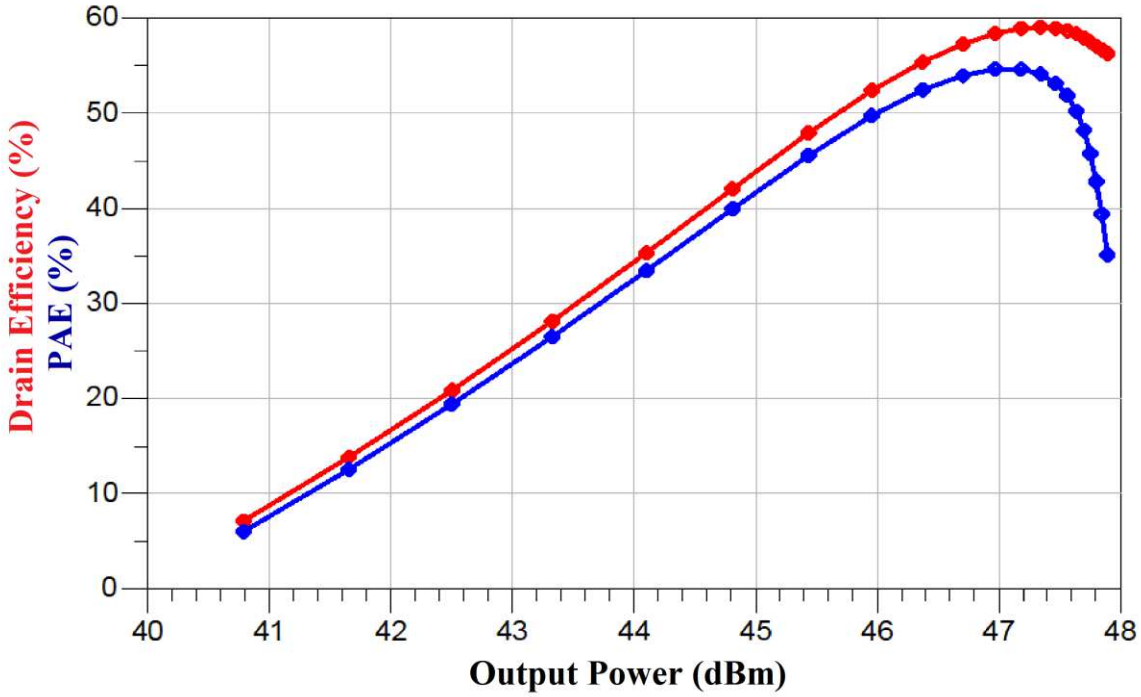


Figure 14. PAE and Drain Efficiency of the proposed Main PA (Class-AB)