Optimization of Heat Transfer Process in Double Gate MOSFET Using Modified BDE Model

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Abstract

In this paper, a nonlinear electrical model is derived and is used to calculate the electric field and the current density. To corroborate our electrical model, it was compared to TCAD simulator. It was shown that the proposed model captures the current density with a good degree of agreement with TCAD simulator. The electrical model is given by the modified Drift-Diffusion (D-D) model coupled with the Ballistic-Diffusive Equation (BDE) which is able to predict the heat transfer phenomenon in the nanoscale regime. The thermal device performance is then investigated by varying device parameters including gate and drain biases with implementation of different gate dielectric to explore its response on thermal characteristics. It was further shown that the proposed electro-thermal model is able to predict the nano heat conduction in (DG) nanostructure devices. In addition, it is shown that the heat flux process could be controlled by adjusting the drain and gate voltages.

KEYWORDS: Nanoscale heat transport; high-k dielectric; Nano FET; heat dissipation

1) INTRODUCTION

Multi-Gate Metal Oxide Semiconductor Field Effect Transistors (MG-MOSFET) such as Double Gate FET have considered one of the most promising contenders in the semiconductor industry [1-4]. The progressive downscaling of multi-gate MOS structures has led to many problems concerning their electrical and thermal performance [5-9]. There are many challenges for the Double Gate-MOSFET transistor such as the short channel effect [10-12], the heat flux and the temperature inherent the channel region of the transistor [13-16].

In order to overcome these technological defies several numerical and experimental works have been done in recent years. Kown et al. [12] have studied the effect of negative capacitance (NC) in Fully Depleted Silicon-On-Insulator (FD SOI) transistor reliability. They have demonstrated that an improved short channel performance was obtained due to the reverse drain induced barrier lowering characteristics of the NC operation. To better control the short channel effect, Wenstead et al. [11] have combined a thin SiGe channel with a non-band edge gate electrode. They found that this approach effectively solve some of the difficult associated technological challenges. The short-channel scaling of ultrathin SOI MOSFETs was analyzed by the generalization of 2-D numerical simulations by Xie et al. [17]. They found that, like a bulk MOSFET, the short-channel effect of an SOI MOSFET can be described by a scale length. As well, they proposed that the short-channel effect of SOI MOSFETs can be improved by applying a reverse bias to the substrate to push the inversion channel from the back surface to the front. Further, Chen et al. [18] have studied the electro-thermal effects on hot-carrier injection (HCI) in 100-nm silicon-on-insulator (SOI) MOSFET for a digital integrated circuit. They proved that the buried oxide layer leads to a high temperature in the channel and deteriorates the HCI. In their reports, Swahn and Hassoun [19] have studied the self-heating in multi-fin devices by the development of thermal models for single-fin flared channel extension and for multi-fin devices. To measure the device thermal robustness, they have developed a metric for electro-thermal sensitivity.

To better predict the thermal transport in nano-transistors, we are obliged to replace the Fourier Law, which is invalid in the nanoscale regime [19]. Instead, Tzou [19] proposed a new thermal model which is able to predict the heat conduction in the nanoscale regime. From the Boltzmann transport equation, Chen [20] has developed a new model named, Ballistic Diffusive Equation (BDE), which represents a good approximation for the heat conduction in the nanoscale regime.

In order to improve the electrical properties of nano DG-MOSFETs, many works have used the high-k dielectric material as a gate oxide such as TiO_2 [21], Al_2O_3 [22] and HfO_2 [23].

In this report and in order to improve the electro-thermal effects of a 22nm DG MOSFET, we have used a nonlinear transient analysis model, which can be used to investigate phonon scattering and electron transports in a 22 nm DG-MOSFET. We report the drain-source and gate-source voltage effects and high-k dielectric material role on increasing the operation temperature in the analyzed structure. In the first step, we have compared the transfer characteristics and the temperature evolution given by the proposed model with those available in the literature. Then, we have studied the effect of HfO_2 gate oxide on the electro thermal properties of the proposed structure.

2) THEORY AND FORMULAS

In order to predict the electro-thermal properties of the proposed structure, we have used a transient nonlinear electro-thermal model. To compute the heat generation rate $Q = \vec{J} \cdot \vec{E}$, an electrical model given by the electron and hole continuity equations and Poisson equation was used.

When the Fourier low ceases to be valid, we use a thermal model, which can be valid in nanoscale regime. In this work, we have used the DPL model.

A. Continuity and Poisson equations

To predict the electric characteristics of MOS structures, the well-known electron and hole continuity equations coupled with Poisson's equation have been used. Electrons and holes transport equations are given by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla . (J_n) - (R - G) \tag{1}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla.(J_p) - (R - G) \quad (2)$$

Where n and p are the electron and hole concentration respectively. J_n and J_p are the electron and hole current densities.

$$\overline{J}n = qn\mu_{eff}\overline{E} + q\,Dn\overline{\nabla}n \quad (3)$$

$$\overline{J}p = qp\mu_p\overline{E} + q\,Dp\overline{\nabla}p \quad (4)$$

Where μ_n and μ_p are the electron and hole mobilities and (R-G) is the generation-recombination rate. In this work, this quantity is given by:

$$(R - G) = \frac{np - n_0^2}{\tau_n(n + n_0) + \tau_p(p + p_0)}$$

where p_0 and n_0 are the intrinsic carrier concentrations, τ_n and τ_p are the electron and hole lifetimes. In this work, in order to be close to the reality, μ_n and μ_p are given by [24]:

$$\mu_{eff} = \mu_0\left(\frac{T}{T_0}\right)^{-\gamma} \quad (5)$$

The typical value of $\gamma = 1.5$ [25].

The threshold voltage used in our simulation is given by:

$$V_T = V_T(T_0) - k(T - T_0) \quad (6)$$

where T_0 = 300 K, k is the threshold voltage temperature coefficient (a typical value is 2.4 mV/K) [25].

To analyze the electric potential in the proposed structures, we have used the Poisson equation:

$$\nabla(\varepsilon\nabla V) = -q(p - n + N_D - N_A) \tag{7}$$

where ε is the permittivity, V is the electrical potential, and N_D and N_A are the donor and the acceptor concentrations. The electric field is related to the electric potential by a gradient relationship $\vec{E} = -\vec{\nabla}V$.

B. BDE model and heat conduction equation

The heat transfer equation related to the BDE model is expressed as follows [19]:

$$\tau_R \frac{\partial^2 T(r,t)}{\partial t^2} + \frac{\partial T(r,t)}{\partial t} = \frac{\kappa}{C}\nabla\nabla T(r,t) - \frac{\nabla q_b(r,t)}{C} + \frac{\dot{q}_h}{C} + \frac{\tau_R}{C}\frac{\partial \dot{q}_h}{\partial t} \tag{8}$$

where Q represents the volumetric heat generation rate due to the Joule effect, τ_R is the phonon relaxation time, K_{eff} is the effective thermal conductivity and C represents the volumetric heat capacity. The volumetric heat source Q is determined by modified D-D model and it's given by [9]:

$$Q = \vec{J}.\vec{E} + (R - G).(E_g + 3K_B T) \tag{9}$$

where K_B represents the Boltzmann constant and the band gap E_g is given by:

$$E_g = E_{g0} - 6.5 \cdot 10^{-4} \cdot \frac{T^2}{T + 200} \tag{10}$$

in which E_{g0} (eV) denotes the band gap at ambient temperature.

C. Structures and Boundary conditions

In practice, a SiO_2 layer encounters the left and the right sides of the transistors and the ambient temperature is T_0=300 K. For this reason; $\partial n/\partial y = \partial p/\partial y = \partial V/\partial y = \partial T/\partial y = 0$

The drain boundary side is given by the V_{DS} voltage, V_{GS} is applied on the gate side and at the source side $V_{ss} = 0$.

A 22 nm Symmetric Underlap DG MOSFET is selected for nano electro-thermal simulation to predict its thermal stability. The 22 nm DG MOSFET structure under investigation is shown in **Fig. 1a**.

In their report, Chattopadhyay et al. [27] gives all the parameters of the analyzed devices. The height of the SiO_2 interfacial layer was about 0.45 nm and the height of the HfO_2 layer was about 1.9 nm. In order to provide higher physical gate height to the device, the HfO_2 layer is placed over the SiO_2 layer [27]. We validate the electric part of the proposed model with data obtained from Chattopadhyay et al. [27]. For this reason, the underlap length of the structure is 8 nm, the gate height is about 10nm and the Si thickness is 20 nm. To validate the thermal part of the proposed model, we have compared the temperature and the heat flux distributions with those obtained in a 22 nm FD-SOI MOSFET given in **Fig. 1b**.

The buried oxide (BOX), source and drain doping zone widths are 10 nm. The equivalent oxide thickness used in this comparison is 0.9 nm. Furthermore, the two analyzed structures are based on, Silicon, Silicon dioxide and Hafnium dioxide materials. To perform the numerical simulation, the group velocity, the phonon mean free path thermal conductivity and volumetric heat capacity parameters of Si, SiO_2, and HfO_2 are shown in **Table. 1** [28].

3) RESULTS AND DISCUSSION

To validate the electrical part of the present model, we show in **Fig. 2 a** comparison of the output characteristics for V_{DS}=0.85V.

It is obvious that the electrical current obtained by the simulations have the same characteristics as the data obtained using TCAD simulation [27].

Fig. 3 shows a comparison of the temporal temperature profile in the centerline of the analyzed 22 nm DG-MOSFET and FD-SOI MOSFET at V_{GS}=V_{DS}=0.8V. It is clear that after 10ps, the temperature has achieved the saturation in the FD-SOI MOSFET case and the linear regime occurs during this period for the DG-MOSFET case. These curves show that in the DG-MOSFET structure, phonon scattering and phonon collisions phenomena between the two up and bottom interfaces gives the unsaturation phenomena and the exponential increase of the temperature. This phenomenon not seen in the FD-SOI-MOSFET case due to the single Si/SiO_2 interface, where the phonon scattering is neglected.

From **Fig. 3**, at t=50 ps, we show also that the operation temperature is 318 K for the FD-SOI MOSFET case at and 312 K for the studied transistor (DG-MOSFET). **Fig. 4** represents the operation temperature versus drain bias at V_{GS} = 0.9 and t=50 ps. It can be seen that the operation temperature increases exponentially with the drain-source voltage and it is 310 K for V_{DS} = 0.9V. The increase in the temperature is due to the fact that, when V_{DS} is increased, there is an increase in the drain current and the current density. This leads to an increase of the Joule effect given by $\vec{J} \cdot \vec{E}$. We observe also an increase of the operation temperature, due to the increase of the drain bias.

In **Fig. 5** the operation temperature profile versus gate bias at V_{DS} = 0.9V and t=50 ps, was presented. It is clear that the temperature increases until V_{GS} reaches around 0.55 V. Beyond V_{GS} = 0.55 V, the temperature continues to decrease with an increase of the gate-source voltage.

Fig. 6 shows the temporal temperature profile in the centerline of the analyzed structure with different drain–source voltage at V_{GS} = 0.9 V. Fig. 6 is in concordance with **Fig. 4**. It can be seen that up to 10 ps, the temperature is almost fixed and has the same value with different values of V_{DS}. After 10 ps, the temperature increase further with the increase of the drain bias.

The effect of V_{DS} becomes obvious for t=50 ps and an increase in the temperature with a few degrees appears clearly. It should be noted that this effect is nonlinear and it is more obvious for large values of V_{DS}.

Fig. 7 represents the temporal temperature profile in the centerline of the 22 nm DG MOSFET with different V_{GS} for V_{DS} = 0.9 V. It can be seen that the temperature increases gradually with time. We show also that at V_{DS} = 0.9 V, there is operation temperature varies slightly when V_{GS} < 0.7 V. On the other hand, the temperature decreases noticeably when V_{GS} > 0.7 V. It appears clearly that the effect of V_{GS} on the temperature is also nonlinear. The operation temperature achieves the value of 314 K for V_{GS} = 0.2 V and 310 K for V_{GS} = 0.9 V.

Fig. 8 shows the heat flux and the temperature distribution profiles along Y-axis in the centerline of the analyzed DG-MOSFET at t = 50 ps and V_{GS} = V_{DS} = 0.9 V. It is clear that the heat flux is higher in the oxide/semiconductor interfaces and it decreases sharply until it has achieved a constant value in the substrate zone. We show also that the temperature keeps a constant value between the two oxide/semiconductor interfaces. However, an important increase of the temperature was observed by crossing the interfaces. This is due to the phonon walls collisions and phonon scattering between the two walls (oxide/semiconductor interfaces) of the analyzed structures. The diffusion of the heat inside the device mitigates the maximal temperature achieved.

Fig. 9 depicts a comparison of the temporal temperature evolution in the centerline of the transistor with and without high-k dielectric material using V_{GS} = V_{DS} = 0.9 V. It appears clearly that the temperature evolution keeps the same trend with different amplitudes. At t= 50 ps, the achieved temperature was 315 K, when we use only the SiO2 dielectric gate oxide. When a coupled oxide (SiO2+ HfO2 layers) was used, the temperature achieved was 310 K.

Besides, when a layer of HfO2 was involved, the lateral heat conduction was modified and consequently, the maximal temperature reached is affected.

In Fig. 10, a comparison of the temperature profile versus Y-axis with and without HfO_2 oxide layer at $V_{GS} = V_{DS} = 0.9$ V and t = 50 ps was presented. It can be seen that the temperature is almost constant at the value 314 K when a single oxide layer (SiO_2) is employed. In contrast, when the two layers of HfO_2 and SiO_2 are used, the temperature decreases and a value of 310 K was achieved between both channel regions.

Fig. 11 shows a good agreement with **Fig. 9** and **Fig. 10**. In this figure, we present the temporal heat flux evolution in the centerline of the analyzed structure with and without the HfO_2 second oxide layer. It can be seen that the use of the HfO_2 has an important role in order to decrease the heat flux in the centerline and thereafter in the whole of the transistor. The degradation of phonon transports are due to the fact that the use of a high-k dielectric material will decrease the electric field and the current density in the channel region of the analyzed DG-MOSFET. The decrease of the electric field and the current density affects the heat source due to the Joule effect, which decreases the temperature distribution and the heat flux into the analyzed structure.

4) CONCLUSION

In summary, a comprehensive study of phonons and electrons transport in a 22 nm DG MOSFET transistor by using a nonlinear electro-thermal model was successfully reported. We found that the phonon transports and following that the temperature distribution can be controlled by adjusting the drain-source and gate-source voltages in nanotransistors. In a technological viewpoint, the important increase of the operation temperature in the analyzed DG-MOSFET remains lower than that given in a 22 nm FD-SOI-MOSFET. Indeed, we have

also demonstrated that phonon scattering in the DG-MOSFET, (between two oxide/semiconductor interfaces), is considerably influenced by adding the HfO_2 layer. The use of a High-k dielectric layer decreases considerably the phonon transport in nanodevices which is necessary to limit the self-heating mechanisms.

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Table:

Symbol	V(m/s)	Λ (nm)	λ ($Wm^{-1}K^{-1}$)	C($Jm^{-3}K^{-1}$)
Si	3000	100	150	$1.5 \cdot 10^6$
SiO2	5900	0.4	1.4	$1.75 \cdot 10^6$
HfO2	5924	-	2.3	$2.6 \cdot 10^6$

Table 1: Thermal properties of Si, SiO_2 and HfO_2 materials

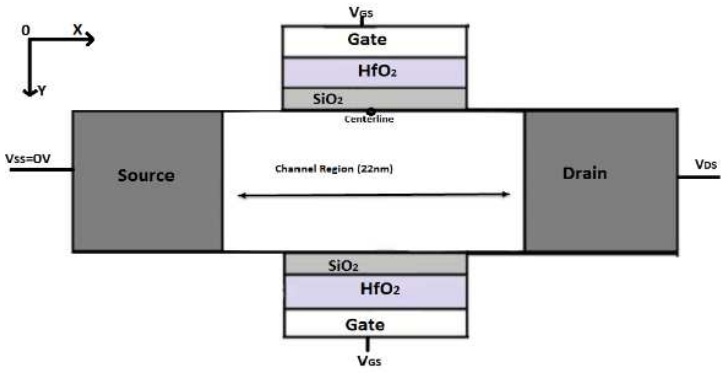

Fig. 1a. Schematic view of 22nm DG MOSFET.

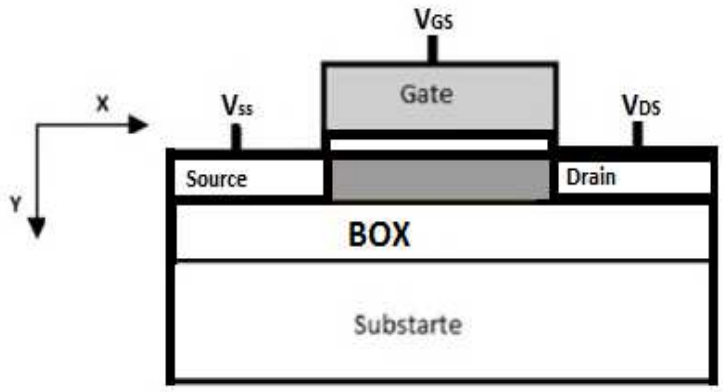

Fig. 1b. Schematic view of 22nm FD-SOI-MOSFET.

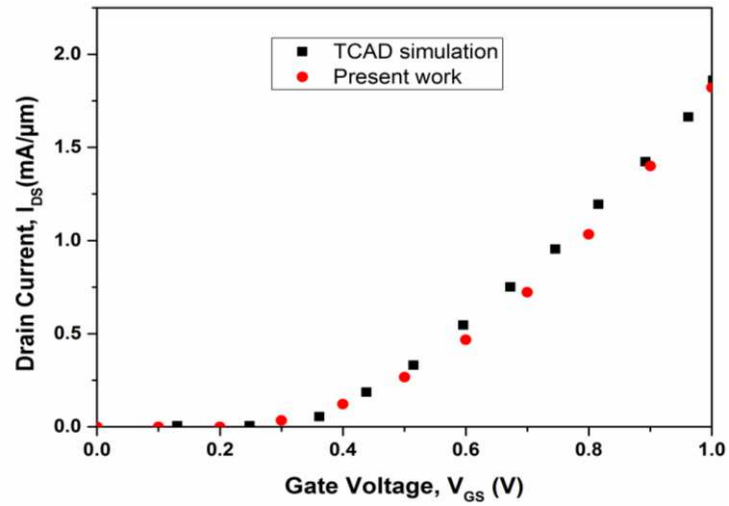

Fig. 2. Transfer characteristics of 22 nm DG MOSFETs compared to TCAD numerical simulation at V_{DS}= 0.85V.

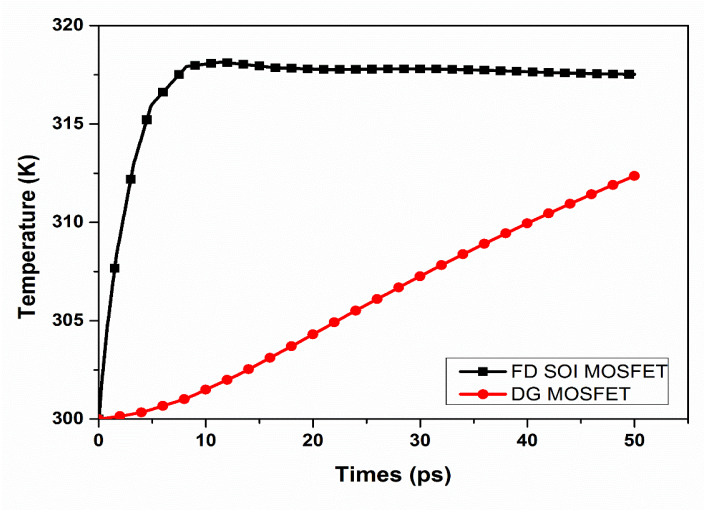

Fig. 3. Comparison of temporal temperature profile of 22 nm FD SOI MOSFET and 22 nm DG MOSFET at $V_{GS}=V_{DS}=0.8V$.

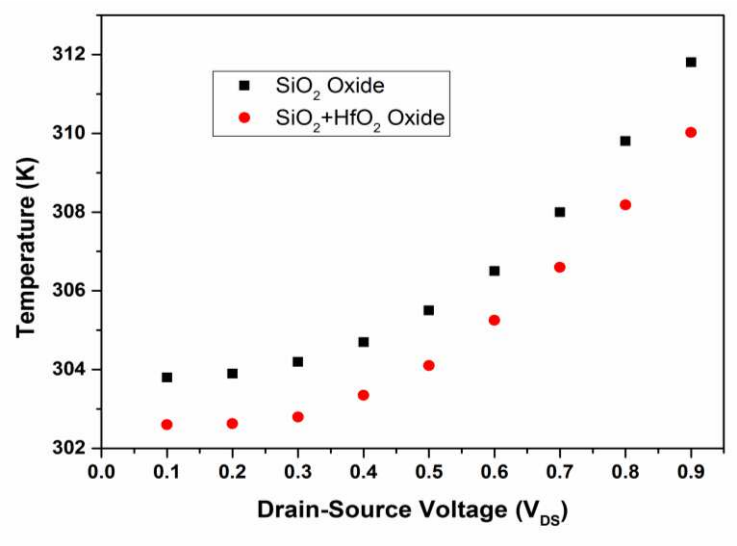

Fig. 4. Temperature versus drain-source voltage in the centerline of the 22nm DG MOSFET with and without HfO_2 oxide at V_{GS}=0.9 V and t=50.

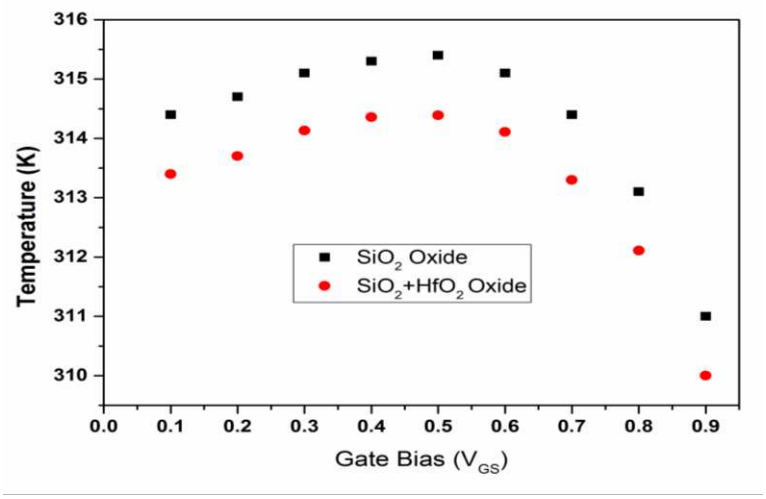

Fig. 5. Temperature versus gate bias in the centerline of the 22nm DG MOSFET with and without HfO_2 oxide at V_{DS}=0.9 V and t=50 ps.

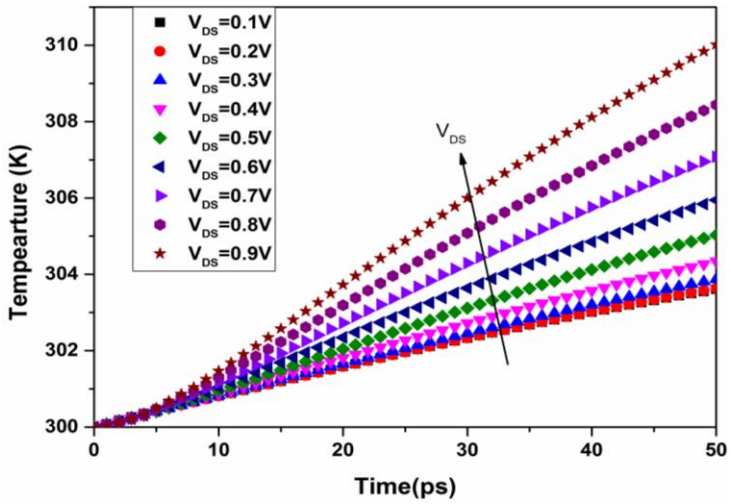

Fig. 6. Temporal temperature profile in the centerline of the transistor with different V_{DS} at V_{GS}=0.9V.

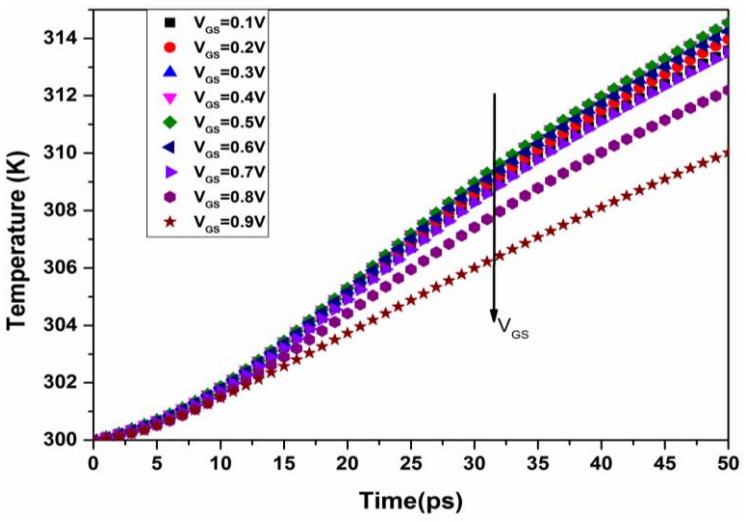

Fig. 7. Temporal temperature profile in the centerline of the transistor with different gate bias at V_{DS}=0.9V.

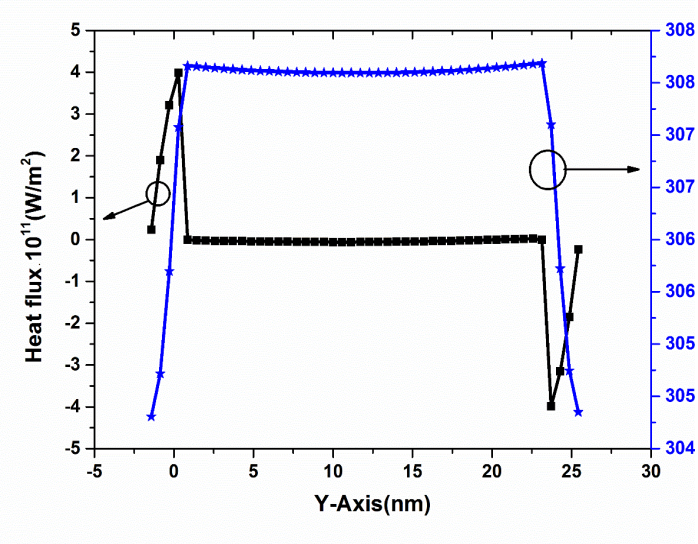

Fig. 8. Heat flux and temperature profile in the centerline of the transistor along Y-axis at t=50 ps

V_{GS}=V_{DS}=0.9V.

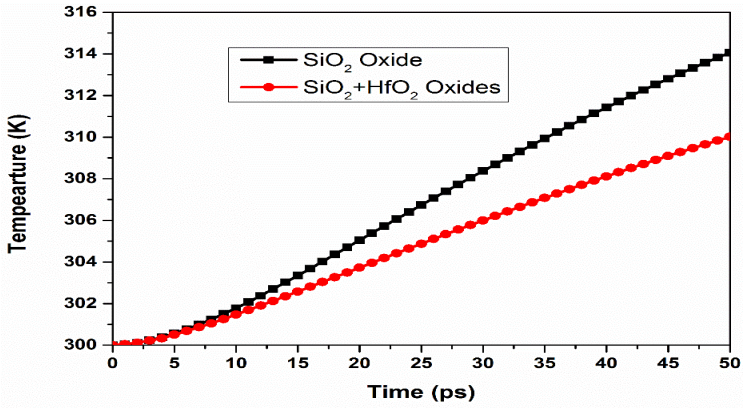

Fig. 9. Comparison of the temporal temperature evolution in the centerline of the transistor with and without HfO2 oxide at VGS=VDS=0.9V.

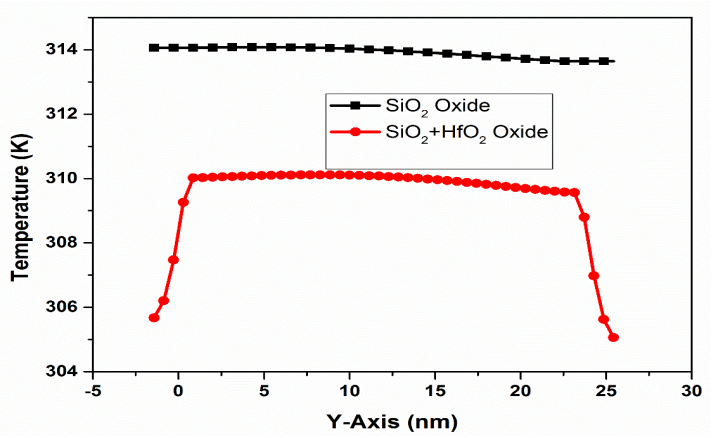

Fig. 10. Comparison of the temperature profile versus Y direction in the centerline of the transistor with and without HfO_2 oxide at t=50 ps and $V_{GS}=V_{DS}=0.9V$.

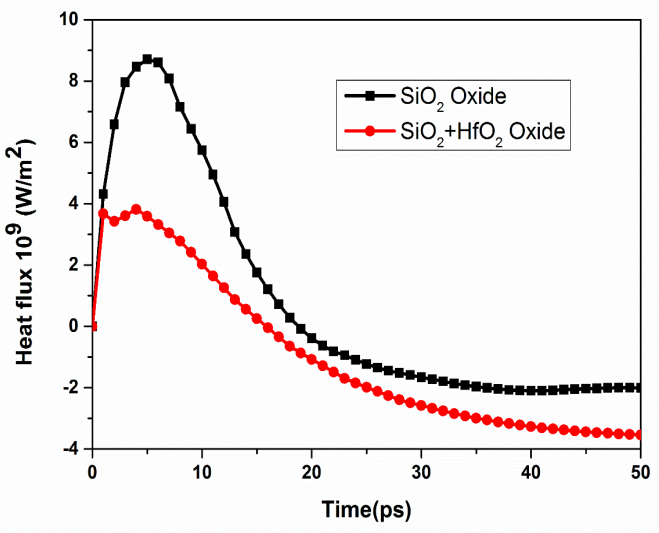

Fig. 11. Comparison of the temporal heat flux evolution in the centerline of the transistor with and without HfO_2 oxide at $V_{GS}=V_{DS}=0.9V$.