Wafer-scale van der Waals Dielectrics of Inorganic Molecular Crystals

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Abstract

Van der Waals (vdW) dielectrics such as hBN are widely used to preserve the intrinsic properties of two-dimensional (2D) semiconductors and support the fabrication of high-performance 2D devices. This is fundamentally attributed to their dangling-bond-free surface, carrying far lower density of charged scattering sources and trap states with respect to the conventional dielectrics (SiO_2 etc.). However, their wafer-scale fabrication and compatible integration with 2D semiconductors remain cumbersome, giving rise to the difficulties in scalable fabrication of high-performance 2D devices. Here we report a high-κ vdW dielectric (ε_r=11.5) composed of inorganic molecular crystal (IMC) Sb_2O_3, allowing for large-scale fabrication and facile integration via standard thermal evaporation process thanks to its particular crystal structure. Similarly, our vdW dielectric also supports remarkably improved 2D devices with respect to the typical conventional dielectric SiO_2. The monolayer MoS_2 field effect transistors (FET) supported by our vdW dielectric exhibits high on/off ratio (10^8), greatly enhanced electron mobility (from 20 to 80 cm^2/Vs) and reduced transfer-curve hysteresis over an order of magnitude. Our results may open a new avenue towards compatible fabrication of vdW dielectrics using IMCs and lead to the scalable fabrication of high-performance 2D devices.

Introduction

Two-dimensional (2D) semiconductors have attracted enormous research interests for their great potentials as channel materials in the next-generation field-effect transistors (FETs) with high mobility and great gate controllability at atomic thinness [1–5]. However, due to such a thinness, their electrical performance can be severely deteriorated by surrounding disorders, generally arising from chemical adsorbates and its neighboring dielectrics. Such disorders may bring charged scattering sources and trap states, resulting in the device performance inferior to their intrinsic properties [6, 7]. Since the discovery of high-quality graphene supported on hBN [6], using vdW dielectrics has become a universal approach to preserve the intrinsic properties of 2D materials [8–11] and support the fabrication of high-performance devices [7, 12, 13]. The advantages of vdW dielectrics over conventional oxides (SiO_2 etc.) substantially stem from their atomically flat surface, free of dangling bonds and with low-density disorders [6, 14–17]. In particular, the 2D FETs using vdW dielectrics exhibit excellent characteristics, including enhanced mobility and better switching stability [12, 13, 18]. However, such vdW dielectrics are prepared via either the mechanical exfoliation [12, 13] or vapor deposition growth on specially-designed substrate at high temperature [16–19], incompatible to the standard semiconductor manufacturing processes. Till now, scalable growth of such vdW dielectric materials as well as its integration with 2D semiconductors remain challenging.

Here we report a vdW dielectric film of inorganic molecular crystal (IMC) Sb_2O_3, which can be readily fabricated via standard thermal evaporation deposition (STED) process thanks to its particular crystal structure. The molecular structure is well preserved during the evaporation owing to the high molecular stability, which is confirmed by our theoretical calculations. The deposited film, free of dangling bonds,

can serve as vdW dielectrics. Its synthesis approach allows for scalable fabrication and facile integration with 2D semiconducting materials for devices fabrication at scale. To demonstrate that our vdW dielectric film similarly possess comparative advantages over the conventional dielectrics, we investigate the device performance of 2D MoS_2 FET supported on Sb_2O_3 and standard SiO_2 substrate respectively. We confirm that our MoS_2/Sb_2O_3 FETs significantly outperform the MoS_2/SiO_2 devices, including a higher on-state current, greatly enhanced electron mobility and reduced hysteresis. Specifically, our monolayer $MoS_2/Sb2O_3$ FET exhibits a high on/off ratio of 10^8 and an enhanced electron mobility of 82 cm^2/Vs at room temperature, in contrast to 20 cm^2/Vs for the same device supported on SiO_2. In addition, all the MoS_2/SiO_2 FETs demonstrate a considerable hysteresis in double-sweep transfer characteristic curves due to the trap states within the SiO_2 substrate, which turn out to be negligibly small for the MoS_2/Sb_2O_3 FETs, with a reduction of more than an order of magnitude. Based on the quantitative analysis of hysteresis, we also estimate a far lower density of trap states (nearly two orders of magnitudes) on Sb_2O_3 substrate in comparison to standard SiO_2. The scalable fabrication of vdW dielectrics via compatible integration processes is a prerequisite for the scale-up of high-performance 2D devices. Our approach of fabricating vdW dielectrics using IMCs may open up unprecedented opportunities to promote such promising 2D devices to technological applications.

Results

Our vdW dielectric film is fabricated via STED (Fig. 1a) at room temperature. We use IMC Sb_2O_3 powder as the evaporation source. It consists of ultra-small Sb_4O_6 molecules in the form of bicyclic cages (Sb-O bond length 1.98 Å) [20–22]. All the molecules are bonded together via vdW interaction (Fig. 1b). Due to such a weak intermolecular interaction, Sb_2O_3 molecules are prone to sublime at elevated temperature in high vacuum before its melting, without the breakage of the Sb-O bonds. Its evaporation temperature is measured to be around (490℃) via thermogravimetric analysis at ambient pressure (Figure S1), much lower than its melting point (656℃), which implies the sublimation process of molecules at elevated temperature (The evaporation temperature in our vacuum chamber is supposed to be much lower according to Clausius-Clapeyron relation). The molecular vapor evaporated from Sb_2O_3 powder, free of dangling bonds all around, deposit on the substrate to form a vdW substrate (Fig. 1a). Our STED process permits the fabrication of homogeneous wafer-scale film (Fig. 1c and Figure S2) and the film thickness can be precisely controlled (Fig. 1d and Figure S2). Atomic force microscopy (AFM) is used to characterize the morphology of our film. It reveals its great homogeneity and flatness of our deposited film in micro-metric scale, without discernible voids or bumps (Fig. 1e and f). The homogeneity of morphology and elemental distribution are also confirmed by scanning electron microscope (SEM) and elemental maps of energy-dispersive X-ray spectroscopy (EDS) (Figure S3).

To confirm the molecular structure of our deposited film, Raman spectroscopy is employed to probe the vibrational modes of the molecules. We find that all the Raman peaks of Sb_2O_3 film can be assigned to the intra-molecule Raman mode (see Table S1) and match well with those of Sb_2O_3 powder used as the

deposition source, implying that Sb_2O_3 evaporates in the form of molecular vapor with the molecular structure preserved. The stability of Sb_2O_3 molecules can be confirmed from the perspective of theoretical calculations via investigating the vacancy formation energy within the molecule. The formation energies of typical O, Sb, and double O vacancy are all found to be over 5 eV (Table S2), indicative of a robust molecule without the formation of vacancies and dangling bonds. Moreover, we investigate our eventual Sb_2O_3 film with X-ray diffraction (XRD), high-resolution transmission microscopy (HRTEM) as well selected-area electron diffraction pattern (SAED), which further reveal the polycrystalline structure of our Sb_2O_3 film(Figure S4). It is worth noting that the benign grain boundaries in our Sb_2O_3 film generally are free of dangling bonds [23], which in principle would not introduce effective defects into the dielectric.

We now investigate the dielectric properties of our Sb_2O_3 film. To determine its band gap, a 40 nm Sb_2O_3 film is deposited on glass substrate for absorption spectroscopy measurement (see Methods). The band gap of Sb_2O_3 film is determined to be 3.95 eV from its absorption spectrum (Fig. 2a), in good agreement with its density of states (DOS) distribution (Fig. 2b). Such a wide band gap renders our Sb_2O_3 film an insulator, as ascertained by the conductive test of a two-terminal device (Fig. 2c). Its resistivity of over 10^9 Ω•cm at 300 K can be extracted from its I-V curve (Fig. 2c). To test its breakdown electric field, Sb_2O_3 film is sandwiched between two electrodes (Figure S6). As demonstrated in Fig. 2d, the breakdown voltage of our Sb_2O_3 film can be estimated to be 180 MV/m, comparable to that of SiO_2.

In order to determine the dielectric constant of Sb_2O_3, we fabricate a series of parallel-plate capacitors, using Sb_2O_3 of 300 nm as the dielectric sandwiched between degenerately doped Si substrate and metal pads. The capacitance with respect to area S are measured at increasing frequency are respectively measured (Fig. 2e inset). We then extract the static capacitance at low frequency (10 kHz) and estimate the capacitance per unit area to be C = 0.34 nF/mm^2. The relative dielectric constant of our Sb_2O_3 film then can be calculated to be $\varepsilon_r = 11.5$ via the formula $C = \varepsilon_r\varepsilon_0/d$ where ε_0 is dielectric constant of vacuum and d is the thickness of Sb_2O_3 film. The measured dielectric constant of our Sb_2O_3 matches well with the reported value [24]. In addition, such a high dielectric constant is comparable to typical high-κ dielectric Al_2O_3. As the low dielectric constant of hBN (~ 5 [12]) is one of its limitations in the FET application, our Sb_2O_3 vdW dielectric, in contrast, possesses the highest dielectric constant in all the reported vdW dielectrics (Figure S7).

In analogy to typical vdW dielectric h-BN, our Sb_2O_3 film of molecular crystal is free of dangling bonds, naturally holding low-density charge scattering centers and charge trap states. Our vdW film can potentially support high-performance 2D electronic devices of higher mobility and smaller hysteresis as well. To demonstrate its advantages in this regard, we fabricate 2D FETs respectively on our Sb_2O_3 vdW substrate and standard SiO_2 substrate, then systematically investigate their temperature-dependent device characteristics.

The well-studied 2D semiconductor MoS_2 is chosen as the representative channel materials and all the FET devices are fabricated using the same processes (see Methods). For a clear comparison, our Sb_2O_3 substrate is composed of 40-nm film deposited on the standard SiO_2/Si substrate to fully screen the charged center and trap states on SiO_2 substrate (Fig. 3a). 2D MoS_2 flakes are prepared via mechanical exfoliation and transferred onto the substrates. Their thickness are confirmed via optical measurement (Figure S8) and AFM (Figure S9a and b) before the device fabrication. Degenerately doped Si serves as FET back gate in our measurement (Fig. 3a). To minimize the effect of contact resistance in our devices, we use In/Au metal to form low-resistance contact with MoS_2 [25]. Moreover, we also degas all the devices in high vacuum (10^{-6} torr) for 3 hours to reduce air adsorption on our device surface before the tests are carried out [26]. The FET based on monolayer MoS_2 supported on Sb_2O_3 substrate is demonstrated in Fig. 3b.

For monolayer MoS_2, the band offsets at valance band maximum (VBM) and conduction band minimum (CBM) can be estimated from its band alignment to Sb_2O_3 (the vacuum level at 0 eV while the well-known VBM and CBM of MoS_2 are extracted from reference [27]) (Fig. 3c). These band offsets over 1 eV effectively confine the charges within the MoS_2 channel during the device measurement. The Ohmic contact of electrodes to 2D MoS_2 and great gate control of our FET can be verified from the linear output curves (I_{ds}-V_{ds}) both at 40 K (Fig. 3d) and 300 K (Figure S9c). From the typical double-sweep transfer characteristics curves (I_{ds}-V_{gs}) of monolayer MoS_2/Sb_2O_3 FET measured at 40 K(Fig. 3e), we observe a negligibly small hysteresis window (sweep rate in all our measurements ~ 1 V/S) and estimate the electron mobility μ_{FE} at the linear range to be over 80 cm^2/Vs (see Methods). In contrast, monolayer MoS_2 FET on SiO_2 exhibits a considerable hysteresis and much lower mobility (~ 20 cm^2/Vs) despite the same device fabrication processes and measurement conditions (Figure S13). For a clear comparison of dielectric effect (Sb_2O_3 and SiO_2) on FET mobility, we plot together their electron mobility at various gate voltage (V_{gs}) (Fig. 3f). The maximum electron mobility appears at around V_{gs} = 50V, corresponding to the charge carrier density $n = 4.0 \times 10^{12}/cm^2$ (see Methods), in agreement with the reported MoS_2 FETs [25]. The FET mobility monotonically decreases at higher temperature for our devices (Fig. 3g), presumably due to rising phonon scattering. In comparison to the reported measurements at room temperature, our monolayer MoS_2/Sb_2O_3 FET exhibits a mobility μ_{FE} of over 70 cm^2/Vs, even higher than the reported value of MoS_2 supported on hBN [12, 16] (Fig. 3g).

Similar contrast experiments are also carried out using few-layer MoS_2 as channel materials. The thickness-dependent mobility of supported different substrates are measured at various temperature (Fig. 3g). The comparative advantages of our vdW substrate for thicker MoS_2 can also be clearly identified though the mobility improvement becomes less apparent, by a factor of 2 (from 40 cm^2/Vs on SiO_2 to 90 cm^2/Vs on Sb_2O_3 for trilayer MoS_2 at 40 K). This is generally attributed to the rise of screening effect for thicker MoS_2 to the charged disorders on the underlying dielectric. Interestingly, the MoS_2 thickness more sensitively affect the mobility for the SiO_2 supported devices (mobility changes by

a factor of 2 for monolayer and trilayer MoS_2) while MoS_2 of various thickness on Sb_2O_3 demonstrate similar mobility (see Fig. 3g). This also implies the low-density of disorders on our Sb_2O_3 substrate, without apparent scattering to the carrier transport of all the MoS_2 channel.

We now focus on the hysteresis of our MoS_2 FET to investigate the charge trapping states of our vdW Sb_2O_3 and SiO_2 substrates. The hysteresis of transfer characteristic curves features the instability of a FET at work, usually caused by the trapping states located in channel semiconductors, dielectric and at their interface [28]. Using vdW dielectric has been proved effective to minimize the hysteresis of 2D semiconductor FETs [12, 29]. In Fig. 3e, we already demonstrated the ultra-small hysteresis in the double-sweep transfer curves. Such a small hysteresis demonstrate a clear contrast to that obtained from a typical SiO_2-supported monolayer MoS_2 FET (Fig. 4a). The variation of the onset voltage ΔV_{on}, which is usually used to quantify the FET hysteresis, reduces over an order of magnitude from 5.1 V for MoS_2/SiO_2 to 0.24 V for MoS_2/Sb_2O_3 FET at 40 K. We also investigated the temperature-dependent transfer characteristics of our FET (Fig. 4b and d). We firstly note that the onset voltage (V_{on}) position apparently shifts toward lower voltage with the increasing temperature, presumably resulted from the Fermi level downward shift due to rising thermal excitation in MoS_2, in agreement with the reported works [30, 31]. As to the amount of hysteresis ΔV_{on}, the temperature variation from 40 K to 300 K leads to a slight increase of hysteresis for MoS_2/Sb_2O_3 FET. Such a small dependence implies to a low density of effective trap states within our Sb_2O_3 dielectric as the hysteresis is generally induced by the charge carriers trapped into the trap states during the FET on/off switching (Fig. 4). In contrast, the hysteresis of monolayer MoS_2/SiO_2 FET sensitively depends on the temperature (Figure S13). The double-sweep transfer curves exhibit a large hysteresis window at 300 K and its ΔV_{on} reaches 12 V. This observation accordingly points to a high density of trap states on SiO_2 substrate, which can even be thermally activated at higher temperature [31].

To confirm the source of trap states, we also investigate the thickness-dependent hysteresis of MoS_2 FETs. For all the MoS_2/Sb_2O_3 FETs at various temperature, the transfer characteristic curves exhibit small hysteresis window and ΔV_{on} negligibly depends on MoS_2 thickness (Fig. 4d). Such an observation implies that the trap states are not caused by the bulk defects in MoS_2 considering that the density of such trap states are in principle thickness-dependent. For MoS_2/SiO_2 FETs, as one can anticipate, the hysteresis demonstrates no obvious dependence on MoS_2 thickness but increases considerably with temperature due to the thermal activation of trap states at higher temperature. As our Sb_2O_3 substrates are exposed in air for long time (a few days), air adsorption onto our Sb_2O_3 film may introduce some the trap states and leads to the hysteresis [25]. Our experimental results, however, ruled out this possibility. It turns out that the typical gas can hardly adsorb onto Sb_2O_3 molecules, as revealed by our theoretical calculations owing to its inert surface (see Table S3).

In order to quantitate the trap states density on Sb_2O_3 and SiO_2 substrates, we investigate the variation of threshold voltage ΔV_{th} in double-sweep transfer characteristic curves, which correlates to the charge of trap states density ΔQ according to $\Delta V_{th} = \Delta Q \times C$ [28], where C and ΔQ respectively stand for the gate capacitance and trapped charges. The values of ΔV_{th} for all our MoS_2/Sb_2O_3 devices can hardly be precisely extracted by linearly extrapolating the transfer curves due to the almost negligible hysteresis window (see Fig. 3e, Figure S9 d). We estimate ΔV_{th} for monolayer MoS_2/Sb_2O_3 device to be lower than 0.1 V without observable dependence on temperature, thus corresponding to a trap states density of $6.9 \times 10^9/cm^2$. In contrast, the trap states density on SiO_2 demonstrates a trap charge states of 4V at 40 K. It furthermore increases to 9V at 300 K under thermal activation, corresponding to a trap states density $4.3 \times 10^{11}/cm^2$, which matches well with the reported value extracted from $MoTe_2$ FET [28]. We thus confirm a remarkable reduction of trap states by nearly two orders of magnitude for our Sb_2O_3 substrate with respect to SiO_2.

Our approach substantially relies on the particular structure of Sb_2O_3 and its excellent insulating properties. Our results may merely open up the opportunities for the scalable fabrication of vdW dielectrics via compatible processes. Evidently, such an approach of compatible fabrication is not limited to the Sb_2O_3, but applicable to other IMCs. In this regard, it would be of great interest to explore other IMCs (for instance with large bandgap and higher dielectric constants). As to our Sb_2O_3 film, the fabrication process can still be optimized via the modulation of substrate temperature and deposition rate in more advanced deposition systems. For instance, the deposition at low temperature may lead to formation of amorphous Sb_2O_3 film, which may furthermore modulate the film morphology (such as film roughness) as well as dielectric properties.

As a representative example, the monolayer MoS_2/Sb_2O_3 FETs demonstrated a mobility enhancement of 4 times using a FET measurement. However, the contact issue at the InAu-MoS_2 interface may still exists for two-terminal devices, possibly leading to some underestimation of the vdW dielectric effect on the FET mobility enhancement. Its full potentials may be realized via the measurement of Hall devices. In principle, such a vdW dielectric may improve the device performance based on other 2D materials [2] and can be potentially used in other device architectures [32–34].

Conclusion

In summary, we demonstrated a novel approach to fabricate vdW dielectrics via thermal evaporation deposition using IMCs. Such an approach allows for precise deposition control, scalable fabrication and facile integration to other 2D materials. In addition, taking MoS_2 FET as an initial demonstration, we unambiguously confirm that our vdW dielectric is capable of supporting higher-quality 2D electronic devices with respect to SiO_2, with a significant electron mobility enhancement and a great hysteresis reduction. Our vdW dielectric not only overcomes the drawbacks of other vdW dielectrics (hBN etc.) in terms of process compatibility to standard semiconductor manufacturing, but also keeps their

comparative advantages in the fabrication of high-performance electronic devices over conventional dielectrics. Our results potentially lead to the scalable fabrication of 2D devices with their intrinsic properties preserved using vdW dielectrics.

Methods

Thermal evaporation deposition. The thermal evaporation deposition of Sb_2O_3 is carried out via standard deposition system (Nexdep, Angstrom Engineering) in high vacuum (10^{-6} torr). The deposition rate is well controlled by an in-situ crystal quartz monitor. We use a low deposition rate of 0.06 Å/S for all the fabrication of Sb_2O_3 film to keep the flatness of Sb_2O_3 film.

AFM. The morphology characterization and thickness calibration of Sb_2O_3 film as well as the thickness measurement of MoS_2 are carried out with AFM (Bruker Dimension FastScan).

Absorption spectroscopy. Absorption spectrum of Sb_2O_3 film deposited on glass substrate is obtained via Shimadzu SolidSpec-3700i UV-VIS-NIR spectrophotometer.

Optical spectroscopy. Raman spectra and photoluminescence are obtained in a confocal Raman system (WITek Alpha300) with an excitation laser of 532 nm at 2 mW.

Computation methods. The first-principles calculations were performed in the Vienna ab initio simulation package (VASP). The computation details for density of states for Sb_2O_3, vacancy formation energy within Sb_2O_3 molecule and gas adsorption are respectively described in supplementary information.

MoS_2 FET fabrication and test. 2D MoS_2 are prepared via mechanical exfoliation using scotch and PDMS. The SiO_2 substrates are firstly well cleaned with Ar plasma (Diener Pico). The fabricated Sb_2O_3 substrates are normally exposed in air before the exfoliation of MoS_2. After the confirmation of MoS_2 via optical measurement. PMMA is spin-coated onto the substrates with MoS_2. Afterwards, the electrodes are defined via standard electron beam lithography (EBL), followed by the deposition of 10 nm In and 90 nm Au evaporated via electron beam. After the metal lift-off in acetone, the devices are transferred into a chamber equipped with semiconductor analyzer Keithly 4200. We pump the chamber and keep it in high vacuum (10^{-6} torr) for 3 hours to eliminate the gas adsorption on device surfaces before the device test. Afterwards, devices tests are carried out at increasing temperature from 40 K to 300 K.

FET mobility extraction. The FET mobility is extracted from transfer curve via the formula

$$\mu_{FE} = \frac{L}{WCV_{ds}} \frac{dI_{ds}}{dV_{gs}}$$

where L and W are respectively the width and length of channel material, C is the gate capacitance, V_{ds} and I_{ds} are respectively the biased voltage and current between source and drain, and V_{gs} is gate voltage. The

capacitance of SiO_2 substrate is estimated to be 1.15×10^{-8} F/cm^2 for the dielectric constant (3.5) and thickness (300 nm). The capacitance of our Sb_2O_3 substrate deposited on SiO_2/Si is estimated to be 1.15×10^{-8} F/cm^2 for the dielectric constant (11.5) and thickness (40 nm).

Carrier density estimation. The charge carrier density of channel materials is estimated via $n=C\ (V_{gs}-V_{th})/\ e$ where V_{gs} is the gate voltage and V_{th} is the threshold voltage (determined from the FET transfer characteristic curves) and e is electron charge.

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Declarations

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Author contributions

K.L and T.Z conceived the ideas. K.L and B.J. designed and carried out most the experiments under T.Z.'s supervision. K.L, B.J and X.H deposited the film. K.L and J. D performed the absorption spectrum measurement. P.G, and L. H carried out the works of first-principle calculations. X. C, L.L, S.Y and F. Z helped to analyze the data. K.L, W.H, L.L and T.Z worked on the images with the assistance from all the others. K.L wrote the paper with the inputs of all the co-authors.

Competing financial interests

The authors declare no competing financial interests.

Figures

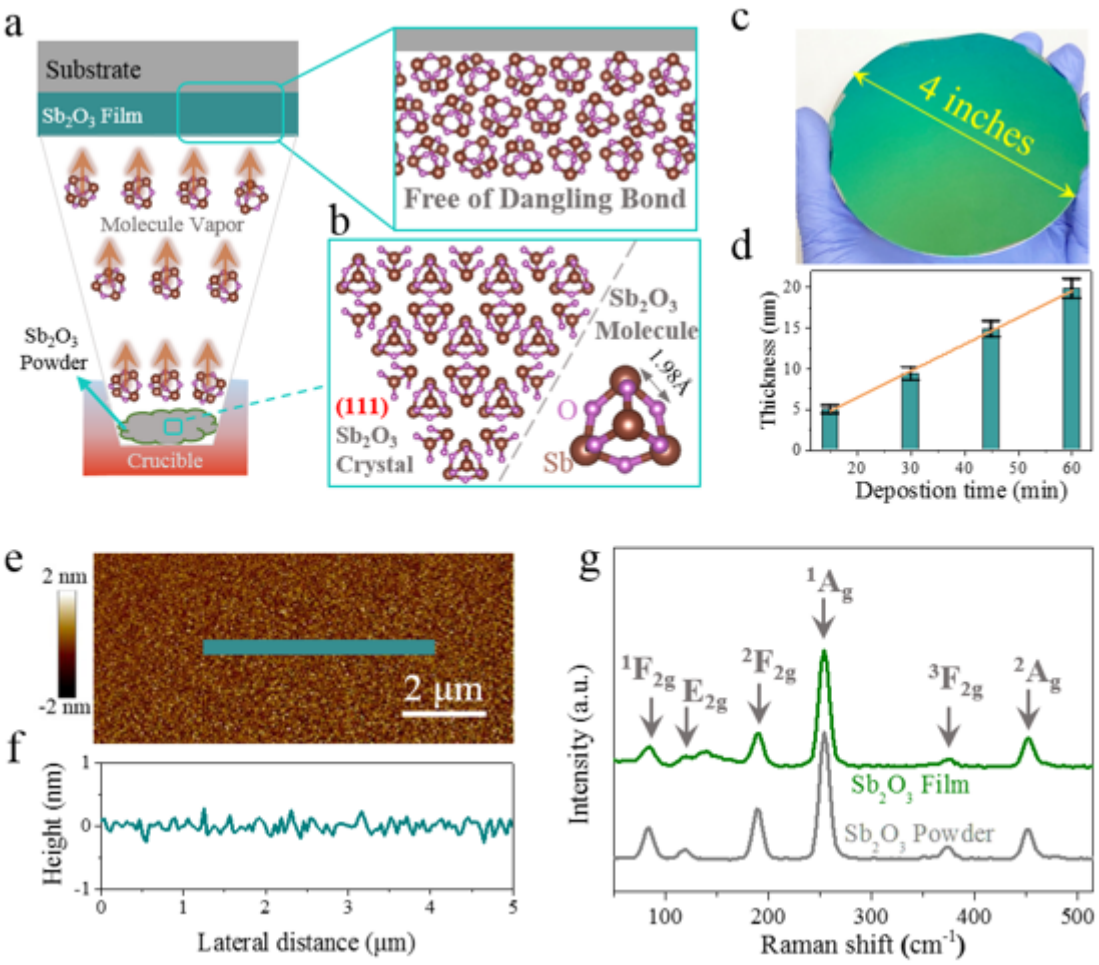

Figure 1

Fabrication of wafer-scale Sb2O3 film via standard thermal evaporation deposition. a, Schematic figures for the fabrication of vdW film composed of Sb2O3 molecules via STED. b, Molecular crystal structure of Sb2O3 showing (111) plane and the structure of the ultra-small molecule. c, Sb2O3 film of 40 nm homogeneously deposited on a 4-inch wafer. d, Well-controlled thickness of our Sb2O3 film versus deposition time at a given deposition rate. e and f, AFM image of Sb2O3 film and a corresponding line profile. g, Raman spectra of Sb2O3 film of 40 nm deposited on substrate (green) and Sb2O3 source powder (grey) for thermal evaporation deposition in a.

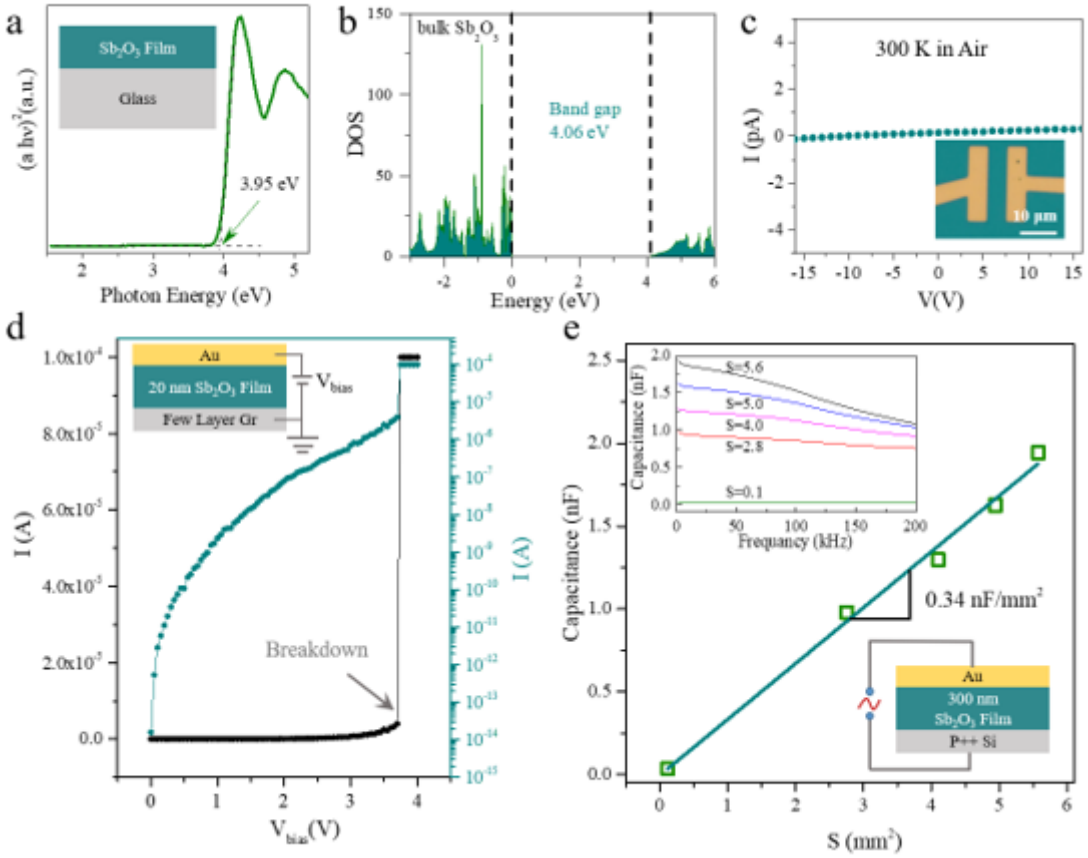

Figure 2

Dielectric properties of Sb2O3 film. a, The absorption spectrum of Sb2O3 film deposited on glass. , The density of state of bulk Sb2O3 via first-principle calculations, with the CBM being set at 0 eV. c, Conductivity measurement of Sb2O3 film deposited on SiO2/Si substrate. Inset: the optical image of the device for the measurement. d, The breakdown measurement of Sb2O3 film. Inset: the schematic figure of the measurement device. e, The capacitances of parallel plate with Sb2O3 film as the dielectric material at relatively low frequency (10 kHZ), from which the dielectric constant of Sb2O3 film can be determined. Inset: the capacitance measured at various frequency (top-left corner) and the schematic figures of the devices for frequency-capacitance measurement (bottom-right corner).

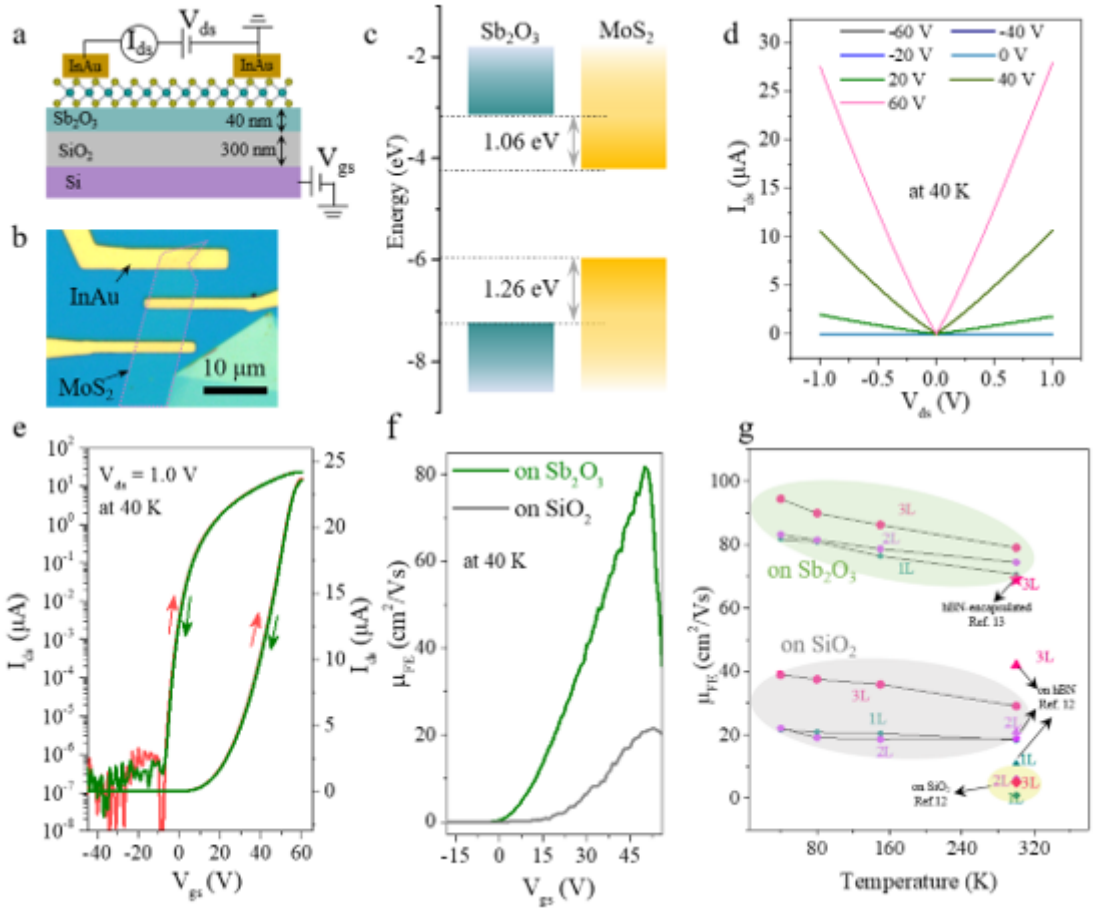

Figure 3

MoS2 FET supported by vdW Sb2O3 substrate. a, Schematic figure of monolayer MoS2 FET supported on Sb2O3 substrate. b, Optical image of the FET device. c, The band alignment of Sb2O3 and monolayer MoS2[27], with the band offsets over 1 eV. d, The output curves (Ids-Vds) of monolayer MoS2/Sb2O3 FET measured at 40 K. e, the double-sweep transfer characteristic curves of monolayer MoS2 FET. f, The FET mobility of monolayer MoS2, respectively on Sb2O3 and standard SiO2 substrate at various gate voltage Vgs. g, The temperature-dependent FET mobility of few-layer MoS2 supported on Sb2O3 and SiO2 substrate. As references, we also plot together some reported values of MoS2 FET supported on the widely used vdW dielectric hBN as reference [12, 13].

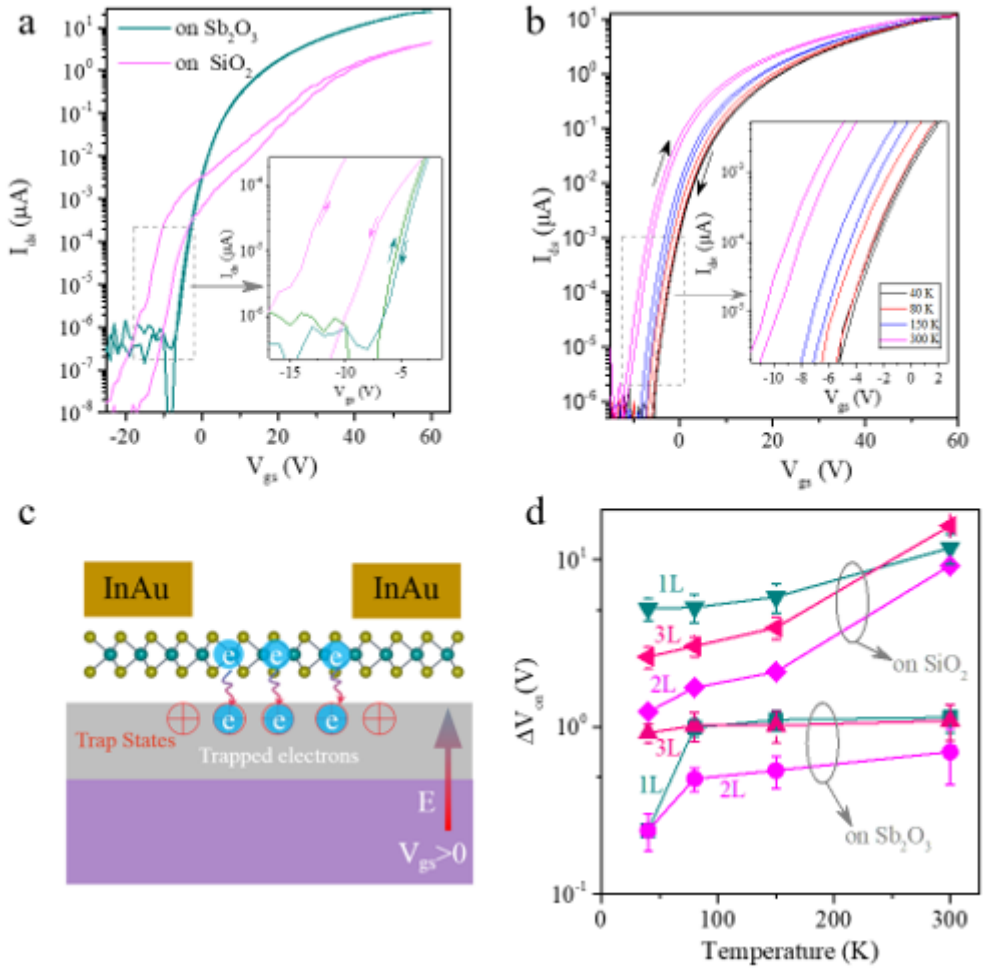

Figure 4

Hysteresis of MoS2 FETs supported on Sb2O3 and SiO2 substrate. a, Double-sweep transfer characteristic curves of monolayer MoS2/Sb2O3 and MoS2/SiO2 FETs respectively. b, Temperature-dependent hysteresis of monolayer MoS2/Sb2O3 FET. c, Schematic figure depicting the charge trapping from channel material into dielectric trap states during the FET switching, giving rise to the hysteresis window in double-sweep transfer characteristics curves. d, Temperature-dependent hysteresis (ΔVon) of MoS2 FET with various layer number supported on SiO2 and Sb2O3 substrates.

Supplementary Files

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- Supplementaryinfo.docx