Design of Low Power Architecture for Approximate Parallel Mid-Point Filter

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***Abstract*—Approximate computing is a modern techniques for design of low power efficient arithmetic circuits for portable error resilient applications. In this work, we have proposed a Adaptive Parallel Mid-Point Filter (APMPF) architecture using proposed imprecise Max-Min Estimator (MME)targeting digital image processing. Parallel architecture for the MME can trade-off hardware at the expense of accuracy are proposed and used in the proposed APMPF. In APMPF, we use three level of sorting to estimate the mid-point of 3 x 3 window. Switching based trimmed filter is proposed for precise estimation of the selected window. Experimental Results interms of Area, Power and Delay with 90nm ASIC technology exposed that to the least, Proposed filters demonstrate 7% and 9% Area Delay Product (ADP) and Power Delay Product (PDP) reductions, respectively, compared to precise filter design.**

Index Terms*—Mid-Point Filter, Approximate Computing, Low Power architecures

1. INTRODUCTION

Digital images are often degraded by the noise resulting from image sensors or transmission of images. Hence, Image denoising is implemented to restore the noisy pixels with a likely value.To achieve the high visual performances, many algorithms were intended to increase the computational complexities and hardware requirements. These imparts the researchers to design an efficient hardware architectures attended to meet high visual performances.

Approximate computing is done better in error resilent applications for signal and image processing. Approximate compressors were proposed [1,2] and implemented in various multiplier designs for the image and signal processing applications. In ref[3] approximate subtractors proposed for various signal and image enhacement applications. Approaches in [4,5] various imprecise adders were intended for the low power circuits.

Approximate computing is an energy efficient approach to design low power architectures applicable for error tolerant applications. For the digital image processing applications, the visual quality degradation is less, eventhough the small error persist. In literature the various approaches were proposed for hardware implementation that use approximate computing. Two hybrid CMOS imprecise adders were designed [6] and implemented in gaussian filter for image processing application. Simple and efficient novel imprecise comparators were proposed and implemented in median filter for low power image processing application was proposed in Ref[7,8]. A novel sorting algorithm to design high speed area efficient median filter was proposed by Vasanth etal in Ref[9]. Novel mid-point filter was proposed in ref[10] using quantum cells in its buiding blocks for salt and pepper noise removal. 2-D median filter was proposed to focus on low cost design in ref[11]. approaches in [12-15] proposed to reduce hardware complexity in median filter architecture in imaging applications. In ref[16] gaussian filter was proposed for efficiently reduce the latency by the compact architecture and error introduced adder which play the role major role in the circuit. In Ref [17] , new architecture was designed to estimate the median for the 25 input values.

In this research work, we use the approximate computation in the Max-Min Estimator, for enhancing the performance of the Adaptive Parallel Mid-Point filter (APMPF). we propose the novel design of PMPF to perform at higher noise densities of Salt and Pepper Noise affected image and three designs Max-Min Estimator units (MME). The filter uses the first order neighbourhood of the processing pixel in design. The novelty of the proposed work is that the architecture, we employ the trim to corrupted pixels for processing, so as to reduces the major negative aspect of the mid-point filter in salt and pepper noise removal. This will equalize the error occurred due to the approximation in the MME for the error tolerant imaging applications.

The rest of the paper is organized as follows. A brief description about the related approaches on filter architectures is discussed in section-2. Detailed explanation of the proposed MME architectures and its building blocks are in section-3. The novel proposed APMPF has discussed in section-4. Performance evaluation and comprehensive comparison with earlier approaches is given in Section-5. Finally, the proposed work done is concluded in Section-6

2. RELATED WORKS

Mid-point filter perform sorting on a set of inputs in a processing window to replace corrupted processing pixel with the mid-point value. Sorting algorithm employed in MF design fall into three main categories viz., systolic array, sorting network-based architectures and radix method or Threshold Decomposition Filter (TDF) [7]. Parallel operation can be performed with sorting based algorithms to design high speed MPF architectures. A brief comparison of various sorting architectures to estimate the Maximum and minimum for the filter is discussed in following sub sections.

2.1 Quantum midpoint Filter (2020)

Abdalla Essam Ali et al [10] proposed a novel approach for Quantum Mid point Filter (QMPF) with Quantum MME and other building blocks. The proposed Reversible logic based, three basic modules and four composite modules are implemented in the mid-point filter architecture. Filter

architecture is based on sorting of rows and colomn values so as to estimate the required value to restore the corrupted. Three cell sorter consists of three MME to processs the three input,produces the Qmax and Qmin based on Quantum Circuit. It uses 13 MME units for a 3 X 3 processing window and has 6 units in the critical path.

2.2 Low Latency Filter(2017)

Vineet kumar et al [17] proposed a design of efficient architecture for 5x5 processing window. Row and colomn sorting based approach implemented in five input sorter. The architecture is modified to estimate the mid point is shown in fig. 2. A Five Cell Sorter (FCs) consists of twelve MME unit which includes 4- three cell sorter. Note from the LLF architecture it uses 84 MME units and 24 MME units in its critical path.

In this work we focus on to reduce the Power-Delay Product (PDP) and Area-Delay Product (ADP) with little sacrification of precise MME circuit which plays the essential role in the filter architecture.

3. Proposed Max-Min Estimator

In this work, we have proposed three designs of low power approximate Max-Min estimator units, that are developed to estimate the Max-Min of the given N input. For an *n* bit input, design-1(S_{6b}) use 3*n*/4 MS bits, design-2(S_{4b}) use *n*/2 MS bits and design-3(S_{8b}) uses cascade structure of the two *n*/2 bits in both LS & MS bits for MME. Boolean Expression for the proposed Max-Min estimator(MME) unit designs for 8-bit (n=8) is shown in Eqs(1)-(3). S_{6b}, S_{4b} and S_{8b} represents the select signals of Proposed MME-1, MME-2 and MME-3 Max-Min Estimator unit respectively. Out_{max} and Out_{min} denotes the corresponding Maximum and Minimum outputs of the MME UnitThe logic level optimization is done by simplifying the logic using Karunagh Map (K-Map), whereas circuit level optimization has been carried out by using different transistor sizes. Two bit K-Map for the MME unit is shown in figure 1.

$$S_{6b}=\left((((\overline{a2}b2+\overline{a3}b3)+\overline{a4}b4\right)+\overline{a5}b5)+\overline{a6}b6)+\overline{a7}b7 \quad (1)$$

$$S_{4b}=\left((\overline{a4}\,b4+\overline{a5}\,b5\right)+\overline{a6}\,b6)+\overline{a7}\,b7 \quad (2)$$

$$S_{4b\_LS}=\left((\overline{a0}\,b0+\overline{a1}\,b1\right)+\overline{a2}\,b2)+\overline{a3}\,b3$$

$$S_{8b}= S_{4b\text{-}LS} + S_{4b\text{-}Precise\text{-}MS} \quad (3)$$

b_1b_0 / a_1a_0	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

(a)

b_1b_0 / a_1a_0	00	01	11	10
00		1	1	1
01			1	1
11				
10		①	1	

(b)

Fig. 1. Select Signal for two bit MME Unit. a) Precise b) Approximate

The researchers are concentrating the approximation in MME or compare and swap unit recently and earlier it is less. Node capacitance of the proposed gate level circuit for the three MME units is less in the critical path compared to the standard design. The inputs of the proposed MME Units are represented by a[7:0] and b[7:0] for MME-3, MME-2 uses a[7:2] -b[7:2], and MME-1 uses [7:4]-b[7:4] bits respectively.

Logic depth of proposed MME-1, MME-2 and MME-3 units are given by Eqs(4-6) respectively

$$t_{AC1}=2*t_{AND}+4*t_{OR}+2*t_{NOT} \quad (4)$$

$$t_{AC2}=2*t_{AND}+6*t_{OR}+2*t_{NOT} \quad (5)$$

$$t_{AC3}=2*t_{AND}+8*t_{OR}+2*t_{NOT} \quad (6)$$

4. Proposed Mid - point filter

The Adaptive Parallel Mid-Point Filter is proposed, which process the neighbourhood to replace the processing pixel with the Mid-Point of the N-inputs. It consists of Impulse detector and Mid-Point Filter (MPF) which are the two basic blocks in the proposed structure, shown in figure 2. The various filters were discussed in literature, which conclude that the median filter works better in terms of visual enhancement of impulse noise corrupted image but requires more hardware for the implementation. Hence, it generates high power and area. To maintain the quality and reduce the hardware requirements, modified architecture is designed to estimate the mid-point which requires less hardwarea and performs well in high density corrupted images.A brief about the blocks are discussed in the following subsections.

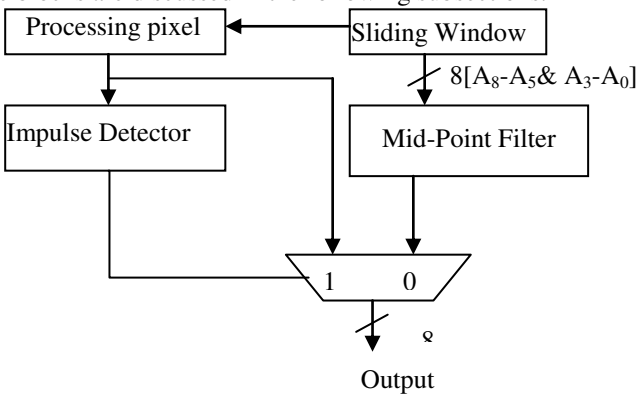


Fig 2. Block Diagram of Mid-Point Filter

4.1 Impulse Detector

Detect an impulse noise is an interesting task due to its variable high-low characteristics. Direct detection works well in the range of 1 to 2n-1, i.e. n- number of bits, but fails to detect in the range [0-2n]. The resultant of the adaptive detection fail to achieve the 100% accuracy more than 30% noise corrupted in the first order neighbourhood. Overcome this issues the higher order neighbourhood should be considered for impulse noise detection.

4.2 Proposed Filter

In this Proposed filter, Novel architecture for adaptive pixel selection of uncorrupted neighbourhoods and process to improve the performances in filtering. Here, We designed with three stages of sorting network based architecture to estimate the mid-point. The three stages are required for adaptive Max-Min selection to exclude the corrupted from processing. In the first stage all the n-inputs are processed by Max-Min Estimator. For n-8, four Max-Min Estimator ($MME_{1\text{-}4}$)

produces the n/2 maximum and n/2 minimum. Similarly, the second stage (MME_{5-7}) produces n/4 maximum and n/4 minimum. Finally, The third stage (MME_{8-10}) produces the overall maximum and overall minimum from the n-input. The Select Signal for the PMPF is explaind as the algorithm below.

Algorithm Steps:

1. initialize the count=0, input[n]=0.
2. check for the uncorrupted from neighbourhood pixels using NDU.
3. if NDU='0' then push the value in the input and increment the count else goto the step-2 until all the neighbourhood pixels are processed.
4. increment the pointer in the input array.
5. repeat the steps [2-4] until n-number of processing
6. if count = n/4, n/2 and n, then SS='01','10' &'11' respectively

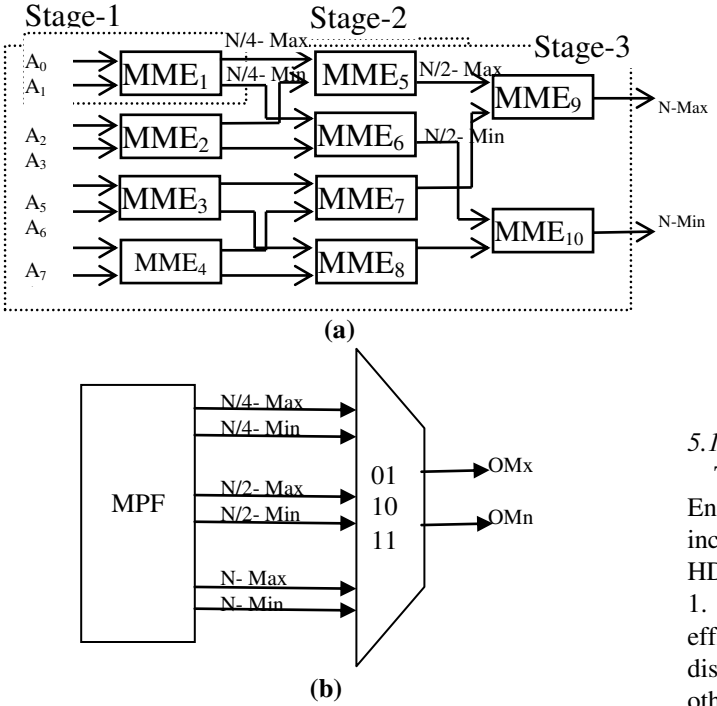


Fig 3. Block level architecture of (a) Three Level MME Unit (b) Proposed Filter

4.3. Mid-Point Computation Unit

The Mid-Point Computation Unit (MCU) Consists of Ripple Carry Adder (RCA) and shifter. At first, the shifter plays the right shift operation of the given two input(OMx and OMn) then the RCA produce the result that Mid Point of the given n-input. The block diagram for the Mid-Point Computation Unit is shown in figure 5.

5. Results and Discussions

In this Section, the performance of the proposed filters are discussed in terms of circuit metrices. The proposed architectures Circuit metric and visual quality results for the proposed designs are compared with other state-of-the art designs and the performances for the same is analysed to verify its functional ability. For the circuit metric analysis, Power, area and delay are evaluated.

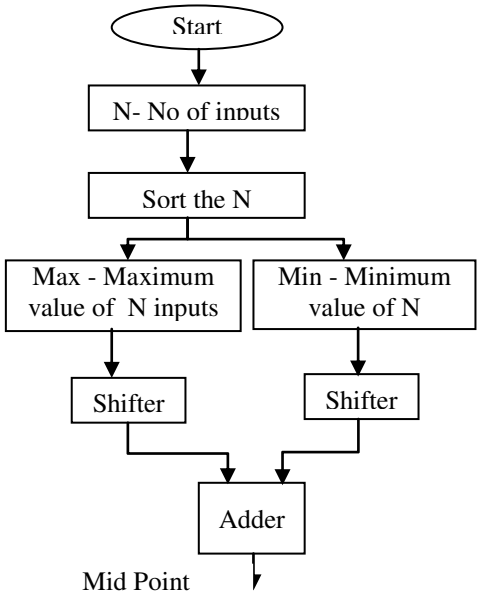


Fig.4 Flow Chart of Mid-Point Filter

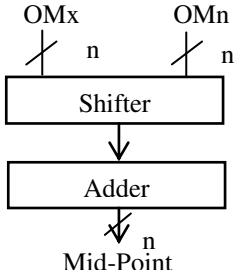


Fig.5 Mid-Point Computation Unit (MCU)

5.1 Circuit Metrics

The circuit metrics are synthesized by the Cadence Encounter tool in 90nm ASIC technology. All the designs including state of the art filters are designed using verilog HDL. The circuit metrics comparison table is shown in table-1. It clearly shows that the proposed PMPF reveals high efficiency than the other designs. Note from table 1, the power dissipation of the proposed filter is low compared with the other state-of the art designs. This is due to the low logical depth of the filter architecture.Hardware testing for the mid-point filter using Xilinx system generator was used.

The APMPFs performance and state-of the art designs, interms area, delay, power, PDP and ADP are shown in Tables 1. Note from Table 1, that PF-MME_A1, PF-MME_A2, PF-MME_A3 is 16%, 11 & 10% power reduction compare to the PF-MME_P1 design. Also note the power dissipation of PF-MME_A1 is significantly low compared to other PF designs. QPMF-MME_A1 and LLMF-MME_A1 is best in its respective MME designs, Circuit level performances are high when compared to the PF Designs.Conversly the average error of increases compare to other proposed methods.

Implementations of the proposed filters are carried out with verilog HDLusing Xilinx ISE 14.2 compiler tool and spartan 6 (XC6XLX45-CSG324).

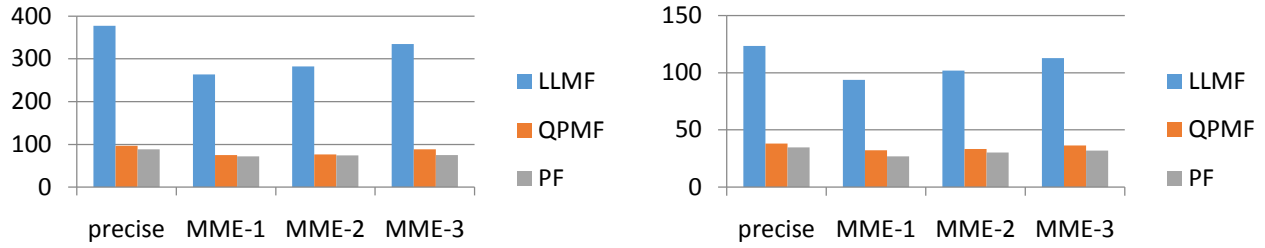
6. Results and Discussions

This paper has presented a low power mid point filter architecture is implemented in image denoising application.

Parallel implementations exposed reduce the physical properties and detection based approach precise the results with high accuracy. Also this paper presents three approximate max-min estimators plays key role for low power architectures. Different architectures are being analyzed its functional efficacy for the size of nine input with same size of state -of- art designs. The proposed filters shows better result in circuit metrices compared to QPMF and LLMF designs.

Table 1 Performance Comparison of Proposed and Filter designs (n = 8) in 90nm ASIC Technology

Designs	APMPF					QPMF					LLMF				
	Area (μm^2)	Delay (pS)	Power (μW)	PDP	ADP	Area (μm^2)	Delay (pS)	Power (μW)	PDP	ADP	Area (μm^2)	Delay (pS)	Power (μW)	PDP	ADP
PF-P1	3615	9590	91.768	88.05	34.66	3897	9785	98.427	96.427	38.13	12547	9847	383.189	377.32	123.55
PF-A1	3059	8828	77.467	72.27	27.00	3546	9047	82.541	74.674	32.08	10259	9125	289.14	263.84	93.613
PF-A2	3171	9059	81.870	74.05	30.31	3645	9145	83.645	76.493	33.33	10748	9489	297.789	282.57	101.98
PF-A3	3518	9554	82.747	74.91	31.85	3752	9671	91.548	88.536	36.28	11654	9687	345.687	334.86	112.89



(a) (b)

Fig.9 (a) PDP comparison, (b) ADP Comparison

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