A Novel Structure of All-optical Optimised NAND, NOR and XNOR Logic Gates Employing a Y-shaped Plasmonic Waveguide for Better Performance and High-Speed Computations

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Abstract

All-optical devices are proven to have broad range of applications in the areas of communication. These devices form the basic building blocks of complex integrated circuits. By integrating these devices in the fields like signal processing, chip designing and network computations, a much more efficient device can be achieved. The design of all-optical logic gates like NAND, NOR and XNOR using plasmonic based Y-shaped power combiner is implemented in this paper work. The concept of linear interference is applied in the combiner to achieve the desired logic gates. The work is simulated and analysed using Finite-Difference Time Domain (FDTD) method, which is valuated using MATLAB. The present work fits under the area of 60 μm^2 which is smaller than the existing structures. The insertion loss, transmission efficiency and extinction ratio parameters are calculated and compared to variety of other designs.

1. Introduction

The demand for faster communication is surging at an unexpected rate. While the researchers are carrying several experiments to meet the needs of high speed transmission, a new offspring called plasmonic evolved from its predecessors (Gibbs et al. 1985; Hu et al. 2008). In the earlier days, semiconductor based transistors served the need of electronics. It often sits back due to limitations like low speed, high power consumption and heat dissipation (Cotter et al. 1999; Priya et al. 2021). Having eliminating these, photonic evolved with high speed communication by replacing electrons with photons (Tang et al. 2010; Holmgaard et al. 2007; Wu et al. 2004). However, it is limited by diffraction when the order of design is close to the operating wavelength (Kumar et al. 2017). Also the optical sources are bulk and are difficult to fabricate, making the devices larger. Plasmonics solved these limitations by combining the advantages of electronics and photonics (Hayashi et al 2012). The surface plasmon polaritons evolved as a result of surface plasmon resonance phenomenon confining at nanoscale level thereby eliminating the diffraction limit (Barnes et al. 2003; Zhang et al. 2009; Talebi et al. 2008; Gramotnev et al. 2005). Various configurations of plasmonic waveguides like MIM, IMI, DLSPPW etc., are used to design the plasmonic structures (Feng et al. 2007; Zia et al. 2006; Pile et al. 2005; Charbonneau et al. 2005; Jung et al. 2010). All optical logic gates are being proposed by many researchers around the world using several design techniques like electro-optic (EO), semiconductor optical amplifier based mach-zehnder interferometer (SOA-MZI), photonic crystals (PhC) and plasmonic (Rao et al. 2021; Fakhruldeen et al. 2018; Pal et al. 2020; Birr et al. 2015; Gogoi et al. 2015). Using these techniques, all the basic gates like NOT, AND, XNOR, OR, XOR and universal gates like NAND and NOR are realized (Taflove et al. 2000; Anguluri et al. 2021; Kumar et al. 2015; Kim et al. 2006; Nozhat et al. 2017). These can be used to create a variety of other combinational and sequential circuits (Singh et al. 2019; Rao et al. 2020; Isfahani et al. 2009; Nozhat et al. 2015; Singh et al. 2014). Using a Y-shaped power combiner, all optical universal logic gates such as NAND and NOR, as well as all-optical XNOR gates are presented and proven using the FDTD method (Kotb et al. 2020; Moradi et al. 2019; Fu et al. 2012; Moniem et al. 2017; Swarnakar et al. 2021). The present work is categorized into several sections. The design and operation of NAND, NOR and XNOR (NNX) gates utilise the same structure covered in Section 2. Sections 3, 4 and 5 gives the simulation results and assessment of all-optical NAND, NOR and XNOR respectively. Section 6 gives the conclusion of the present work.

2. Design And Operation Of All-optical Nand, Nor And Xnor Logic Gates

All-optical NAND, NOR and XNOR logic gates are built using a Y-shaped plasmonic waveguide. The schematic consists of two Y-shaped power combiners which are cascaded such that the output of one Y-combiner is given as input to the second Y-combiner. The two inputs of the first combiner are considered as the ports for input signals (A and B) and the third input signal is considered as the reference signal (R). The second combiner's output port serves as the output port of the designed structure. The layout of the design is depicted in Fig. 1.

The plasmonic waveguide structure is designed with a refractive index of 2.01. The linear interference principle governs how the Y-combiner works. The two Y-combiners are combined by a linear waveguide of length (L) 2.9 μm. The phase shift of the input is controlled by an external phase shifter. The entire schematic is designed under the footprint of 12 μm × 5 μm. The two inputs to logic gates are applied to the first and second ports of first Y-combiner and the output is given to the second combiner. The second Y-combiner's second input is connected to R, which is always high. The phase of R is adjusted in accordance with the desired output of the logic gate. The principle of constructive and destructive interference occurs at the junction of each combiner. According to linear interference, if the input’s path difference is zero and phase is in the order of even multiples of π, constructive interference will occur, resulting in modulation of the optical signal, and vice versa. Similarly, if the path difference is zero and phase is in odd multiples of π, the destructive interference will occur there by cancelling the optical signal. The design specifications of the structure are shown in below Table 1.

Table 1
Design parameters of the proposed structure

Sl. No.	Parameter	Value
1.	S-bend Length (S)	2.9 μm
2.	Linear waveguide (L)	5.2 μm
3.	Input separation gap (D)	3 μm
4.	Waveguide width	0.3 μm
5.	Refractive index	2.01

3. Simulation Results And Discussion

The FDTD method employs the device analysis. A continuous transverse electric (TE) optical wave with perfectly matched boundary conditions is considered as the input. In this design, low intensity signals have an optical intensity of 1e9 W/m, while high intensity signals have an optical intensity of 3e9 W/m are used to excite the input ports with 1550 nm wavelength. All the input states of two-input NAND, NOR and XNOR are provided with the change in phase of the inputs with either 0^0 or 180^0 to satisfy the gate's output. The parameter specifications for designing NAND, NOR and XNOR gate are shown in Table 2.

Table 2
Parameter specifications of NAND, NOR and XNOR gate

Sl. No.	Simulation Parameters	NAND		NOR		XNOR	
1.	Mesh size	X (μm)	Z (μm)	X (μm)	Z (μm)	X (μm)	Z (μm)
		0.0480	0.0438	0.0370	0.0346	0.0738	0.0738
2.	No. of mesh cells	X	Z	X	Z	X	Z
		103	273	124	295	67	162
3.	Input field transverse	Gaussian		Gaussian		Gaussian	
4.	Low intensity signal	1e9 W/m		1e9 W/m		1e9 W/m	
5.	High intensity signal	3e9 W/m		3e9 W/m		3e9 W/m	
6.	Reference signal	3.3e9 W/m		3.3e9 W/m		3.3e9 W/m	

3.1 NAND Logic gate

The nand gate works like, when both inputs are high, the output is low; otherwise, it is high. To improve the feasibility of constructing complicated digital circuits, universal gates must be used. The simulation and analysis of NAND gate is carried using FDTD approach. The practical outcomes are then compared to the theoretical outcomes derived using MATLAB. The NAND schematic's simulation parameters are shown in Table 2. For 2-input NAND gate, four combinations of inputs are applied to the designed waveguide. The output of NAND gate is obtained from the output port of second combiner. The output normalized power (P_{out}) along with the input phase of each input combination is shown in Table 3.

Table 3
Simulation results of all-optical NAND gate

Sl. No.	Input signals				Output signal	
	A	ϕ_A	B	ϕ_B	P_{out}	Transmission efficiency (%)
1.	0	0^0	0	0^0	1.0983 ≡ 1	109
2.	0	0^0	1	180^0	1.4147 ≡ 1	141
3.	1	0^0	0	180^0	1.4734 ≡ 1	147
4.	1	0^0	1	0^0	0.1137 ≡ 0	11.3

From Table 3, it is clear that the output behaviour of NAND gate is satisfied. The high and low intensity output signal powers are noted. Transmission efficiency is calculated by multiplying the highest output power with 100 as represented in Table 3. Fig. 2 displays the timing diagram of a NAND gate verified using MATLAB. Fig. 3 shows the light propagation across NAND gate for all input signal combinations.

Case (i):

Here, a low-intensity signal of 1e9 W/m is applied as input to both of the first Y- combiner ports. A phase of 0^0 is applied to input A and 180^0 is applied to the input B. The intensity of 3.3e9 W/m with a phase of 180^0 is applied as input to R. The first combiner receives inputs that are out of phase and have the same intensity, there exists destructive interference at the output and the input to the next Y-combiner is assumed to be low. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output as represented in Fig. 3(a).

Case (ii):

Here, the first input port is given the signal intensity of 1e9 W/m with phase of 0^0 and the second input port is given the intensity of 3e9 W/m with a phase of 180^0. Due to the out-of-phase nature of these signals, destructive interference occurs at the output of the first combiner, resulting in a low signal at the next input. The R being high signal as the other input causes constructive interference at the output leading to high signal as represented in Fig. 3(b).

Case (iii):

Similar to the above case, the first and second input ports are given high and low intensity signals of intensity 3e9 W/m and 1e9 W/m respectively. The phase shift of the input ports remains same as 0^0 and 180^0 for first and second ports respectively. Due to destructive interference, the low signal reaches the next combiner and the R will reach the output port as a result of constructive interference i.e., logic '1' as shown in Fig. 3(c).

Case (iv):

In this case, the two input ports are given high intensity signal of intensity 3e9 W/m. The phase shift of two inputs ports is made 0^0. Then according to constructive interference, the output signal will be high and of more intensity as the input signal. The R of intensity 3.3 W/m is given as the compensating signal to cancel the previous output so as to obtain the logic '0' at the output. The low intensity output is observed due to occurrence of destructive interference at the output junction as shown in Fig. 3(d).

3.2 NOR logic gate

The output of NOR gate is examined with the same structure as depicted in Fig. 1. The output of NOR gate goes low when any of the inputs is high and high when both are low. The FDTD approach is used to simulate and analyse the NOR gate. The obtained practical results are then compared with the theoretical results obtained from MATLAB. The simulation specifications of NOR schematic is given in Table 2. The P_{out} and input phase for all-optical NOR gate is shown in Table 5. From Table 5, it is clear that the output behaviour of NOR gate is satisfied. The transmission efficiency is also formulated and provided in Table 5. The timing diagram of NOR gate is verified using MATLAB and is shown in Fig. 4.

Table 5
Simulation results of all-optical NOR gate

Sl. No.	Input signals				Output signal	
	A	ϕ_A	B	ϕ_B	P_{out}	Transmission efficiency
1.	0	0^0	0	0^0	1.3361 ≡ 1	134
2.	0	0^0	1	0^0	0.0136 ≡ 0	1.36
3.	1	0^0	0	0^0	0.0087 ≡ 0	0.87
4.	1	0^0	1	0^0	0.0237 ≡ 0	2.37

Case (i):

In this case, the low intensity signal of 1e9 W/m with phase shift of 0^0 is applied as input to both the input ports of first Y-combiner. The R of intensity 3.3e9 W/m is applied as input with a phase shift of 180^0. Since the first combiner takes inputs having same intensity and in phase, constructive interference will occur at the output and the input to the next Y-combiner is assumed to be low. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output i.e., logic '1' as shown in Fig. 5(a).

Case (ii):

In this combination, the first input port is given the low signal of intensity 1e9 W/m and the second input port is given high signal of intensity 3e9 W/m with a phase of 0^0 for both ports. A high signal is obtained at the output of the first combiner as a result of constructive interference. The R

being high and is out of phase with the output from first combiner causes destructive interference at the output leading to low signal as shown in Fig. 5(b).

Case (iii):

The first and second input ports are provided with intensity of 3e9 W/m and 1e9 W/m respectively with 0^0 phase shift. Due to the constructive interference, the high signal reaches the next combiner and the R with high intensity which is out of phase caused destructive interference and low signal will reach the output port as in Fig. 5(c).

Case (iv):

In this case, the two input ports are given high intensity of 3e9 W/m with a phase shift of 0^0. The combiner output gives logic high signal as a result of constructive interference. This high signal is combined with R of opposite phase. Due to destructive interference at the output junction, the low signal is received at the output as shown in Fig. 5(d).

3.3. XNOR logic gate

The same structure as depicted in Fig. 1 can be used to get the output of XNOR gate. The output goes low when inputs are different and high when inputs are same. The simulation and analysis of XNOR gate is carried using FDTD method. The practical findings are compared to the theoretical results generated using the MATLAB simulink tool. The simulation parameters of XNOR schematic are given in Table 2. For 2-input XNOR gate, four combinations of input values are applied as input to the design. The normalized P_{out} along with the input phase is shown in Table 7 for all-optical XNOR gate.

Table 7
Simulation results of all-optical XNOR gate

Sl. No.	Input signals				Output signal	
	A	ϕ_A	B	ϕ_B	P_{out}	Transmission efficiency (%)
1.	0	0^0	0	180^0	1.4294 ≡ 1	143
2.	0	0^0	1	180^0	0.0094 ≡ 0	1
3.	1	0^0	0	180^0	0.0138 ≡ 0	1.3
4.	1	0^0	1	180^0	0.5448 ≡ 1	55

From Table 7, it is clear that the output of XNOR gate is determined. The high and low intensity output signal powers are noted. The transmission efficiency is also formulated and provided in Table 7. The NAND gate timing diagram is presented in Fig. 6, which was simulated using MATLAB.

The simulation results of the XNOR gate are shown in Fig. 7. The input combinations are applied based on the truth table of XNOR gate.

Case (i):

In this combination, the low optical signal of intensity 1e9 W/m is applied as input to both the input ports of first Y-combiner. Phase of 0^0 and 180^0 is applied to first and second input ports. The R of intensity 3.3e9 W/m is applied as input to the reference. The output of first combiner will be XOR of A and B and is given to second combiner. The other port receives R as high intensity signal and the same is driven towards the output, thereby receiving the high signal at the output as shown in Fig. 7(a).

Case (ii):

Here, the first port is given the low signal of intensity 1e9 W/m with 0^0 phase shift and the second input port is given high signal of intensity 3e9 W/m with a phase of 180^0 for both ports. Due to constructive interference, high signal is obtained at the output of first combiner. The R being high signal and is out of phase with the output from first combiner causes destructive interference at the output leading to low output as shown in Fig. 7(b).

Case (iii):

Similar to the above case, the first and second input ports are given high and low intensity signals of intensity 3e9 W/m and 1e9 W/m respectively with 0^0 and 180^0 phase shift. Due to constructive interference, the high signal reaches the next combiner and the R which is out of phase causes destructive interference and low signal will reach the output port i.e., logic '0' as shown in Fig. 7(c).

Case (iv):

In this case, the two input ports are given high intensity signal of 3e9 W/m with 0^0 and 180^0 phase shift. The combiner output gives low signal as a result of destructive interference. This signal is combined with the R of opposite phase difference. Due to constructive interference at the output junction, the high signal is received at the output as shown in Fig. 7(d).

4. Performance Analysis Of Nand/nor/xnor Gate

The performance analysis of NAND/NOR/XNOR gate is analyzed by calculating extinction ratio (ER), insertion loss (IL) and transmission efficiency. The P_{out} matches the theoretical truth table of NAND/NOR/XNOR gate and the efficiency of the transmission is as high for NAND as 147% in case of '10' condition, NOR gate as high as 134% in case of '00' condition, XNOR gate as high as 143% in case of '00' condition.

On the basis of the output data, performance measures such as IL and ER are determined. The IL is given by

$$IL = 10log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (1)$$

where P_{out} is the peak output power and P_{in} is the peak input power (P_{in}). The ER is the proportion of peak P_{out} in the ON state ($P_{out}|\,ON$) to peak P_{out} in the OFF state ($P_{out}|\,OFF$). It is given by

$$ER = 10log_{10}\frac{\left(P_{out}|\,ON\right)}{\left(P_{out}|\,OFF\right)} \quad (2)$$

The IL and ER of the all-optical NAND gate are found to be 0.407 dB and 11.13 dB respectively. The IL and ER of the all-optical NOR gate are observed to be 1.25 dB and 24.29 dB respectively. The IL and ER of the all-optical XNOR gate are found to be 1.55 dB and 21.82 dB. The comparison of present work with the existing work is shown in Table 8.

Table 8
Comparison of all-optical NAND/NOR/XNOR gate with the existing structures

Sl. No.	Ref. No.	Designed logic gate	Components	Wavelength (nm)	Size	Channel profile	Low intensity optical Signal	High intensity optical Signal	Insertion Loss (dB)	Extinction Ratio (dB)	Transmission Efficiency (%)
1.	[8]	NAND	4 MZIs	1550	38 × 10 μm^2	n.r.[a]	0.026e6 W/m	0.026e6 W/m	n.r.[a]	n.r.[a]	n.r.[a]
		NOR	3 MZIs	1550	45 × 8 μm^2	n.r.[a]	0.026e6 W/m	0.026e6 W/m	n.r.[a]	n.r.[a]	n.r.[a]
2.	[26]	NAND	3 EO-MZIs	1330	~70 mm	n.r.[a]	0 V	6.75 V	n.r.[a]	n.r.[a]	n.r.[a]
		NOR	2 EO-MZIs	1330	~70 mm	n.r.[a]	0 V	6.75 V	n.r.[a]	n.r.[a]	n.r.[a]
3.	[27]	NAND	2 SOA-MZI Structures	1539.45	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	>15	n.r.[a]
4.	[28]	NAND	5 × 5 array of gold disk particles	445.5	520 × 520 nm^2	1.5	n.r.[a]	n.r.[a]	n.r.[a]	24	~90
5.	[29]	NAND	2 MZIs	1550	40 × 7.5 μm^2	1.65	0.7e9 W/m	3e9 W/m	0.756	10.25	n.r.[a]
6.	[30]	NAND	12 × 9 grid of photonic crystals	1550	7.2 × 5.4 μm^2	3.46	0 W/m	1 mW/m	n.r.[a]	17.59	n.r.[a]
		NOR	12 × 9 grid of photonic crystals	1550	7.2 × 5.4 μm^2	3.46	0 W/m	1 mW/m	n.r.[a]	14.3 dB	n.r.[a]
		XOR	12 × 9 grid of photonic crystals	1550	7.2 × 5.4 μm^2	3.46	0 mW	1 mW	n.r.[a]	10.52	n.r.[a]
7.	[31]	NOR	2 micro ring resonators	1550	n.r.[a]	3.1	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	81%
8.	[32]	NOR	2 square ring resonators and 3 linear waveguides	1535	n.r.[a]	1.47	0.004e6 W/m	0.007e6 W/m	n.r.[a]	n.r.[a]	70%
9.	[33]	NOR	Two 3dB couplers and 2 SOA amplifiers	1555	500 × 0.15 μm^2	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	15.67 dB	n.r.[a]
10.	[34]	XOR	3 SOAs and One Delayed Interferometer	1540	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]	n.r.[a]
11.	[35]	XOR	1 square ring resonator and 3 linear waveguides	1628	n.r.[a]	1.47	n.r.[a]	n.r.[a]	n.r.[a]	22.66	n.r.[a]
12.	[36]	XOR	Gold coated plasmonic slot waveguide	830	11 μm × 100 nm	1.5	n.r.[a]	n.r.[a]	n.r.[a]	24	219.3

Sl. No.	Ref. No.	Designed logic gate	Components	Wavelength (nm)	Size	Channel profile	Low intensity optical Signal	High intensity optical Signal	Insertion Loss (dB)	Extinction Ratio (dB)	Transmission Efficiency (%)
13.	[37]	XOR	18 × 15 array of silicon rods	1550	35 × 21 μm^2	3.39	0 mW	100 mW	n.r.[a]	n.r.[a]	87
14.	This work	NAND	2 Y-combiners	1550	12 × 5 μm^2	2.01	1e9 W/m	3e9 W/m	0.407	11.13	147
		NOR	2 Y-combiners	1550	12 × 5 μm^2	2.01	1e9 W/m	3e9 W/m	1.25	24.29	134
		XNOR	2 Y-combiners	1550	12 × 5 μm^2	2.01	1e9 W/m	3e9 W/m	1.55	21.82	143

n.r.[a] – not reported

Conclusion

In this work, the miniaturised design of all-optical logic gates like NAND, NOR and XNOR using Y-shaped plasmonic combiner has been proposed. The design, simulation and analysis of the work is done using FDTD method. The design of this work fits with in the area of 60 μm^2 which is smaller when compared to the existing structures. Several parameters like IL, transmission efficiency and ER which determines the performance are calculated from the output results. The ER of NAND, NOR and XNOR gates are found to 11.13 dB, 24.29 dB and 21.82 dB respectively. Because of its compact structure, the size of digital circuits will reduce by a significant amount which accounts for better performance in optical computing.

Declarations

Declarations

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Tables

Tables 4 and 6 are not available with this version

Figures

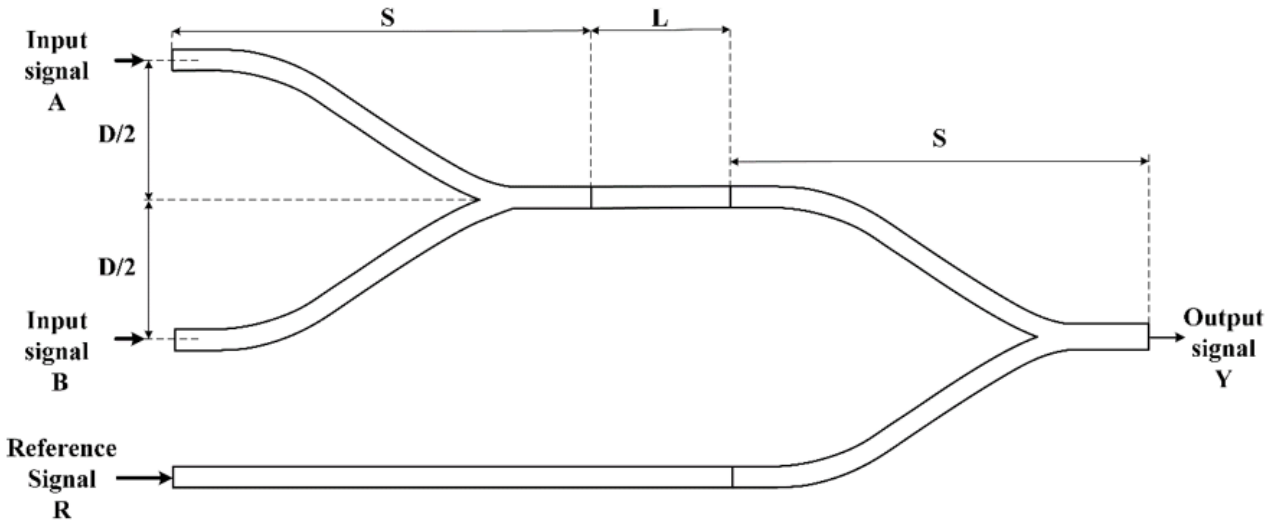

Figure 1

Schematic of NAND, NOR and XNOR using Y-combiner

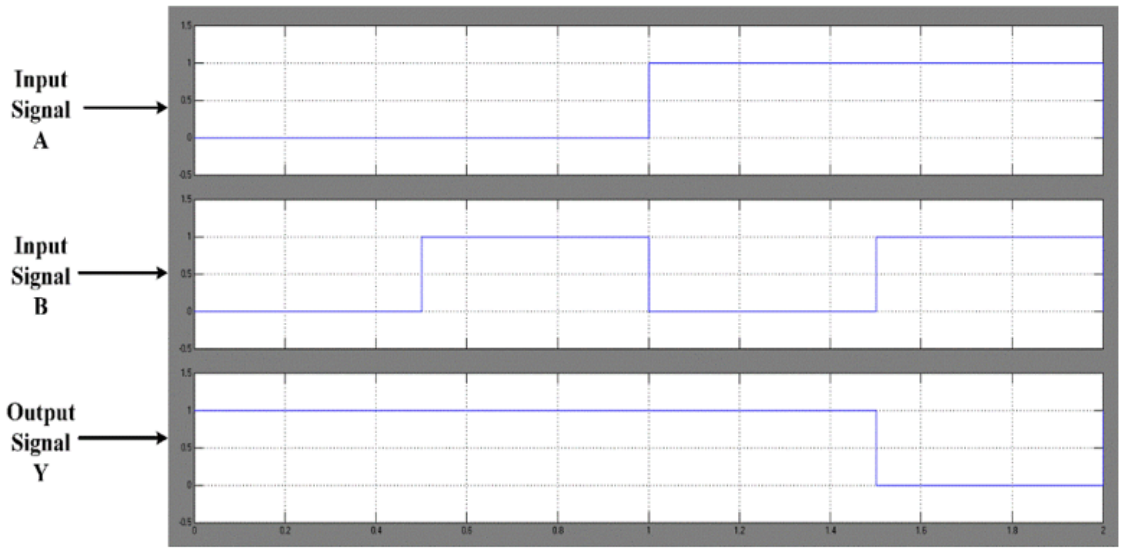

Figure 2

Timing diagram of all-optical NAND gate obtained using MATLAB

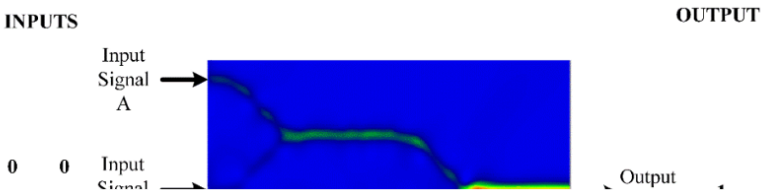

Figure 3

Light propagation across NAND gate for all input signal combinations

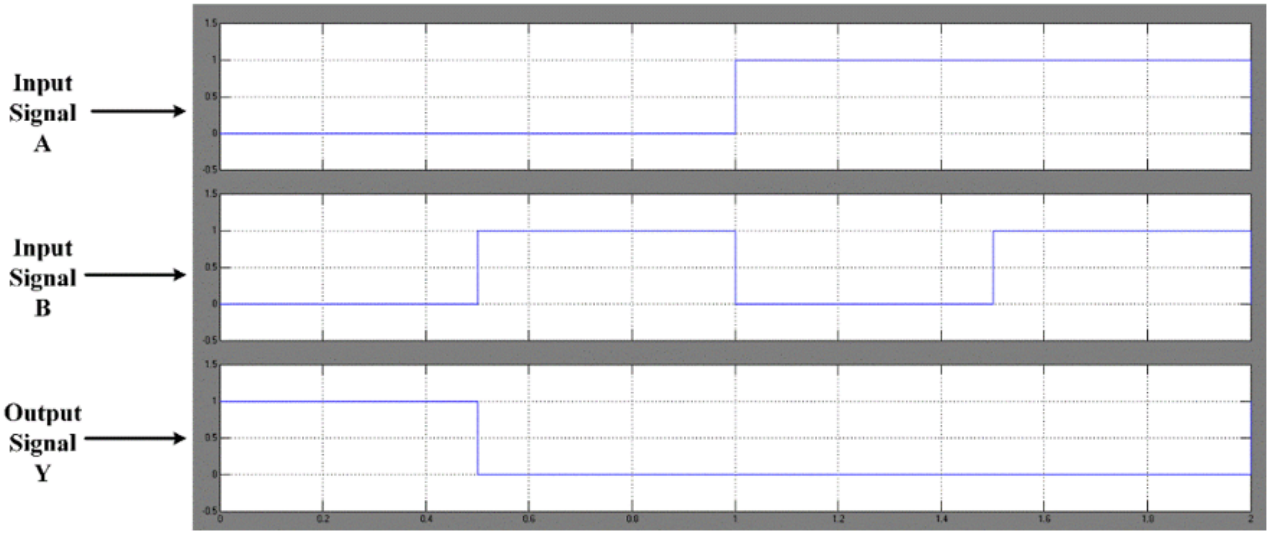

Figure 4

Timing diagram of NOR gate using MATLAB

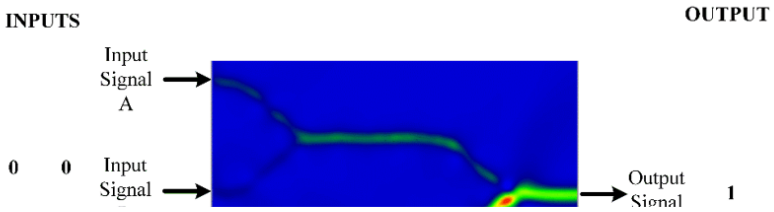

Figure 5

Light propagation across NOR gate for all input signal combinations

Figure 6

Timing diagram of all-optical XNOR gate using MATLAB

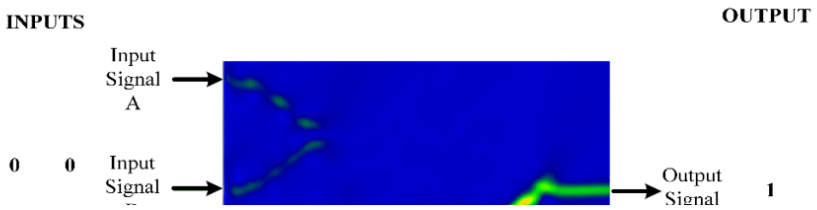

Figure 7

Light propagation across XNOR gate for all input signal combinations