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Design and Energy Analysis of a New Fault-Tolerant SRAM Cell in Quantum-dot Cellular Automata

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Abstract

Quantum-dot cellular automata (QCA) is an emerging technology proposed in response to the limitations of CMOS technology. Moreover, static RAM (SRAM) is a crucial part of memory design, and efficient RAM design can play a significant role in this regard. This paper proposes a fault-tolerant QCA SRAM cell based on QCA three- and five-input majority gates. A novel structure of QCA-RAM based on a fault-tolerant five-input majority cell is proposed, which outperformed its counterparts in terms of complexity, area, and total energy dissipation. The proposed design is implemented on a single layer and does not require any rotated cell, which significantly improves the manufacturability and robustness of the design. Furthermore, our design can tolerate a single omission fault. Our majority gate improves complexity, area, and energy dissipation, on average, by 54 %, 68 %, and 67 % in 1 Ek, respectively, as compared to its previous counterparts. The proposed fault-tolerant SRAM cell improves the complexity, area, and total energy dissipation by almost 13 %, 25 %, and 35 % in 1 Ek, respectively, as compared to its state-of-the-art QCA-based single-layer fault-tolerant counterpart.

Keywords: Quantum-dot cellular automata; memory design; fault tolerance, SRAM; single layer; energy dissipation analysis

1 Introduction

The VLSI chip design industry has developed in recent decades. Following the Moore's law, the size of the transistors has reduced to the nanoscale, while the number of computations performed per unit of time increased immensely [1][2]. In general, to design VLSI circuits, the critical performance parameters such as speed, area, complexity, power consumption, and reliability should be considered as the portable electronic devices face issues such as limited battery lifetime and excessive power consumption [3][4][5]. Supply voltage scaling has been a unique method for reducing overall power dissipation [6]. The energy dissipation within the VLSI chips is due to the interconnects and transistors. The chip designers have proposed many techniques such as charge recovery and energy recapturing to mitigate energy dissipation.

Moreover, by reducing the feature size, reliability and fault tolerance have been raised as critical issues in modern chips [7]. As a result, to address this issue, circuit designers introduced fault-tolerant designs. Nowadays, there are many efforts to this issue. However, it is worth noting that different applications come with different requirements. Detecting and tolerating faults has been well studied and is an area of research in circuit design [8][9].

Faults in QCA circuits can occur due to the production process and misalignment of cells on a surface. Considering the very small size of QCA cells and the high accuracy required for the cell alignment, these defects can be introduced during the deposition phase. The deposition phase is divided into cell omission, extra-cell deposition, and cell displacement [10]. Thus, fault tolerance is crucial for the design and manufacturing of QCA integrated circuits.

This paper proposes a fault-tolerant three-input majority gate and a modified fault-tolerant five-input majority gate. Then, with the use of the proposed building blocks, we design a QCA-based SRAM cell. The advantages of the presented design compared to the other SRAM cells are its smaller area, lower cell count, and lower energy consumption. Moreover, we do not use any rotated cells in the proposed SRAM cells, facilitating the fabrication process and lowering costs.

The remainder of this paper is organized as follows: Section 2 reviews the QCA preliminaries. The previous works are discussed in Section 3. Section 4 describes the implementation of proposed area-efficient fault-tolerant QCA logic gates. Simulation results and comparisons are presented in Section 5. Finally, Section 6 concludes the paper.

2 QCA Preliminaries

There are two different positions for electrons inside a QCA cell representing 0 or 1 logic. Given the quantum-mechanical mechanism, the electrons can tunnel between the dots and achieve cell polarization of $P = -1$ (logic 0) or $P = 1$ (logic 1) as illustrated in Figure 1 (a). The polarity can be defined through Eqn. 1, where i is the probability of the presence of an electron in quantum-dot i [11][12][13][14].

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_3 + \rho_2 + \rho_4} \quad (1)$$

The coulomb energy interaction force between the two electrons in each cell is calculated by Eqn. 2 [15].

$$E_{ij} = \frac{K \times q_i q_j}{r_{ij}} (J) \quad (2)$$

where E_{ij} is the kink energy, $K = 9 \times 10^9 J.m/C^2$ is the Coulomb constant, q_i and q_j are electric charges ($1.6 \times 10^{-19} C$), and r_{ij} is the distance between two electric charges i and j .

$$K \times q_i q_j = 23.04 \times 10^{-29} \quad (3)$$

The electrostatic energy applied to electrons $q_i q_j$ are calculated by Eqn. 4.

$$U_{T_i} = \sum_{i=1}^n E_{ij} \quad (4)$$

In the QCA technology, inverter and majority gates are two essential gates for logical calculations, as shown in Figures 2 (a) and (b). The majority gate votes among the input cells and propagates the majority polarization of the inputs to the output cell. Assuming that the inputs are a, b and c, the logic function of the majority gate is expressed in Eqn. 2. By fixing one of the inputs to binary ‘0’ or ‘1’, the majority gate turns into a logic “AND” or “OR” gate, respectively [12][13][14][16][17].

$$Maj(A, B, C) = AB + BC + AC \quad (5)$$

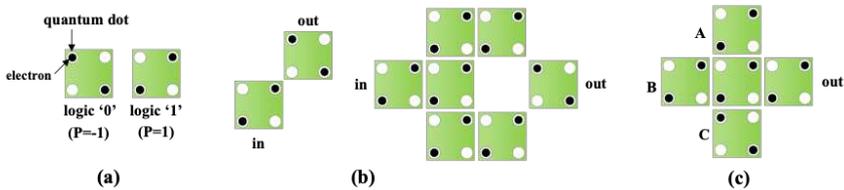


Fig. 1 QCA logic for (a) QCA cells representing logic ‘0’ and logic ‘1’ (b) QCA inverter gate (c) QCA three-input majority gate

The clock signal is the only source of power in QCA circuits. The clocking mechanism is used in pipelining and determining data direction. The mechanism consists of four-phase clock signals, used to propagate data through the logic circuits [12][13][14][16][17][18]. The clocking mechanism consists of the switch, hold, release, and relax phases, as illustrated in Figure 2.

Another important issue is QCA circuit is wire crossover. Generally, there are three QCA crossovers methods: multi-layer crossover, coplanar crossover, and different phase crossover [10] as shown in Figure 3.

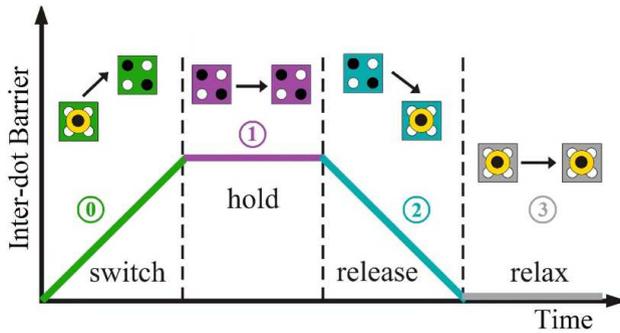


Fig. 2 Clocking zones in QCA designs

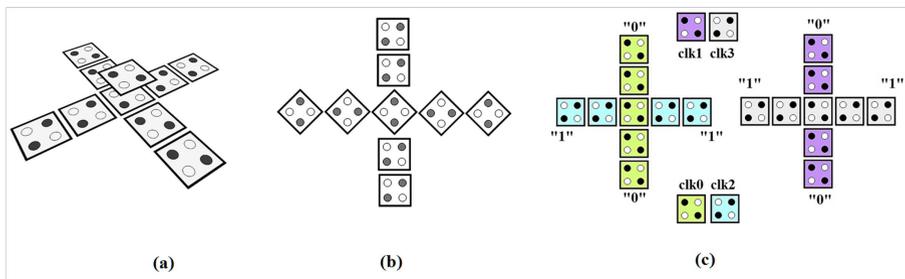


Fig. 3 QCA wire crossing (a) Multilayer approach (b) Coplanar approach (c) Different phases approach

In multi-layer crossover, two separate substrates are required to prevent interference between intersecting QCA wires polarization. There have been no reports indicating the implementation of multi-layers crossovers based on semiconductor-QCA circuits. However, a hybrid method for implementing multi-layer crossovers based on molecular-QCA circuits has been introduced in which graphene is used as the substrate, and carbon nanotube is used to create multi-layer crossovers. In the coplanar crossover, a wire with normal cells crosses another wire with cells rotated by 45 degrees. The binary polarization of the crossing wires does not affect each other. This method is not robust enough, and to mitigate this limitation, another kind of crossover is used in which there is a 180-degree phase difference from the clock signal of one crossing wire to the clock signal of the other wire [10]. In different phase crossover, the crossing wires should have different phases of the clock signal applied to them so the signal values in each wire can cross simultaneously and propagate their values without any conflicts [19].

The defect is a critical issue in QCA cells. The defects in QCA technology occur in the deposition process. Various defects are shown in Figure 4, which can essentially be divided into four categories: cell omission, cell displacement, cell misalignment, and extra cell deposition.

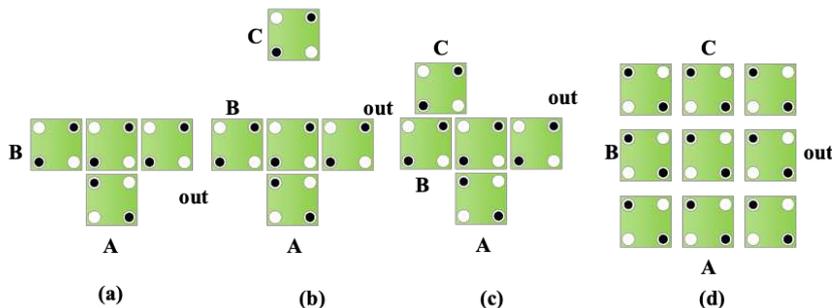


Fig. 4 Defects in QCA circuits (a) cell omission (b) cell displacement (c) cell misalignment (d) extra cell deposition

3 Previous Work

In this section, the previous fault-tolerant QCA majority and RAM cells are reviewed. Majority and inverter gates are two crucial elements in the QCA technology, which serve as the building blocks for extending more complex circuits. Hence, these gates should be designed to accommodate a variety of different applications. Moreover, in some applications such as mission-critical systems, fault tolerance is a top priority, with area, latency, power, and complexity criteria coming next in terms of importance. Besides introducing fault-tolerant designs, decreasing other parameters is crucial. For example, one might need to have a low power device in some applications because maybe power sources are not available for an extended period [20].

3.1 Fault-tolerant three-input majority gates

The authors [21] proposed a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5a). [22] introduced a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5b). [23] provided a fault-tolerant three-input majority gate with higher complexity, occupied a large area, and required two clock phases (Figure 5c). [24] provided a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5d). [25] suggested a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5e). [26] proposed a fault-tolerant three-input majority gate with higher complexity and used rotated cells (Figure 5f). Besides, [25][27] in their designs use rotated cells, which can increase fabrication costs. [27] proposed a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5g). [28] proposed a fault-tolerant three-input majority gate with higher complexity and occupied a large area (Figure 5h). [29] proposed a fault-tolerant three-input majority gate with higher complexity, which occupied a larger area. [30] proposed a fault-tolerant three-input majority gate that increased the complexity and occupied area.

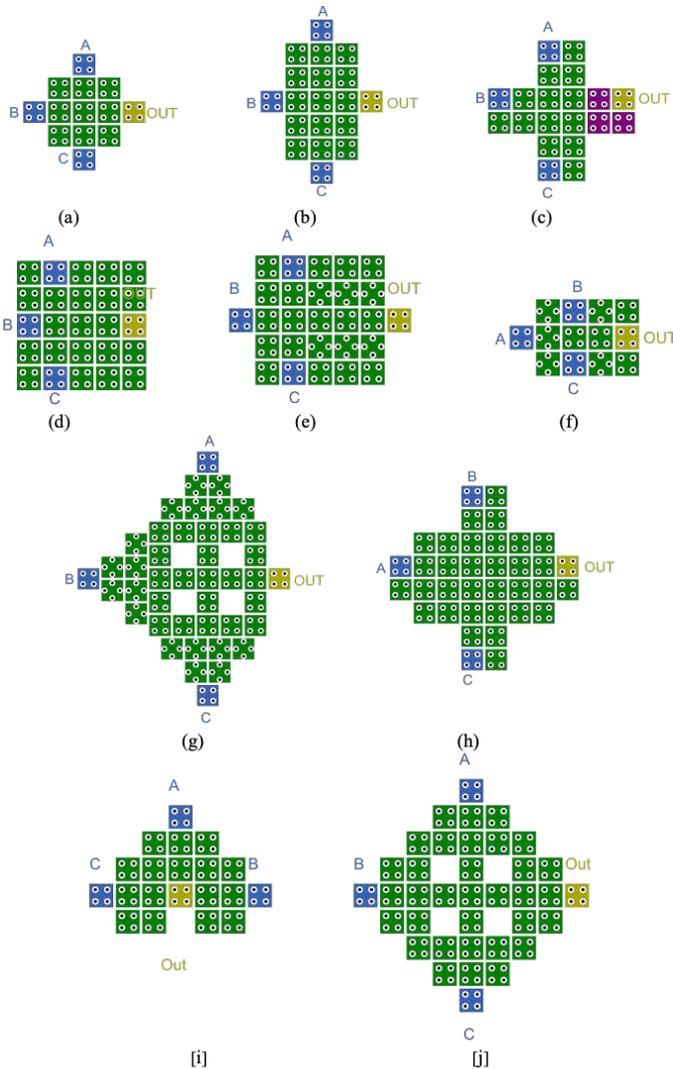


Fig. 5 State-of-the-art Fault-tolerant three-input majority gates. (a) [21], (b) [22], (c) [23], (d) [24], (e) [25], (f) [26], (g) [27], (h) [28], (i) [29], (j) [30]

3.2 Fault-tolerant five input majority gates

There have been many five-input majority gates for embedded applications. Figure 6 (a) shows the design proposed in [31], which is implemented with a high number of cells and occupies a large area. In this work, the single-cell omission was investigated. The main disadvantage of this design is that the output cell is placed in the middle of the design, and hence, it is required to use a multi-layer structure for cascading.

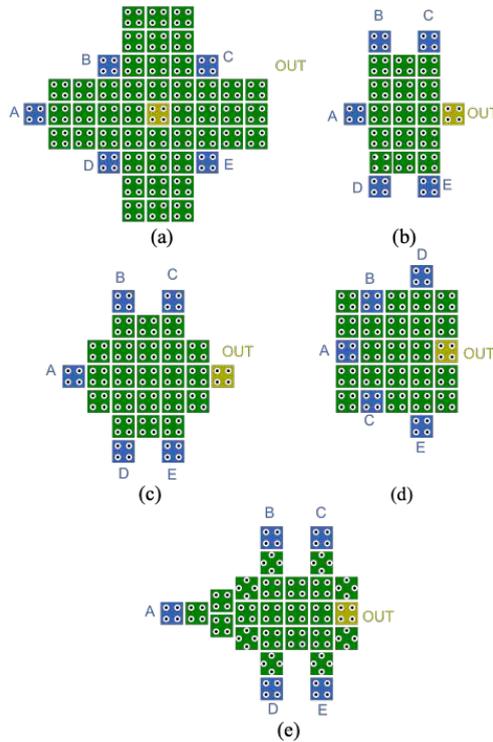


Fig. 6 State-of-the-art Fault-tolerant five-input majority gates. (a) [31], (b) [22], (c) [32], (d) [24], (e) [26]

Another design introduced in [31] is shown in Figure 6 (b). This cell is implemented with an efficient number of cells and has a smaller area compared to the design of [31]. The design presented in [32], which is shown in Figure 6 (c), was implemented with a large area to tolerate single-cell omission. In [24], another fault tolerant 5-input majority was presented, which is shown in Figure 6 (d). In [26] another fault tolerant five-input majority gate was presented (see Figure 6 (e)), which was implemented with a large area and high cell count for tolerating single-cell omission.

3.3 Fault-Tolerant RAM

A fault-tolerant RAM cell based on a five-input majority gate was presented in [26]. This design, which is shown in Figure 7, uses the corner type inverter instead of the fault-tolerant inverter gate in its structure. Besides, this design occupies a large area and suffers from high complexity and high power consumption to implement a fault-tolerant RAM cell.

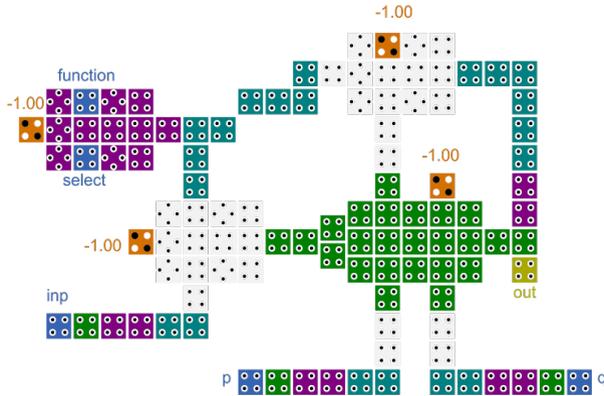


Fig. 7 Fault-tolerant one-bit SRAM cell presented in [26]

4 Proposed Designs

4.1 The proposed fault-tolerant three-input majority gate

The proposed fault-tolerant three-input majority gate is shown in Figure 8.

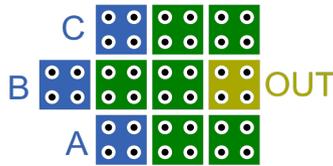


Fig. 8 The proposed fault-tolerant three-input majority gate

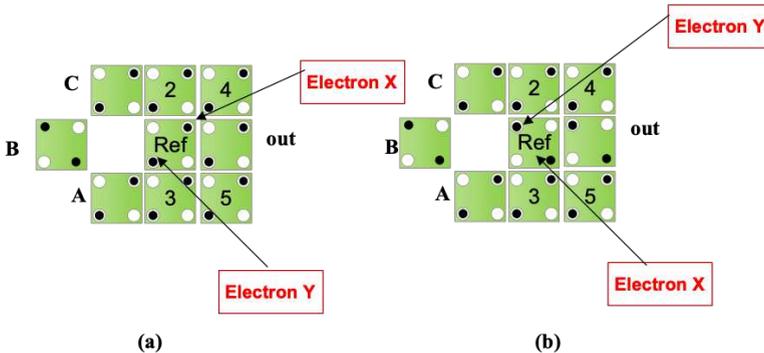


Fig. 9 Calculating output when the middle cell is missing

In this design, we add five cells to the baseline three-input majority to cover single-cell omission fault. It is worth noting that our cell's output is reachable,

and no multi-layer implementation is required for cascading. Furthermore, it does not require any rotated cells, which reduces the complexity and manufacturing costs. In this section, this structure is evaluated using physical verification based on the single-cell omission fault.

Table 1 Kink energies between electrons of Figure 5 (a) based on Electron X

$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \simeq 1.27 \times 10^{-20}$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.15 \times 10^{-20}$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 18.11 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.15 \times 10^{-20}$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{43.05 \times 10^{-9}} \simeq 0.55 \times 10^{-20}$
$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{2.83 \times 10^{-9}} \simeq 8.14 \times 10^{-20}$
$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$	$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$

Table 2 Kink energies between electrons of Figure 5 (a) based on Electron Y

$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{42.5 \times 10^{-9}} \simeq 0.55 \times 10^{-20}$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.15 \times 10^{-20}$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \simeq 1.27 \times 10^{-20}$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.15 \times 10^{-20}$
$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{53.74 \times 10^{-9}} \simeq 0.43 \times 10^{-20}$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$
$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{38.5 \times 10^{-9}} \simeq 0.6 \times 10^{-20}$	$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$

Table 3 Kink energy between the e_1 to e_8 electrons with the X and Y electrons of the output for Figure 9 (a)

Electron X	Electron Y	Sum of energies, Electron X
$U_{T_{11}} = 14.694 \times 10^{-20}(J)$	$U_{T_{12}} = 5.74 \times 10^{-20}(J)$	$U_{T_1} = 20.468 \times 10^{-20}(J)$

Table 4 Kink energy between the e_1 to e_8 electrons with the X and Y electrons of the output for Figure 9 (b)

Electron X	Electron Y	Sum of energies, Electron X
$U_{T_{21}} = 17.84 \times 10^{-20}(J)$	$U_{T_{22}} = 16.61 \times 10^{-20}(J)$	$U_{T_2} = 34.46 \times 10^{-20}(J)$

Considering Tables 1 through 4, the design shown in Figure 5 (a) is more stable compared to the design shown in Figure 5 (b). Considering the calculation results, the output value place in a stable level of energy when one pair electrons place with lower neighboring forces, so based on results of Table 3 output electrons placement in Figure 9 (a) have much stable and design could keep their functionality.

4.2 Analyzing the fault tolerance of the utilized five-input majority gate

The five-input majority gate used for designing the proposed RAM cell was introduced in [33]. This cell is shown in Figure 10. However, the original paper did not report any mathematical proof to show the fault tolerance capabilities of this design. Moreover, the original work exclusively used this five-input majority gate for low-power applications. In this section, this structure is evaluated using physical verification based on the single-cell omission fault. We investigate the single-cell omission on the central voter cell as the energy at the center of the design is critical. Therefore, the worst-case scenario occurs when the central cell is missing. The assumed values of input cells are $a = 1$, $b = 1$, $c = 1$, $d = 0$, and $e = 0$. The kink energies between the electrons in this design are given in Tables 5 to 8. Considering the results, the case shown in Figure 11 (a) is more stable than the one shown in Figure 11 (b). The proposed majority gate implements in symmetric shape that issue help to designers for better physical management. Also, this design has a good output derive and can easily change the next levels of any circuit.

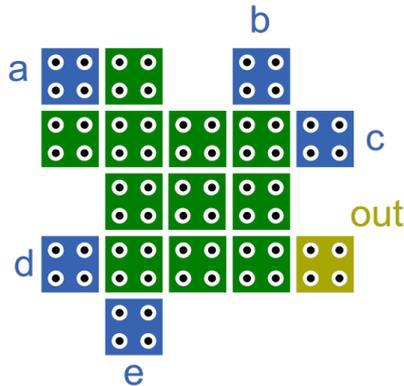


Fig. 10 The five-input majority gate

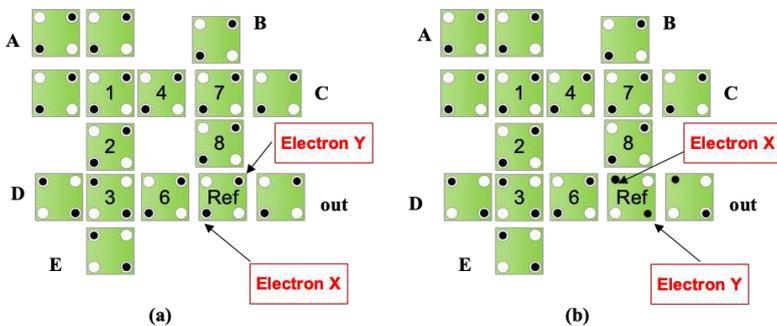


Fig. 11 Calculating output when the middle cell is missing

Table 5 Kink energies between electrons of Figure 5 (a) based on Electron Y

$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{56.57 \times 10^{-9}} \simeq 0.41 \times 10^{-20}$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{62.03 \times 10^{-9}} \simeq 0.37 \times 10^{-20}$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{44.72 \times 10^{-9}} \simeq 0.51 \times 10^{-20}$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{58.03 \times 10^{-9}} \simeq 0.4 \times 10^{-20}$
$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{58 \times 10^{-9}} \simeq 0.4 \times 10^{-20}$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{43.86 \times 10^{-9}} \simeq 0.52 \times 10^{-20}$
$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{44.72 \times 10^{-9}} \simeq 0.51 \times 10^{-20}$	$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{43.91 \times 10^{-9}} \simeq 0.52 \times 10^{-20}$
$U_9 = \frac{A}{r_9} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.27 \times 10^{-20}$	$U_{10} = \frac{A}{r_{10}} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \simeq 0.61 \times 10^{-20}$
$U_{11} = \frac{A}{r_{11}} = \frac{23.04 \times 10^{-29}}{40 \times 10^{-9}} \simeq 0.576 \times 10^{-20}$	$U_{12} = \frac{A}{r_{12}} = \frac{23.04 \times 10^{-29}}{28.42 \times 10^{-9}} \simeq 0.81 \times 10^{-20}$
$U_{13} = \frac{A}{r_{13}} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.152 \times 10^{-20}$	$U_{14} = \frac{A}{r_{14}} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \simeq 1.27 \times 10^{-20}$

Table 6 Kink energies between electrons of Figure 5 (a) based on Electron Y

$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{62.03 \times 10^{-9}} \simeq 0.37 \times 10^{-20}$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{56.57 \times 10^{-9}} \simeq 0.41 \times 10^{-20}$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{43.91 \times 10^{-9}} \simeq 0.52 \times 10^{-20}$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{44.72 \times 10^{-9}} \simeq 0.51 \times 10^{-20}$
$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{43.16 \times 10^{-9}} \simeq 0.52 \times 10^{-20}$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{22 \times 10^{-9}} \simeq 1.05 \times 10^{-20}$
$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{58.03 \times 10^{-9}} \simeq 0.4 \times 10^{-20}$	$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{44.72 \times 10^{-9}} \simeq 0.51 \times 10^{-20}$
$U_9 = \frac{A}{r_9} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.152 \times 10^{-20}$	$U_{10} = \frac{A}{r_{10}} = \frac{23.04 \times 10^{-29}}{42.02 \times 10^{-9}} \simeq 0.55 \times 10^{-20}$
$U_{11} = \frac{A}{r_{11}} = \frac{23.04 \times 10^{-29}}{60.73 \times 10^{-9}} \simeq 0.38 \times 10^{-20}$	$U_{12} = \frac{A}{r_{12}} = \frac{23.04 \times 10^{-29}}{40 \times 10^{-9}} \simeq 0.57 \times 10^{-20}$
$U_{13} = \frac{A}{r_{13}} = \frac{23.04 \times 10^{-29}}{42.05 \times 10^{-9}} \simeq 0.55 \times 10^{-20}$	$U_{14} = \frac{A}{r_{14}} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \simeq 1.15 \times 10^{-20}$

Table 7 Kink energy between the e_1 to e_8 electrons with the X and Y electrons of the output for Figure 5 (a)

Electron X	Electron Y	Sum of energies, Electron X
$U_{T_{11}} = 9.319 \times 10^{-20}(J)$	$U_{T_{12}} = 8.644 \times 10^{-20}(J)$	$U_{T_1} = 17.963 \times 10^{-20}(J)$

Table 8 Kink energy between the e_1 to e_8 electrons with the X and Y electrons of the output for Figure 5 (b)

Electron X	Electron Y	Sum of energies, Electron X
$U_{T_{21}} = 10.699 \times 10^{-20}(J)$	$U_{T_{22}} = 10.024 \times 10^{-20}(J)$	$U_{T_2} = 20.723 \times 10^{-20}(J)$

Considering the calculation results, the output value is placed in a stable energy level when one pair electrons place with lower neighboring forces, so based on Table 7, output electrons placement in Figure 11 (a) have much stable and design could keep their functionality.

4.3 Proposed fault-tolerant RAM design

RAM cells are among the most critical blocks in any electronic system. In the QCA field, RAM cell design is based on two types, which are loop-based and line-based [20]. In the loop-based type, the store mechanism works using a loop containing the clocks' entire zone. Besides, a QCA wire is used to store the previous output like a pipeline in line-based type.

In the QCA field, the loop-based type design is totally used for the SRAM memory cell design. In this structure, the storage mechanism is worked via circling a bit of data within a wire-loop of the QCA cells. In this case, usually, some popular logic functions such as D-latch, SR-latch, multiplexer, and majority gates are used [34].

Despite the great importance of the QCA RAM cell, the fault tolerance aspect of this cell has not been much assessed. This section proposes two fault-tolerant line-based RAM cells with the set/reset ability in QCA. In the proposed design shown in Figure 12, we used the new 3-input fault tolerance majority gate in our structure. The fault tolerance proof of the proposed 3-input majority gate is shown in Tables 1 through 4. The proposed RAM design consists of four three-input majority gates and one five-input majority gate. Moreover, this design has four control lines, including Set, Reset, Select and write/(read). In the primary state, it produces (Set = '0' and Rest = '0') when the select line is activated ('1') and the write/(read) line is set to '1', that the input data will be transmitted to the output, and consequently, the write operation will be performed. Additionally, the read operation is performed by setting the select and the write/(read) signals to '1' and '0', respectively. In the set mode that Set = '1' and Reset = '0' the bit stored on the RAM cell will be set to '1'. Similarly, in the reset mode that Set = '0' and Reset = '1' the bit stored on the RAM cell will be reset to '0'.

It is worth noting that, in the previous fault-tolerant RAM cells [26] corner inverter gate was used instead of a fault-tolerant inverter gate to reduce the cell count. However, based on the fault tolerance design rule, all gates used in a fault-tolerant circuit must be implemented based on fault tolerance structures. Accordingly, using non-robust corner inverters in the RAM cell presented in [26] is a critical violation of the fault-tolerant design. As a result, to address this issue in the proposed design, we use the fault-tolerant inverter gate to keep the privileged requirements.

5 Performance Evaluation

In order to simulate our QCA circuits, the QCADesigner tool [35] is used as the most famous and powerful tool for QCA simulation purposes. The critical parameters used for the simulation are QCA cell size = $18nm$, diameter of quantum dots = $5nm$, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = $65nm$, relative permittivity = 12.9, clock low = $3.8e^{-23}J$, clock high = $9.8e^{-22}J$, clock amplitude factor = 2.000, layer separation = $11.5nm$, and maximum iterations per sample = 100. The simulation

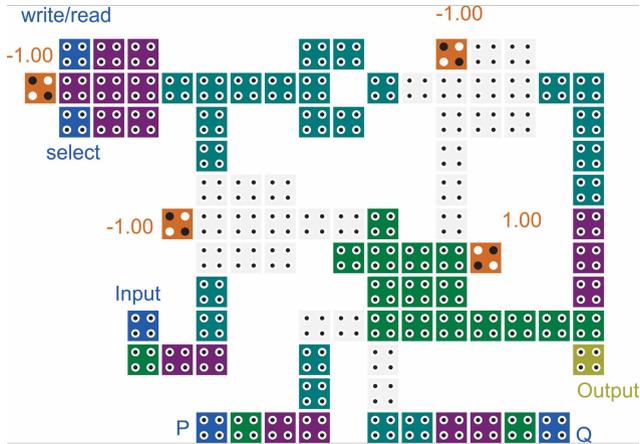


Fig. 12 The structure of the proposed majority-based SRAM cell

results, shown in Figures 16, 17, and 18, validate the functionality of the proposed fault-tolerant RAM cells. Moreover, Tables 5 through 8 compare the proposed fault-tolerant three-input, five-input, and RAM cells designs.

Table 9 Comparing fault-tolerant three-input majority gates in terms of QCA design metrics

Designs	Cell Count	Area	Latency	Type	Omission
[21]	13	0.0096	0.25	Normal	Single
[25]	27	0.0218	0.25	Rotated	Single
[22]	19	0.0135	0.25	Normal	Single
[23]	20	0.0139	0.5	Normal	Single
[27]	44	0.0388	0.25	Rotated	Single
[24]	25	0.0096	0.25	Normal	Single
[28]	36	0.0358	0.25	Normal	Single
[26]	13	0.0057	0.25	Rotated	Single
[29]	20	0.0221	0.25	Normal	Single
[30]	37	0.0317	0.25	Normal	Single
Proposed	10	0.0045	0.25	Normal	Single

Table 10 Comparing fault-tolerant five-input majority gates in terms of QCA design metrics

Designs	Cell Count	Area	Latency	Omission
[31]	50	0.035	0.25	Single
[22]	22	0.016	0.25	Single
[32]	27	0.031	0.25	Single
[24]	27	0.013	0.25	Single
[26]	27	0.035	0.25	Single
[36]	28	0.021	0.25	Single
This work based on [33]	17	0.009	0.25	Single

Table 11 Comparing single layer fault-tolerant SRAM cells in terms of design metrics

Designs	Cell Count	Area	Latency	Type
[26]	107	0.012	1.25	Rotated
Proposed	93	0.09	1.25	Normal

The QCAPro tool is widely used to evaluate the leakage, switching, and total energy dissipations of the QCA circuits [37]. Tables 12, 13, and 14 present the energy dissipation analysis of the proposed fault-tolerant three-input majority gate, fault-tolerant five-input majority gate, and the proposed RAM cells. The simulation results are calculated in three levels of distinct tunneling energies ($0.5Ek$, $1Ek$, and $1.5Ek$), considering $2K$ as the conventional operational temperature for QCA energy analysis. Figures 13 and 14 show the thermal map of our designs at $2K$ temperature and $1Ek$. While Figure 15 shows the thermal map of the proposed fault-tolerant RAM cell alongside some state-of-the-art designs at $2K$ temperature and $1Ek$. It is worth pointing out that the darker the QCA cells are, the more energy is dissipated in the circuit.

Table 12 The energy analysis of the three-input majority gate

3-input	(meV)			(meV)			(meV)		
	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$
[21]	2.61	8.26	15.44	31.22	29.00	26.48	33.83	37.26	41.39
[25]	8.20	26.32	49.60	99.14	91.91	83.65	107.34	118.23	133.25
[22]	4.00	11.77	21.74	49.44	46.66	43.29	53.44	58.43	65.03
[23]	3.69	11.72	22.42	53.56	50.36	46.37	57.25	62.08	68.79
[27]	26.61	69.27	114.65	57.44	45.99	37.25	84.05	115.26	151.90
[24]	6.16	17.76	31.91	61.37	57.46	53.19	67.53	72.21	85.09
[28]	6.70	21.47	41.07	110.75	105.31	98.61	117.45	126.78	139.68
[26]	5.46	15.34	26.45	21.42	18.23	15.43	26.88	33.57	41.87
[29]	3.73	11.94	22.68	52.65	49.36	45.43	56.38	61.3	68.1
[30]	6.92	22.44	43.32	112.16	105.81	97.83	119.08	128.25	141.16
Proposed	1.8	5.7	10.56	17.1	15.6	14	18.9	21.3	24.56

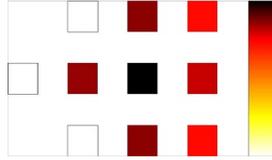
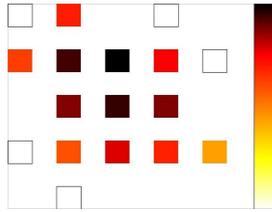
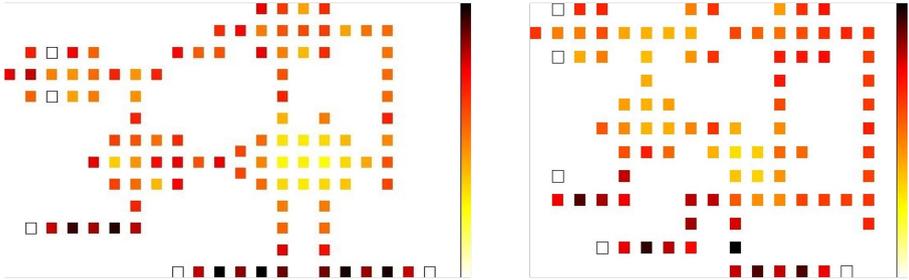
Table 13 The energy analysis of the five-input majority gate

5-input	(meV)			(meV)			(meV)		
	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$
[31]	10.53	32.62	60.68	134.66	127.16	118.42	145.19	159.78	179.11
[22]	4.49	13.41	24.5	45.4	42.18	38.64	49.89	55.59	63.14
[32]	4.97	15.33	28.73	71.07	67.1	62.42	76.04	82.43	91.15
[24]	6.24	18.40	33.08	56.78	52.47	47.97	63.02	70.87	81.05
[26]	5.94	18.07	32.90	53.59	49.35	44.86	59.53	67.42	77.77
[29]	8.84	26.69	49.09	89.3	82.78	75.43	98.14	109.47	124.54
Proposed	2.25	7.69	15.03	38.44	36.22	33.49	40.69	43.91	48.51

The graphical thermal maps of the RAM cells are depicted in Figure 15, which reflect the total energy dissipation of the designs. This diagram attests to the energy efficiency of our proposed structure.

Table 14 The energy analysis of fault-tolerant one-bit SRAM cells

Designs	(meV)			(meV)			(meV)		
	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$	$0.5Ek$	$1Ek$	$1.5Ek$
[26]	0.0462	0.1365	0.2435	0.0264	0.02201	0.0181	0.0726	0.1585	0.2617
Proposed	0.0262	0.0795	0.1425	0.0278	0.0240	0.0206	0.0540	0.1034	0.1631

**Fig. 13** Energy dissipation map for the modified fault-tolerant three-input majority gate at $2K$ temperature with $1Ek$ **Fig. 14** Energy dissipation map for the modified fault-tolerant five-input majority gate at $2K$ temperature with $1Ek$ **Fig. 15** Energy dissipation map for the fault-tolerant SRAM cell at $2K$ temperature with $1Ek$ (a) [26], (b) proposed design

According to Figure 15, it can be concluded that our design has much lower energy dissipation in comparison to the previously reported designs. Appropriate cell arrangements and avoiding rotated cells in the proposed design are the most important reasons for such minimized energy consumption.



Fig. 16 Simulation results of the fault tolerance three-input majority gate

In an objective comparison of the total energy dissipation (over all of the possible vector pairs) to the previously reported fault-tolerant QCA SRAM Cells, our proposed design dissipates, on average, 26 %, 35 %, and 38 % lower energy in $0.5Ek$, $1Ek$, and $1.5Ek$ tunneling energy levels, respectively.

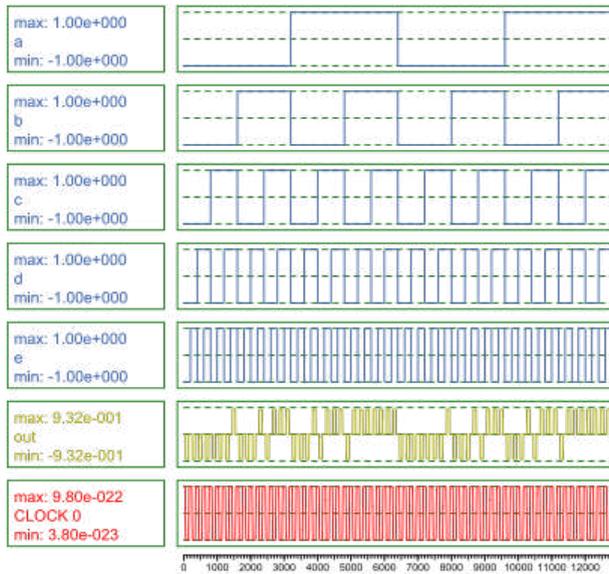


Fig. 17 Simulation results of the fault tolerance five-input majority gate

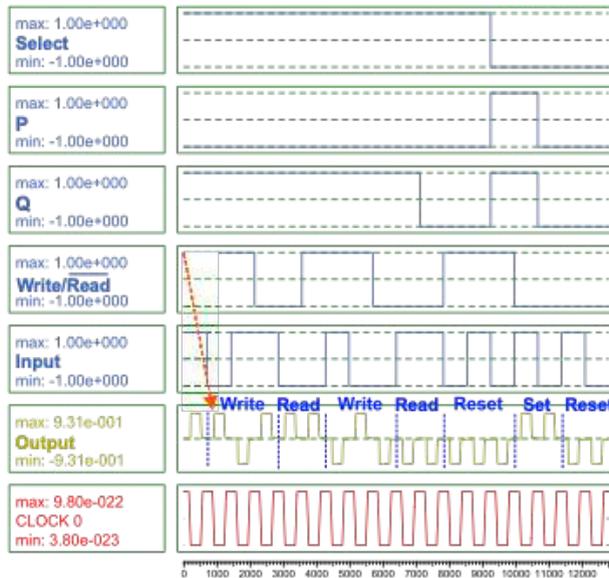


Fig. 18 Simulation results of the proposed fault-tolerant one-bit SRAM cell

6 Conclusion

In this paper, we proposed a fault-tolerant three-input majority capable of tolerating a single-omission fault. Our design, has less complexity, smaller area, and lower energy consumption compared to the other state-of-the-art implementations. Besides, we used a square shape for the proposed fault tolerant three input majority, which can help designers to develop with low garbage milieu in the cheap area. Accordingly, we designed a new fault-tolerant RAM cell with high efficiency regarding complexity, area, and energy consumption. Finally, comparing to the state-of-the-art QCA-based single-layer fault-tolerant SRAM cells, we achieved considerable improvements in terms of complexity, area, and total energy dissipation by 13 %, 25 %, and 35 % in $1Ek$, respectively.

Declaration

Conflict of Interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

Ethical Approval This article does not contain any studies with human participants performed by any of the authors.

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