Three-Dimensionally and Stackable C-Axis-Aligned Crystalline Indium-Gallium-Zinc Oxide Field-Effect Transistor with Gate Length of 6.8-nm

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Three-Dimensionally and Stackable *C*-Axis-Aligned Crystalline Indium-Gallium-Zinc Oxide Field-Effect Transistor with Gate Length of 6.8 nm

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Abstract— Hardware is required to be further miniaturized aiming at advancement of the Internet of things and artificial intelligence. Widely used Si transistors, which have achieved miniaturization on the order of 10 nm, are apparently difficult to further miniaturize, and stacking techniques have been developed as a breakthrough. Our IGZO FETs have a gate length of 6.8 nm or less owing to the wide band gap of IGZO and an optimized transistor structure, and can be highly integrated by a contact formation technique.

INTRODUCTION

In the history of advancement of complementary-metal-oxide-semiconductor (CMOS) technologies, conventional miniaturized planar field-effect transistors (FETs), especially 32/28 nm node devices and smaller ones, have already reached the limits of accuracy of patterning, and many studies have examined FETs having three-dimensional (3D) gate structures such as Fin FETs and gate-all-around (GAA) transistors, rather than planar FETs [1–2] (Fig. 1). For higher integration, higher performance, and lower power consumption, techniques for three-dimensionally stacking FETs have been actively studied. In such 3D stacking techniques, including monolithic stacking and bonding, reducing the footprint of devices formed in each layer is important for improving the degree of integration; accordingly, the technology node and the degree of integration of the devices fabricated in a back-end-of-line (BEOL)

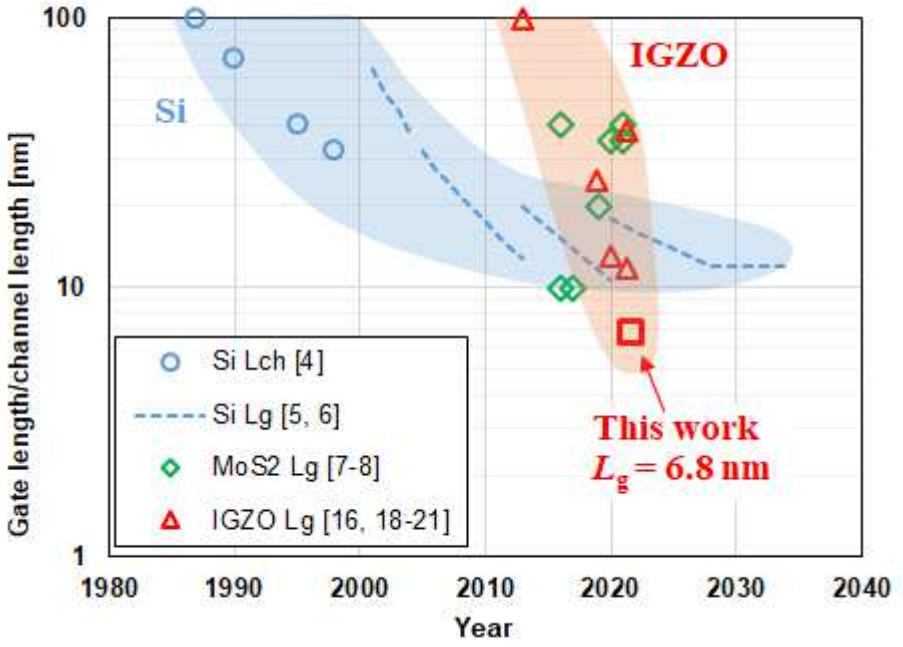

Fig. 1 | Changes in channel length (L_{ch}) or gate length (L_g) in SiFET, MoS_2 FET, and IGZO FET

process are expected to be as close to those of the most advanced Si CMOS circuit as possible. As materials and techniques for stacking FETs over a CMOS circuit, carbon nanotubes, two-dimensional materials, polycrystalline Si, and bonding have been proposed, for example [3]. However, a technique which fulfills all the requirements, including a low-temperature process applicable to a BEOL process, a technology node close to that of a Si CMOS circuit [5–6], excellent on/off characteristics, and lower power consumption, is under development.

As one response to these technical needs, Indium–gallium–zinc oxide (IGZO), have been attracting attention. IGZO typically has a wider band gap ($E_g > 3$ eV) than Si ($E_g = 1.1$ eV), and is a promising material for enabling low-power devices which cannot be obtained only with Si. IGZO has been often used mainly for ultra-low-power displays [9–11]. Because IGZO FET can be stacked monolithically over a Si CMOS circuit by a low-temperature process (< 450°C), various applications of IGZO as a channel material for low-power devices have been reported [12–17]. Of several types of IGZO, *c*-axis-aligned-crystalline IGZO (CAAC-IGZO) which has high crystallinity only in the *c*-axis direction has been getting attention because of its unique crystal structure and high thermal and structural stability as well as ease of sputter deposition [18–19]. In recent years, miniaturization of IGZO FETs has also been actively studied with their application to LSI in view [20–21]. However, when the thickness of a gate insulating film (GI) is reduced according to the scaling law along with miniaturization of the FET, GI leakage might increase to make the IGZO FET compromise its advantage, the low power consumption [22–23]. Furthermore, the carrier concentrations in source, channel, and drain regions are required to be adequately controlled in short channel FETs [24]; however, V_OH, which is a defect generated by bonding of remaining hydrogen to an oxygen vacancy (V_O) to serve as a donor source in an IGZO film [25], is diffused to react in IGZO by thermal budget. Thus, in short channel FETs, a short circuit easily occurs in an n^+ region between the source and drain electrodes, which hinders achieving adequate on/off characteristics. It is accordingly important to develop a devised process capable of controlling distribution of V_O and hydrogen so that short channel FETs can be fabricated using IGZO in their channel layers. In this article, we fabricated a miniaturized IGZO FET having a trench-gate-self-aligned (TGSA) structure by a low-temperature process (< 450°C) [26-27]. Cross-sectional scanning transmission electron microscope (STEM) observation showed that the fabricated CAAC-IGZO FET had a gate electrode length (L_g) of 6.8 nm and a channel width (W) of 32.1 nm. As a fabrication process of CAAC-IGZO FETs, we developed a process in which oxygen is selectively supplied to only the channel region to form a junctionless transistor having $n^+/n^-/n^+$ regions between the source and drain electrodes. The amount of carriers accumulated in the channel region can be controlled by a top gate electrode, which covers a channel side wall as in a Fin FET. IGZO FETs are of an accumulation type and thus have a small characteristics length between the source/drain and the channel [28]. As a result, when including IGZO, even a junctionless, short channel FET in which the Fermi level only slightly differs between the source/drain and the channel can more easily achieve a high on/off ratio than inversion SiFETs. A bottom gate electrode is provided under the channel separately from the top gate electrode in our FET; thus, the threshold voltage (V_{th}) can be adjusted to a desired value by changing the bottom gate voltage (V_{bs}). The IGZO FETs having these features are less likely to be affected by short channel effects [29] and thus our process should be the key to contributing to further miniaturization.

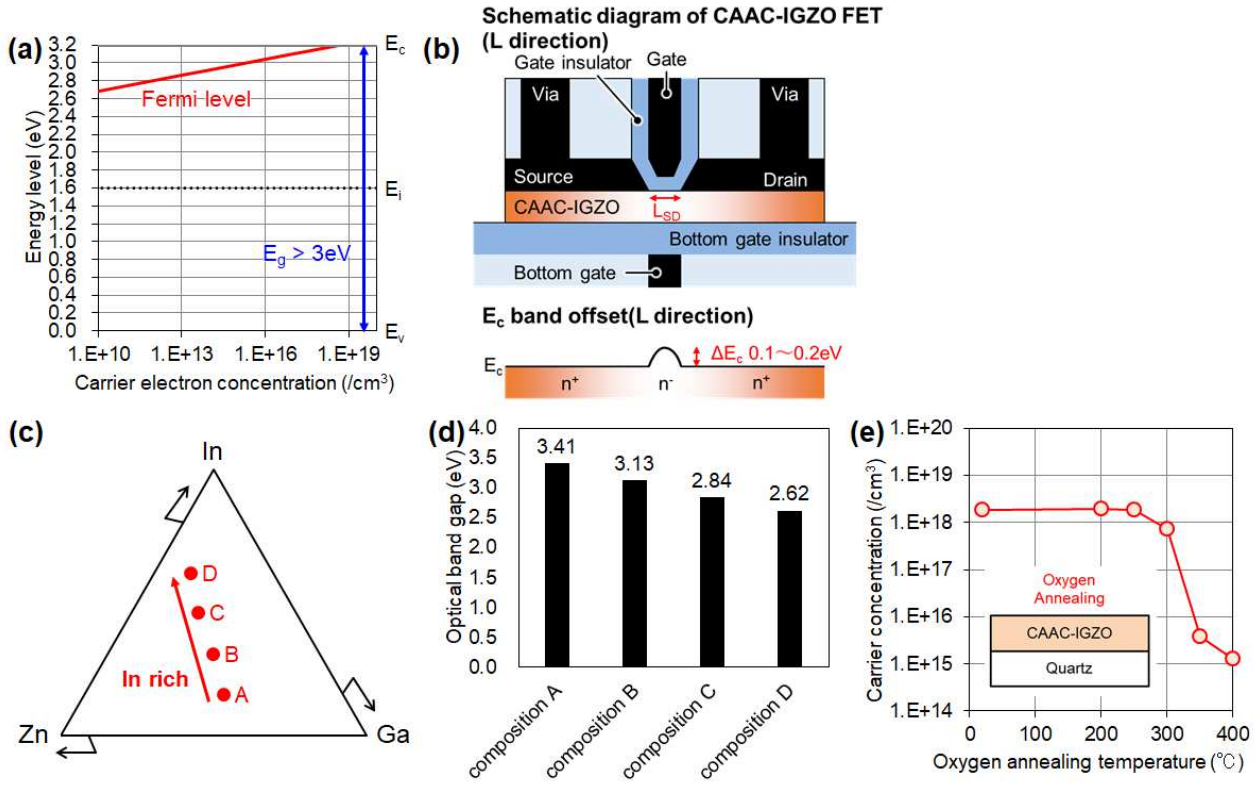

Fig. 2 | Data on various fundamental physical properties of IGZO. (a) Relation between the carrier concentration and the Fermi level, which was calculated from $n = N_c \exp((E_f - E_c) / k_B T)$ where n represents the carrier concentration, N_c represents the density of state in the conduction band (set to 5×10^{18} /cm^3), E_f represents the Fermi level, E_c represents the energy at the conduction band minimum, k_B represents the Boltzmann constant, and T represents absolute temperature (set to 300 K). **(b)** A schematic cross-sectional diagram of an CAAC-IGZO FET in the L_{ch} direction and a schematic band offset diagram of the conduction band in the same direction. **(c)** A phase diagram of IGZO. A, B, C, and D are in order of increasing In richness. **(d)** Optical band gaps of IGZO with the compositions A, B, C, and D. **(e)** Carrier concentrations in CAAC-IGZO thin films after annealing in an oxygen atmosphere. The carrier concentration of the CAAC-IGZO films had been increased by Vo and VoH formation.

PHYSICAL PROPERTIES OF CRYSTALLINE IGZO

Despite being oxides, IGZO, ZnO, and other materials have the properties of semiconductors. The carrier type of many kinds of oxide semiconductor is an n-type. Although p-type oxide semiconductor has also been studied, their performance is inferior to n-type oxide semiconductor [30].

Device simulation results of IGZO FETs have already revealed that FET characteristics with a high on/off ratio can be obtained when the donor concentration in a channel region of an IGZO film is kept at approximately 10^{16} /cm^3 to 10^{17} /cm^3 or lower [31]. For example, the Fermi level (E_c–E_f) when the carrier concentration is 10^{16} /cm^3 is approximately 0.2 eV, indicating n$^-$-type conductivity. In a short channel FET, even in the case where the channel region has a low carrier concentration, the conduction band minimum of the channel region is lowered by the conduction band lowering effect, so that a conduction band offset between the source/drain region and the channel region is reduced [32]. Accordingly, an FET including IGZO can be regarded as a junctionless accumulation transistor with an n$^+$/n$^-$/n$^+$ structure in which the channel region is of an n$^-$ type and the source and drain regions are of an n$^+$ type (Figs. 2(a) and 2(b)).

The band gap of IGZO is slightly dependent on its composition, i.e., In: Ga: Zn ratio, but is approximately larger than 3 eV when the In: Ga: Zn ratio is around 1:1:1 or the Ga ratio is higher than that in the composition In: Ga: Zn = 1:1:1 (Figs. 2(c) and 2(d)). Because of such a wide band gap, an CAAC-IGZO FET has a

high breakdown voltage and other features, a notable one of which is an extremely low off-state current. Typical FETs can have an increased current amount by having an increased *W*, whereas CAAC-IGZO FETs cannot have an off-state current above the lower detection limit of a usual parameter analyzer even when the *W* is extremely large. In some reports, a circuit dedicated for measuring the low off-state current was fabricated to reveal an extremely low off-state current of an CAAC-IGZO FET [33]. Such low-off-state-current characteristics have been observed in miniaturized CAAC-IGZO FETs as well [34]. By including FETs with the above feature, memory devices can retain data for a long time.

As an origin of donor states in IGZO, V_OH in which hydrogen is bonded to V_O has been reported [25]. Oxygen and hydrogen are respectively a constituent element and a ubiquitous element and are thus very hard to control. Accordingly, controlling the amounts of hydrogen and oxygen around IGZO is of importance. By contrast, a metal in contact with IGZO needs to avoid getting oxidized [24]. Blocking hydrogen by surrounding an CAAC-IGZO FET with SiN_x or the like has been reported to increase the reliability [35]. In an FET fabrication process, V_O and V_OH are inevitably formed in IGZO of the channel region to increase the carrier concentration. In such a case, supplying oxygen to IGZO of the channel region can cure V_O and V_OH to reduce the carrier concentration. Fig. 2(e) shows experimental results plainly indicating that annealing in an oxygen atmosphere can reduce the carrier concentration of an IGZO thin film which has been increased by V_O and V_OH formation. Since controlling the carrier concentration in the channel region by oxygen annealing is not practical in a miniaturized CAAC-IGZO FET, we have developed a structure and a method in which oxygen is selectively supplied to only the channel region to reduce the carrier concentration in the channel region to an adequate level.

FIN STRUCTURE WITH BOTTOM GATE

In this study, we fabricated a CAAC-IGZO FET having a bottom gate electrode by a TGSA gate last process (Fig. 3(a)) [26-27]. The CAAC-IGZO FET had an L_g of 6.8 nm. As a channel material of the FET, 15-nm-thick CAAC-IGZO with *c*-axis aligned crystallinity was formed. A buffer layer was formed under CAAC-IGZO to block diffusion of oxygen from a bottom gate insulating film (BGI). As the source and drain electrodes, TaN_x was deposed by a sputtering method. TaN_x has a higher compressive stress than CAAC-IGZO [24]. This compressive stress causes distortion in CAAC-IGZO and increases the lattice constant. The increase in lattice constant generates V_O in CAAC-IGZO. Hydrogen enters V_O to form V_OH, so that the region under TaN_x has n-type conductivity. SiN_x as a barrier film was formed around the FET to block entry of hydrogen. Furthermore, a HfO_x film absorbing hydrogen was provided inward from the hydrogen barrier film [35]. By inhibiting hydrogen diffusion through the above process, V_OH formation in the channel region was suppressed. To eliminate V_O, V_O must be terminated by oxygen. Thus, a sputter-deposited AlO_x film was provided over the gate. Oxygen can be diffused from the AlO_x film to CAAC-IGZO. The amount of oxygen can be controlled by adjusting the deposition conditions of the AlO_x film.

Through the above process, the donor concentration was successfully varied between the channel region and the source and drain regions in the FET. In our CAAC-IGZO FET, the electric field therearound can be blocked with the bottom gate electrode as in a GAA structure. It is to be noted that the bottom gate electrode of our FET works independently of the top gate electrode unlike in a typical GAA structure in which the bottom gate electrode works as a usual gate electrode. The bottom gate electrode working independently can shift the V_{th} of the FET, and owing to this feature, the FET can be used for a V_{th} correction circuit, for example [36]. Our CAAC-IGZO FET has a

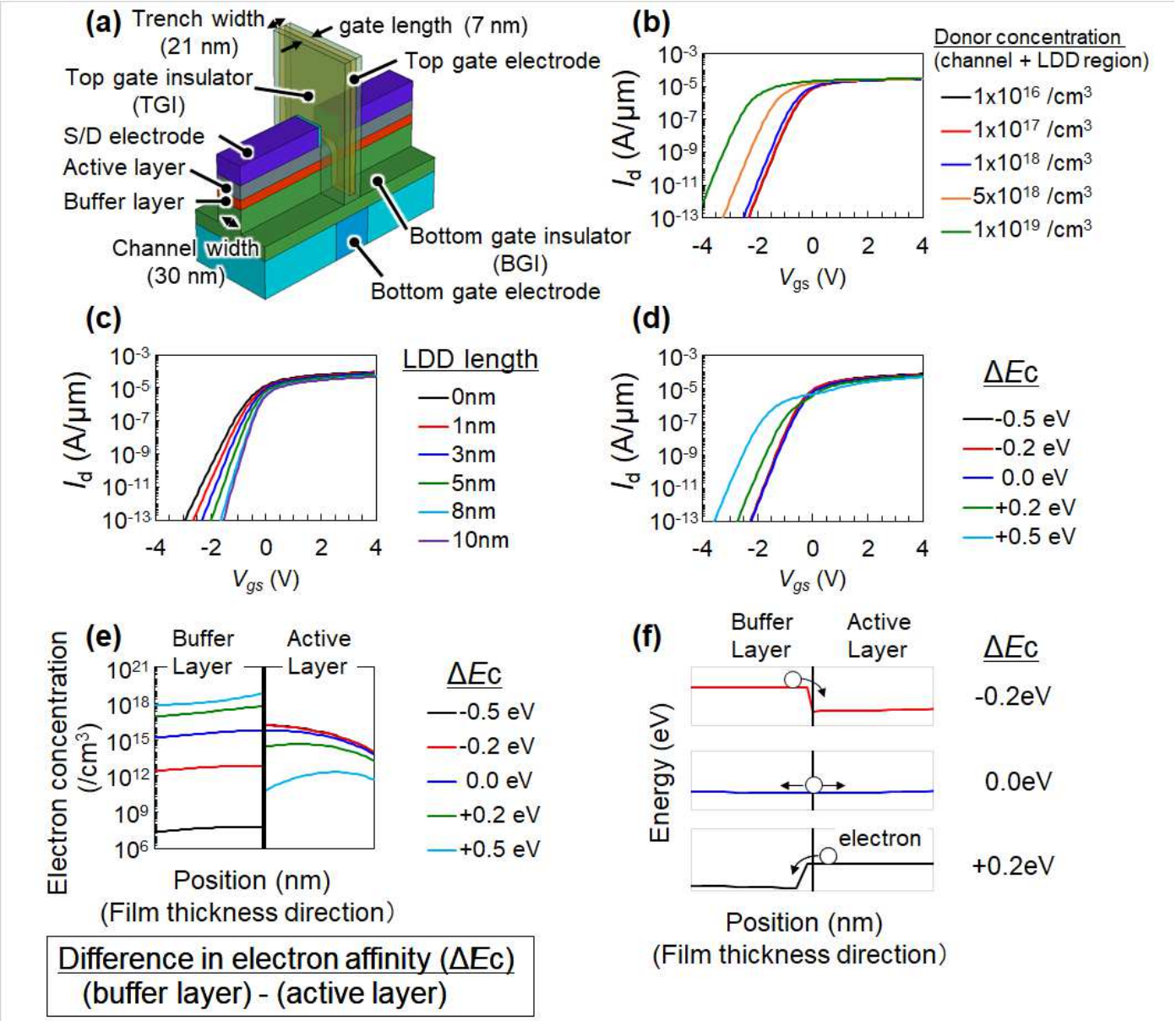

Fig. 3 | **Comparison of device simulation results with various parameters. (a)** A perspective view of a Fin FET with a bottom gate. **(b)** I_d–V_{gs} characteristics with varied donor concentrations of the channel and LDD regions (V_{ds} = 0.1 V, source voltage (V_s) = V_{bs} = 0 V). **(c)** I_d–V_{gs} characteristics with varied LDD lengths (V_{ds} = 0.1 V, V_{bs} = 0 V). **(d)** I_d–V_{gs} characteristics with varied differences in electron affinity (V_{ds} = 0.1 V, V_{bs} = 0 V). **(e)** Electron concentrations with varied differences in electron affinity (at the center of the channel) (V_{ds} = 0.1 V, V_{gs} = −1 V, V_{bs} = 0 V). **(f)** Energies at the conduction band minimum with varied differences in electron affinity (at the center of the channel) (V_{ds} = 0.1 V, V_{gs} = −1 V, V_{bs} = 0 V).

large TGI thickness to prevent gate leakage current. The top gate insulating film (TGI) has a physical thickness of 7 nm (equivalent oxide thickness, or EOT: 5.1 nm) and the BGI has a physical thickness of 40 nm (EOT: 25 nm). Such GI thicknesses are much larger than those of miniaturized FETs of the same size used in SiLSI [37]. This can inhibit gate leakage current despite application of voltage as high as several volts. Conversely, a large GI thickness means weakened control by a gate electric field, which makes it difficult to inhibit the influence of drain induced barrier lowering (DIBL) in a short channel FET. In this study, we attempted fabrication of a miniaturized CAAC-IGZO FET having high current drive capability. In a CAAC-IGZO FET, the influence of impurity scattering is not dominant and thus, the mobility can be increased by increasing the

donor concentration [38]. Therefore, an effective method of enhancing current drive capability is to slightly increase the carrier concentration of the channel region. However, an increase in carrier concentration causes the Fermi level to get close to the conduction band, in which case the V_{th} of a CAAC-IGZO FET is easily negatively shifted and the on/off ratio decreases (Fig. 2(a)). Thus, measures must be taken to obtain a high on/off ratio. In particular, relaxing the drain electric field and enhancing the controllability by the gate electrode are important in a short channel FET. We examined an effective way to refine the process, using device simulation.

First, a method for relaxing a drain electric field was examined. We can vary the donor concentration between regions through well controlled dehydrogenation and oxygen adding treatment. It is thus possible to form a lightly doped drain (LDD) region in order to suppress the drain electric field. Fig. 3(b) shows comparison of drain current (I_d)–gate voltage (V_{gs}) characteristics of FETs having an LDD length of 3 nm and varied donor concentrations. By reducing the donor concentration in the channel and LDD regions, a negative shift in V_{th} can be suppressed. However, the V_{th} ceased to positively shift at approximately 10^{17} /cm^3; thus, to further improve the characteristics, a measure other than reducing the donor concentration is needed. Fig. 3(c) shows comparison of I_d–V_{gs} characteristics of FETs having a donor concentration in the channel and LDD regions of 10^{16} /cm^3 and varied LDD lengths. As can be seen in the graph, a longer LDD length led to a better subthreshold swing (*SS*) and resultantly to a positive shift in V_{th}. This is because the presence of the LDD region relaxes the drain electric field. Nevertheless, normally-off characteristics were not obtained only by taking these measures.

Next, a method for enhancing the controllability by the gate electrode was examined. A typical example of a method for effectively enhancing the controllability by the gate electrode is reducing the thicknesses of the TGI and active layer. However, a reduction in the thickness of the TGI is not preferred because it might increase gate leakage current, contradictory to our aim of minimizing off-state leakage current. Besides, a reduction in thickness of the active layer is not preferred either because it reduces current drive capability, contradictory to our aim of enhancing it. Accordingly, we examined methods other than reducing the thicknesses of the TGI and active layer. To control the oxygen adding process, we form, under CAAC-IGZO, the buffer layer blocking oxygen diffusion from the BGI [24]. Because this buffer layer is inevitable for controlling oxygen diffusion under the status quo, we decided to examine methods in which this buffer layer is utilized to increase the controllability by the top gate electrode.

In the first method, a difference in electron affinity (ΔE_c) between the buffer layer and active layer was utilized. Fig. 3(d) shows comparison of I_d–V_{gs} characteristics with varied ΔE_c. Here, ΔE_c is defined as a value obtained by subtracting the electron affinity of the active layer from that of the buffer layer. When the buffer layer had higher electron affinity ($\Delta E_c > 0$ eV), the FET characteristics curves exhibited a negative shift and included a hump. Fig. 3(e) shows comparison of electron concentration distribution when the V_{gs} was -1 V and the drain voltage (V_{ds}) was 0.1 V. In the case where the buffer layer had higher electron affinity ($\Delta E_c > 0$ eV), the electron concentration of the buffer layer was higher than that of the active layer. This is because electrons will easily move to a layer with higher electron affinity in the case of heterojunction (Fig. 3(f)). Therefore, electrons can be efficiently moved to the active layer by making the electron affinity of the buffer layer lower than that of the active layer ($\Delta E_c < 0$ eV). In this way, only the active layer in IGZO needs to be subjected to the carrier control by the top gate electric field, so that the controllability by the top gate can be increased. In this state, moreover, an

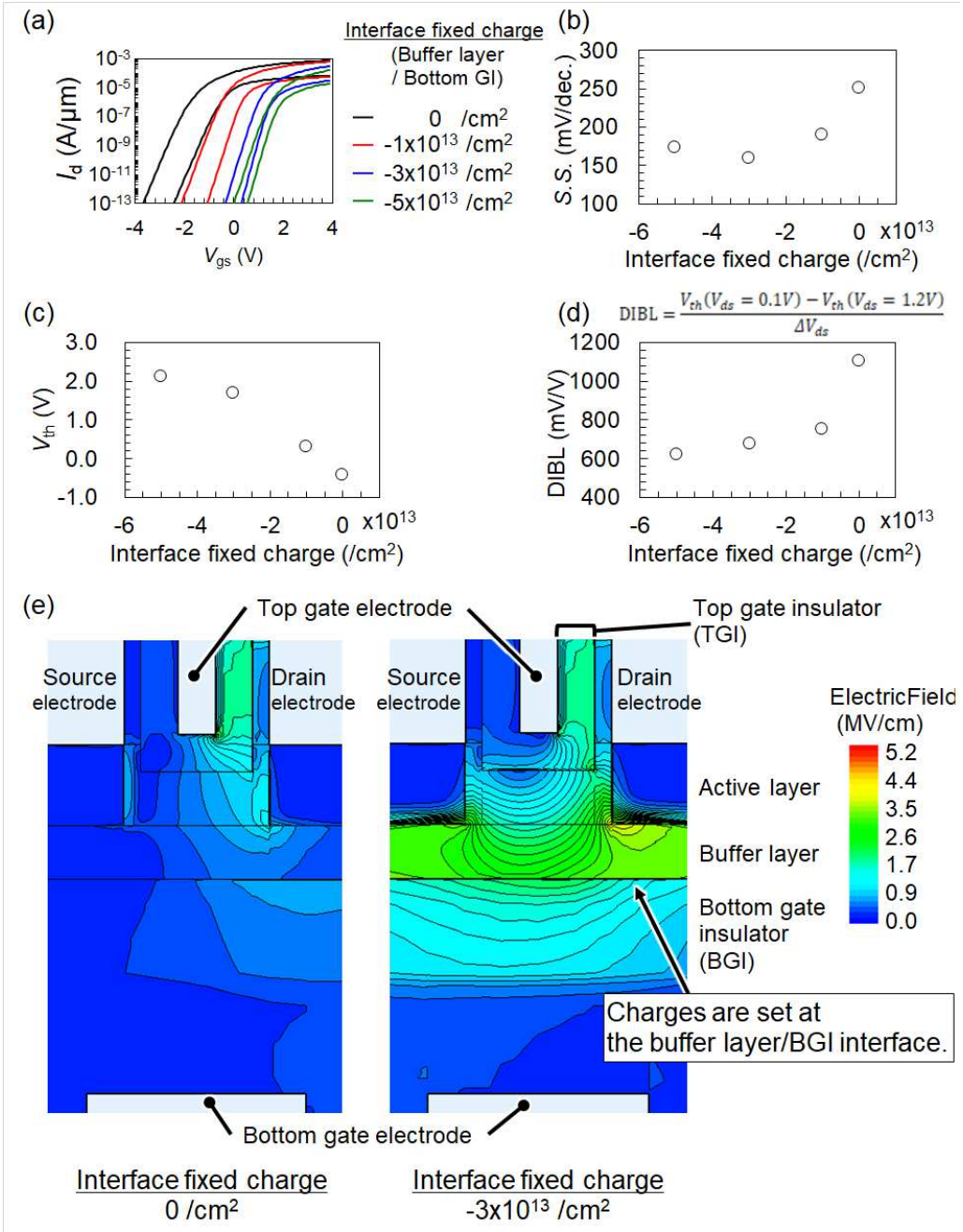

Fig. 4 | Comparison of results of device simulation in the presence and absence of negative fixed charges (V_{bs} = 0 V). (a) I_d–V_{gs} characteristics (V_{ds} = 0.1 V or 1.2 V). **(b)** *SS* (V_{ds} = 0.1 V). **(c)** V_{th} (V_{ds} = 0.1 V). **(d)** DIBL (V_{ds} = 0.1 V or 1.2 V). **(e)** Electric-field intensity distribution (V_{ds} = 1.2 V, V_{gs} = 0 V).

interface between an insulating film and a semiconductor, at which electron traps are easily formed, is present only on the top gate side, so that the influence of electron traps during circuit operation can be reduced.

In the second method, negative fixed charges are formed at the interface between the BGI and the buffer layer. In a typical method for controlling the bottom gate-side electric field, the electric field is controlled with the bottom gate electrode or is increased by reducing the thickness of the BGI. We have already attempted control of the electric field by formation of a bottom gate electrode. However, since the BGI is used as not only an insulating film but also a path for diffusion of oxygen to a wide range, a reduction in the BGI thickness is desired to be avoided. To overcome the insufficiency of the bottom gate-side electric field control

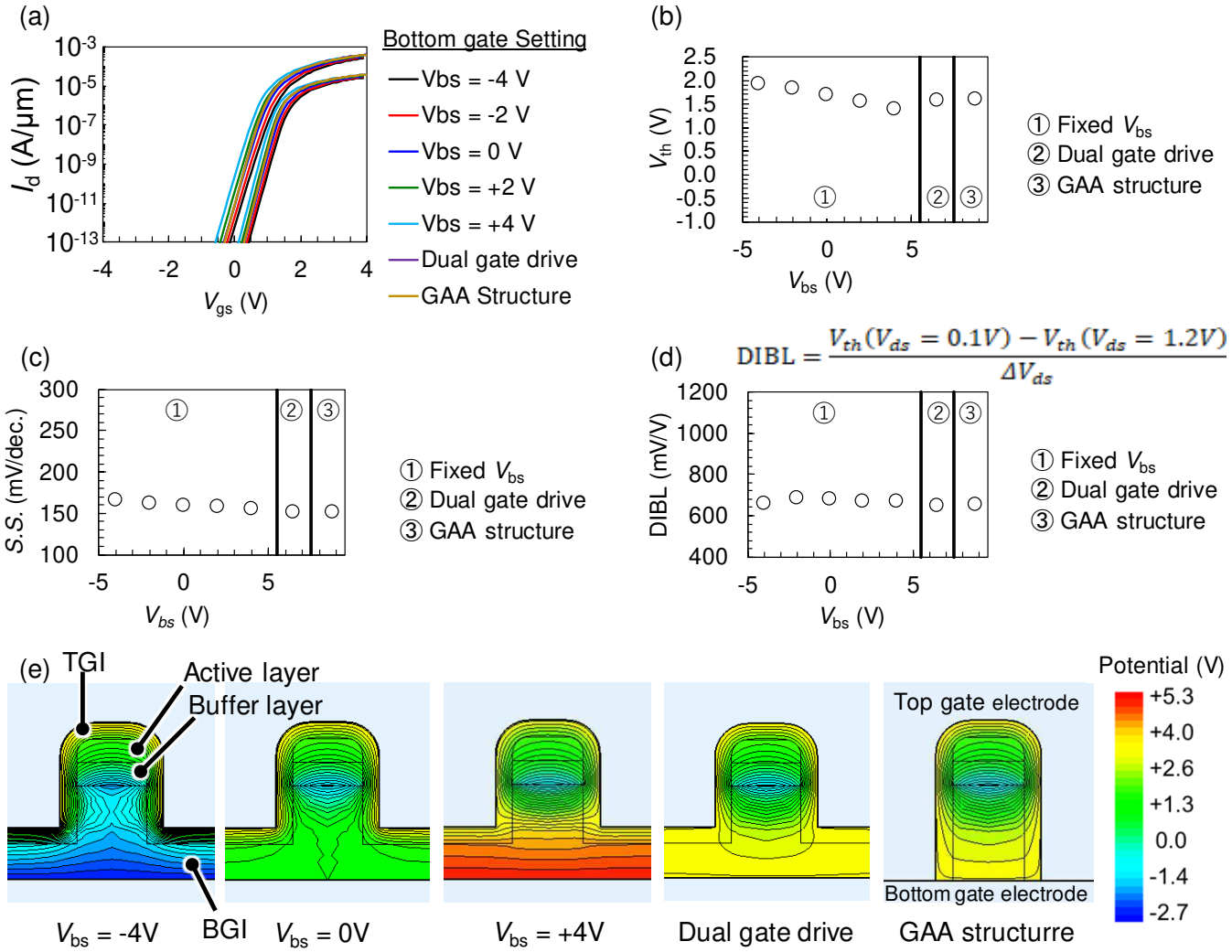

Fig. 5 | Results of device simulation with various bottom gate settings (V_{bs} = 0 V). (a) I_d–V_{gs} characteristics (V_{ds} = 0.1 V or 1.2 V). **(b)** *SS* (V_{ds} = 0.1 V). **(c)** V_{th} (V_{ds} = 0.1 V). **(d)** DIBL (V_{ds} = 0.1 V or 1.2 V). **(e)** Distribution of potential in the *W* direction (V_{gs} = V_{th} + 1 V, V_{ds} = 1.2 V).

with the existing film structure, we examined the method in which negative fixed charges are formed at the interface between the BGI and the buffer layer. Figs. 4(a) to 4(d) show comparison of the I_d–V_{gs} characteristics, *SS*, V_{th}, and DIBL under negative fixed charge conditions. In calculation of V_{th}, a linear extrapolation method was employed. By setting negative fixed charges, the I_d–V_{gs} curve was considerably shifted positively, the SS was improved, and DIBL was substantially saturated. In other words, the controllability by the gate electrode was enhanced and the influence of DIBL was suppressed by setting negative fixed charges. Fig. 4(e) shows electric-field intensity distribution in the presence and absence of negative fixed charges. As shown in the diagram, the presence of negative fixed charges blocked the bottom-gate side drain electric field. It is thus possible to block the bottom-gate side drain electric field by formation of negative fixed charges despite a thick BGI, enabling fabrication of a device that hardly suffers from short channel effect. In addition, the V_{th} of our CAAC-IGZO FET can be shifted by application of freely set voltage to the bottom gate electrode. The CAAC-IGZO FET can also work like an FET having a GAA structure when the potential of the bottom gate electrode is synchronized with that of the top gate electrode. Fig. 5(a) shows comparison of I_d–V_{gs} characteristics with the V_{bs} application mode varied. In the GAA structure, the insulating film between the top

and bottom gate electrodes was etched around the FET to make the top gate electrode come into direct contact with the bottom gate electrode. Under application of constant voltage, V_{th} depended on the V_{bs} as shown in Fig. 5(b). The SS improved in dual gate driving but was not very different from that in the GAA structure (Fig. 5(c)). DIBL was not substantially different between the conditions (Fig. 5(d)). Accordingly, in our CAAC-IGZO FET, the operation mode can be switched to fit the purpose by changing the setting of the bottom gate electrode. Fabrication of this CAAC-IGZO FET in which short channel effect is suppressed will be described in the next section.

PROTOTYPE FABRICATION AND EVALUATION

Figs. 6(a) and 6(b) show cross-sectional STEM images of a CAAC-IGZO FET we prototyped. The cross-sectional images show that our CAAC-IGZO FET has a GAA-like structure in which three surfaces are covered with the top gate and the other surface is covered with the bottom gate and that a fine shape with an L_g of 6.8 nm and a W of 32.1 nm was formed. For higher integration, not only an FET but also lead wiring and other components therearound must be miniaturized. As shown in the plan-view image in Fig. 6(c), the prototype achieved a density as high as 127 Tr/μm^2. The IGZO layer as the active layer was confirmed to have a CAAC structure. Figs. 6(d) and 6(e) show the I_d–V_{gs} characteristics of our CAAC-IGZO FET. As shown in Fig. 6(d), V_{th} = 1.86 V (σ = 0.169 V), SS = 172 mV/dec. (σ = 18 mV/dec.), and g_m = 66 μS/μm (σ = 10 μS/μm) when the drain source voltage (V_{ds}) was 1.2 V, and the DIBL coefficient between V_{ds} = 0.1 V and 1.2 V was 370 mV/V (σ = 134 mV/V). As described above, an adequate on/off ratio was obtained and normally-off characteristics where $V_{th} > 0$ V were exhibited, even with $L_g < 10$ nm. Moreover, the off-state leakage current was below the lower detection limit despite the L_g smaller than 10 nm, and background noise originating from the measurement equipment was observed in the off region. Fig. 6(e) shows the I_d–V_{gs} characteristics when the V_{bs} was increased from −4 V to +4 V in steps of 1 V. The I_d–V_{gs} curve showed a parallel shift at almost equal intervals as the V_{bs} was increased, indicating that only the V_{th} changed. Our CAAC-IGZO FET has a Fin FET-like structure provided with a top gate electrode and a bottom gate electrode. Our CAAC-IGZO FET can have a geometry resembling a GAA structure when in-phase signals are applied to the top gate and the bottom gate, and can make the gates function differently such that a control signal is input from the top gate and V_{th} is controlled by the bottom gate as shown in Fig. 6(e) when power is independently supplied to the bottom gate.

To examine the performance in a logic circuit, a ring oscillator serving as an oscillator circuit was prototyped by serial connection of an odd number of inverters in each of which an n-channel CAAC-IGZO FET was stacked monolithically over a Si p-channel metal-oxide semiconductor (PMOS) circuit (Fig. 6(f)). The oscillation frequency and delay time of the ring oscillator were evaluated. Fig. 6(g) schematically shows the 3D layout of the ring oscillator circuit with an IGZO/Si monolithic stack. This circuit was fabricated by monolithically stacking CAAC-IGZO FETs over SiFETs formed in a front-end-of-line (FEOL) process, as shown in the cross-sectional image in Fig. 6(h). In the evaluation, an output signal V_{osc} of a 51-stage ring oscillator was observed with an oscilloscope. When in-phase signals were applied to the top and bottom gates of the CAAC-IGZO FET, the oscillation frequency was 9.1 MHz as shown in Fig. 6(i), which can be converted into a delay time per stage of 1.1 ns. Fig. 6(j) shows examination results of V_{th} control by the bottom gate in the

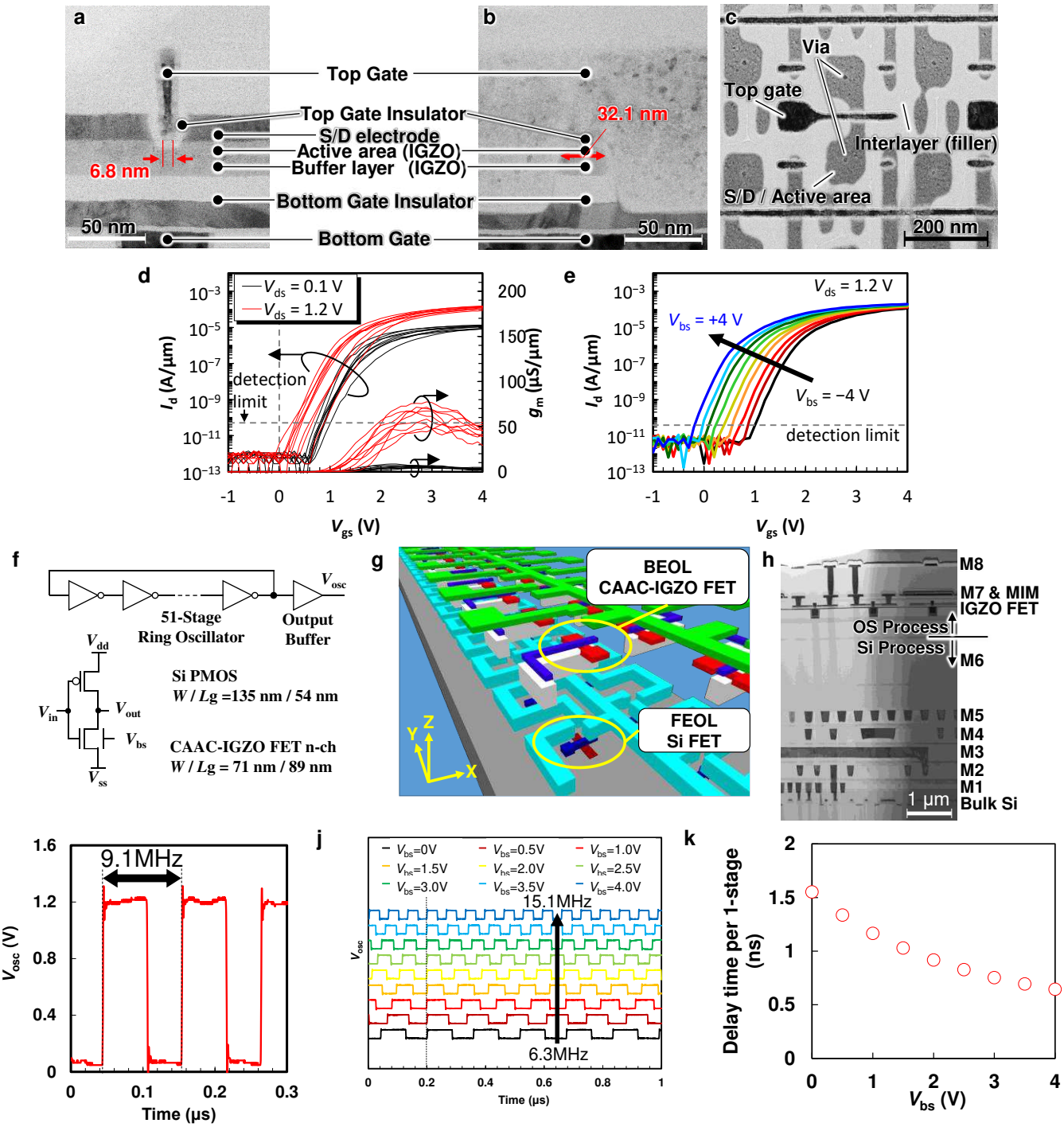

Fig. 6 | Fabricated CAAC-IGZO FET and evaluation results of circuit. (a), (b) Cross-sectional STEM images of our CAAC-IGZO FET (W/L_g = 20 nm/6.8 nm) in the Lch direction (a) and the W direction (b). **(c)** A plan-view STEM image of a CAAC-IGZO FET array (W/L_g = 33.1 nm/19.2 nm) having a density of 127 Tr/μm^2. **(d), (e)** Transfer characteristics of CAAC-IGZO FETs (W/L = 20 nm/20 nm) as a function of V_{ds} (d) and V_{bs} (e). **(f)** A circuit diagram of a ring oscillator fabricated by monolithically stacking n-channel CAAC-IGZO FETs over a Si PMOS circuit. **(g)** A 3D image of an actual layout of the ring oscillator. **(h)** A cross-sectional STEM image of the ring oscillator. **(i), (j)** Output waveforms of the ring oscillator. **(k)** Delay time of the ring oscillator as a function of V_{bs}.

CAAC-IGZO FET. The V_{th} was controlled by independently changing the V_{bs}, and the delay time as a function of V_{bs} was examined. As a result of V_{bs} application from 0 V to 4 V, the oscillation frequency was found to increase approximately 2.4 times and the

delay time per stage was shortened to approximately 0.6 ns. As described above, CAAC-IGZO FETs can be fabricated in a BEOL process and can also be used for a logic circuit combined with a Si PMOS circuit.

Conclusion

A miniaturized TGSA FET having a Fin-type top gate electrode and a bottom gate electrode and including CAAC-IGZO in the channel layer was fabricated. We developed a method for forming a junctionless transistor with the n^- type channel and the n^+ type source and drain regions by appropriately controlling V_O, hydrogen concentration, and band alignment around CAAC-IGZO during the CAAC-IGZO FET fabrication process. The CAAC-IGZO FET formed by this process exhibited excellent normally-off characteristics with a V_{th} of 1.86 V and an *SS* of 172 mV/dec despite the L_g as small as 6.8 nm. We also prototyped a ring oscillator composed of a Si PMOS circuit and CAAC-IGZO FETs formed in a BEOL process, to find out that the ring oscillator operated at an oscillation frequency of 9.1 MHz and with a delay time per stage of 1.1 ns. A junctionless IGZO FETs in which short channel effect is inhibited by the above improvements is expected to be applied to a low-power memory cell array, a selector of a leading-edge embedded memory, an analog amplifier circuit, a high speed logic circuit, and other devices is expected.

Experimental Method

Device simulation

In the calculation of the device characteristics by device simulation, Sentaurus Device manufactured by Synopsys G.K. was used. Other than the varied conditions, the simulation employed the following parameters in principle. For the active layer, the electron mobility was 6 cm^2/Vs, the hole mobility was 0.01 cm^2/Vs, the band gap was 3.2 eV, the electron affinity was 4.7 eV, the donor concentration of the channel and LDD regions was 10^{16} $/cm^3$, and the donor concentration of the source and drain regions was 10^{20} $/cm^3$. For the buffer layer, the electron mobility was 1.5 cm^2/Vs, the hole mobility was 0.01 cm^2/Vs, the band gap was 3.4 eV, the electron affinity was 4.5 eV, the donor concentration of the channel and LDD regions was 10^{10} $/cm^3$, and the donor concentration of the source and drain regions was 10^{10} $/cm^3$. In each layer, the dielectric constant was 15 and the density of state in the conduction band and that in the valence band were 5×10^{18} $/cm^3$. The thickness of the TGI was 7 nm and the dielectric constant thereof was 5.5. The thickness of the BGI was 40 nm and the dielectric constant thereof was 6.6. The work functions of the top gate electrode, the bottom gate electrode, and the source and drain electrodes were 4.7 eV, 5.0 eV, and 4.5 eV, respectively. The trench gate had a width of 21 nm, and its length was 7 nm owing to the TGI formed on both side walls. The Fin width was 30 nm, which was defined as the W.

Fabrication of IGZO thin film and characterization

The IGZO thin films having the compositions A, B, C, and D shown in Figs. 2(c) and 1(d) were formed using IGZO targets having different In: Ga: Zn ratios. All the films were deposited using a radio-frequency magnetron sputtering apparatus, although the film having the composition B was formed using a deposition apparatus different from that used for the other films. In the phase diagram in Fig. 2(c), the compositions A, B, C, and D are not the compositions of the targets but the compositions of the 100-nm-thick IGZO thin films each formed on a Si substrate, which were examined by inductively coupled plasma mass spectrometry using an Agilent Technologies, Inc. Agilent 8900. The optical band gaps shown in Fig. 2(d) were each

calculated by creating a Tauc plot using the optical absorption coefficient of the IGZO thin film obtained by spectroscopic ellipsometry using a HORIBA, Ltd. UT-300. The carrier concentrations in Fig. 2(e) were each obtained by performing Hall effect measurement by the van der Pauw method on a 35-nm-thick CAAC-IGZO thin film which was formed on a quartz substrate and annealed at 450°C in an oxygen atmosphere for 1 hour. The Hall effect measurement was performed using a TOYO Corporation ResiTest 8400. Note that the results in Fig. 2(e) were obtained in such a manner that the carrier concentration was increased by deliberately forming Vo and VoH by annealing on a deposited CAAC-IGZO thin film at 400°C under vacuum for 1 hour and subsequently, annealing was performed at 200°C, 250°C, 300°C, 350°C, or 400°C in an oxygen atmosphere for 1 hour.

Fabrication of IGZO FET and IGZO FETs/SiFETs monolithic integration

The SiFETs were formed by a 55-nm process. Over the thus obtained Si wafer, a 400-nm-thick planarization film of SiO_2 was formed, followed by contact formation. Then, a wiring layer serving as both a bottom gate electrode and an interconnect to the Si wafer was formed. The BGI was a combination of 20-nm-thick HfO_2 and 20-nm-thick SiO_2. Next, source/drain electrode patterns except for the active layer and the channel region were formed at a time. After formation of 10-nm-thick IGZO and 15-nm-thick IGZO having different compositions, baking was performed at 450°C under atmospheric pressure for 1 hour, and 20-nm-thick TaN was deposited to form source and drain electrodes. Then, the channel region and gate electrode were formed by a damascene process in a self-aligned manner. The GI was a combination of 1-nm-thick Al_2O_3, 3-nm-thick SiO_2, and 3-nm-thick Si_3N_4. The gate electrode over and in direct contact with the channel was a combination of 5-nm-thick TiN and 75-nm-thick W each deposited by metal chemical vapor deposition. Photolithographic patterning was adopted in forming contact with the Si wafer.

Measurement

The transfer characteristics were evaluated using a semiautomatic prober manufactured by HiSOL, Inc. at a stage temperature of 27°C in a dry air under atmospheric pressure. As measurement equipment, a Keysight Technologies B1500A was used. V_{ds} was 0.1 V or 1.2 V and V_{bs} was 0 V. The device characteristics parameters described in Section IV are the medians of nine samples. Furthermore, V_{th} was calculated by a linear extrapolation method.

The ring oscillator was evaluated at a stage temperature of 27°C in an indoor environment (atmospheric pressure, humidity: 50%) using a semiautomatic prober manufactured by HiSOL, Inc. As measurement equipment, a Keysight Technologies B1500A was used, and V_{DD} and V_{SS} were 1.2 V and 0 V, respectively. The waveform was read out with the use of a Model 28 Picoprobe® manufactured by GGB Industries, Inc. and a GDS-3504 GW Instek oscilloscope so that the output load can be minimized.

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