# Performance Modelling and Design Techniques for Efficiency Improvement in On-chip Switched-Capacitor DC-DC Converter

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**Research Article**

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# Performance Modelling and Design Techniques for Efficiency Improvement in On-chip Switched-Capacitor DC-DC Converter

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**Abstract - Fundamental charge vector method analysis is a single parameter optimization technique limited to conduction loss assuming all frequency-dependent switching (parasitic) loss negligible. This paper investigates a generalized structure to design DC-DC SC converters based on conduction and switching loss. A new technique is proposed to find the optimum value of switching frequency and switch size to calculate target load current and output voltage that maximize the efficiency. The analysis is done to identify switching frequency and switch size for two-phase 2:1 series-parallel SC converter for a target load current of 2.67*mA* implemented on a 22*nm* technology node. Results show that a minimum of 250*MHz* switching frequency is required for target efficiency more than 90% and the output voltage greater than 0.85*V* where the switch size of a unit cell corresponds to 10Ω on-resistance. MATLAB and PSpice simulation tools are used for results and validation.**

***Keywords*** **– Switched-Capacitor, performance modelling, DC–DC converter, power efficiency, switching loss**

## 1 Introduction

Switched-Capacitor (SC) converter is a class of DC-DC power converters that efficiently converts one voltage level to another using switches and capacitors. The absence of inductors in power stage makes SC converters suitable for integrated circuit applications resulting in high power density, smaller size and mitigation from inductor associated EMI (Electromagnetic interference) problems [1]. In recent years, such SC DC-DC converters that are appropriate for low-power integrated applications became extremely popular. These converters are utilized in a variety of chip-scale power delivery, MIMO (Multiple-Input Multiple-Output) systems and IoT sensor nodes [2], [3], [4]. Higher power density in SC converters results in higher energy storage capacity due to the integrated capacitors compared to the inductor based converters [5], [6]. Most of the current research in this area is being focused on developing very low-power on-chip applications such as battery-powered signal processors where high power conversion efficiency is essential with reduced parasitic losses.

In addition, integrated capacitors get support of technology scaling. Such capacitors like Metal-Insulator-Metal (MIM) capacitors provide high power density with low series resistance to support high output power without additional fabrication steps [7]. In literature, various combinations of capacitors and switches are investigated during charging phase to deliver bi-directional power flow making use of bidirectional switches. In such power-constrained applications, converter efficiency and converter area are significant parameters [8] [9].

SC converters are capable of supplying voltage to all types of loads, thus meeting the requirements for on-die voltage regulation. The significant performance indices of SC converters are regulation, efficiency, ripple, power density, and response time. In addition, SC-based voltage regulators provide the benefits of tighter noise margins due to absence of complex poles, decrease in voltage stress across semiconductor device and converter power loss scaling with load current [10], [11]. A detailed SC converter operation methodology is explained in [12]. Few novel techniques related to understanding the SC operation are given in [9], [13], and [14]. These techniques mainly focus on conduction loss. In this paper, the impact of various parasitic losses associated with switch capacitor, bottom plate capacitor and *ESR* are considered simultaneously as compared to previous literatures, to implement energy efficient SC converter. In literature, a large number of techniques are developed for the design and analysis of SC converters compared to the case of inductive topologies where comprehensive analysis of designs is limited [6], the design and analysis of the SC topologies is a challenging task.

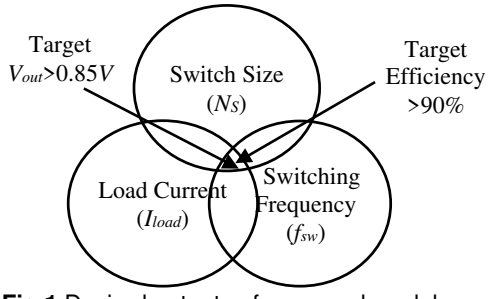



**Fig.1** Desired outputs of proposed model

From the design point of view, the permitted area (fixed flying capacitor), target supply voltage, and the desired load current in SC converter are fixed. However, designers have flexibility in selecting switch size ($N_s$) and switching frequency ($f_{sw}$) parameters. To optimize the efficiency of the converter, there is a tradeoff among conduction loss which is related to Slow Switching Limit & Fast Switching Limit ($R_{SSL}$& $R_{FSL}$) and switching loss ($C_{bott}$, $R_{esr}$ & $C_{sw}$).

In this paper, a novel design technique is proposed to increase the efficiency of fully integrated SC converters by identifying the optimum value of switching frequency and switch size to calculate target load current and output voltage as illustrated in Fig.1. A generalized structure is investigated to design DC-DC SC converters based upon conduction and switching loss. The paper is organized as follows. Section 2 presents a brief analysis for 2:1 series-parallel SC converter based on charge vector method. Section 3 describes a power loss analysis for SC converter. Here, the switching loss associated with the flying capacitor and switch are differentiated which subsequently provides a framework to improve converter efficiency. Section 4 provides various simulation results to show the improvement in power efficiency for a target load current of 2.67$mA$. Section 5 compares MATLAB modelling and PSpice simulation results to validate theoretical justifications. The paper is concluded in section 6.

## 2 Fundamental Analysis: Charge vector method

SC converter is a subset of DC-DC power converters consisting of only switches and capacitors for power conversion. The various types of topologies in SC converters include Ladder, Doubler, Fibonacci, Dickson and Series-Parallel. Fibonacci and Doubler topologies provide high voltage gain compared to other topologies for the same number of switches and capacitors. For power switching and driver symmetry, Ladder and Dickson topologies are used [14]. To achieve maximum capacitor utilization without affecting performance, series-parallel topology is preferred. This paper uses series-parallel topology as an example of the demonstration of analysis and design technique.

For fully integrated applications, capacitor area and efficiency are two significant parameters. The overall steady-state performance of an SC converter is dependent upon its equivalent output impedance [15]. Charging and discharging operation of converter's capacitors allow charge transfer to load producing voltage drop across output impedance. This voltage drop is proportional to the average load current, and all the losses are manifested by voltage drop. Hence, SC converter can be translated into an equivalent DC loss model as depicted in Fig. 2, that captures the steady-state converter operation and power loss (efficiency). This model includes an ideal transformer with a turn ratio equal to the no-load DC conversion ratio. All the conduction losses, including capacitor switching and on-resistance of switch ($R_{on}$) represented by equivalent resistive output impedance ($R_{out}$)[16].

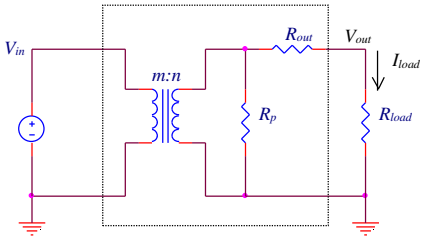



**Fig.2** SC Converter DC Loss Model

The output impedance of converter is a function of switching frequency. It has two asymptotic limits, namely Slow Switching Limit (*SSL*) and Fast Switching Limit (*FSL*), which are responsible for limiting the charging and discharging levels of capacitors.

### 2.1 Slow Switching Limit Analysis

SC converter works in *SSL* regime if the switching frequency is significantly low that the capacitor charge tends to saturate during each phase. In *SSL*, the series resistance associated with switches, capacitors and interconnects are neglected, and the charging/discharging current can be modelled as impulsive. Assuming the switching frequency smaller than the inverse of time constant of capacitive network, the resistive impedances within the converter does not affect output impedance. Thus the converter load appears to be capacitive in nature. For a two-port converter, the concept of charge vector method is presented in [12]. In this method, the charge flow in each capacitor characterized by, the product of output charge and a constant vector (denoted as $a_c$). As this vector multiplies the output charge flow, therefore it is named as capacitor charge multiplier vector.

To understand the analysis of *SSL* through charge vector method, consider an example of a simple single-phase 2:1 series-parallel SC converter shown in Fig. 3. In single-phase converter, there is only one flying capacitor present in the circuit which gets charged during on-phase (phase-1) and discharged during off-phase (phase-2) of the switching clock. We derive a pair of charge multiplier vectors $a^1$ and $a^2$ for charging and discharging phase. These vectors correspond to the instantaneous charge flows when the switches are in closed state.

In steady-state operation, the output charge flow is the amount of charge flowing into the output voltage source in one period. Therefore, the capacitors (and switches) charge flow is proportional to the converter output current ($I_{out}$) given as

$$q_c^j = a_c^j q_{out} = a_c^j \frac{I_{out}}{f_{sw}} \quad (1)$$

where $q_c^j$ represents the capacitor charge in $j^{th}$ phase, $q_{out}$ is the total output charge flow, $f_{sw}$ is the switching frequency, and $a_c^j$ is capacitor charge multiplier in $j^{th}$ phase. Charge multipliers are defined as the ratio of charge flow through each element (output, capacitor and input) to the total output charge flow ($q_{out}$) in one time period, i.e.

$$a^1 = \begin{bmatrix} q_{out}^1 \\ q_c^1 \\ q_{in}^1 \end{bmatrix} / (q_{out}) = \begin{bmatrix} a_{out}^1 \\ a_c^1 \\ a_{in}^1 \end{bmatrix} \tag{2}$$

$$a^2 = \begin{bmatrix} q_{out}^2 \\ q_c^2 \\ q_{in}^2 \end{bmatrix} / (q_{out}) = \begin{bmatrix} a_{out}^2 \\ a_c^2 \\ a_{in}^2 \end{bmatrix} \tag{3}$$

where $a_{out}$ , $a_{in}$ are the charge multipliers for total output, input charge flow respectively, and $q_{in}$ is total input charge flow defined as:

$$q_{in} = a_{in} q_{out} = (a_{in}^1 + a_{in}^2) q_{out} \tag{4}$$

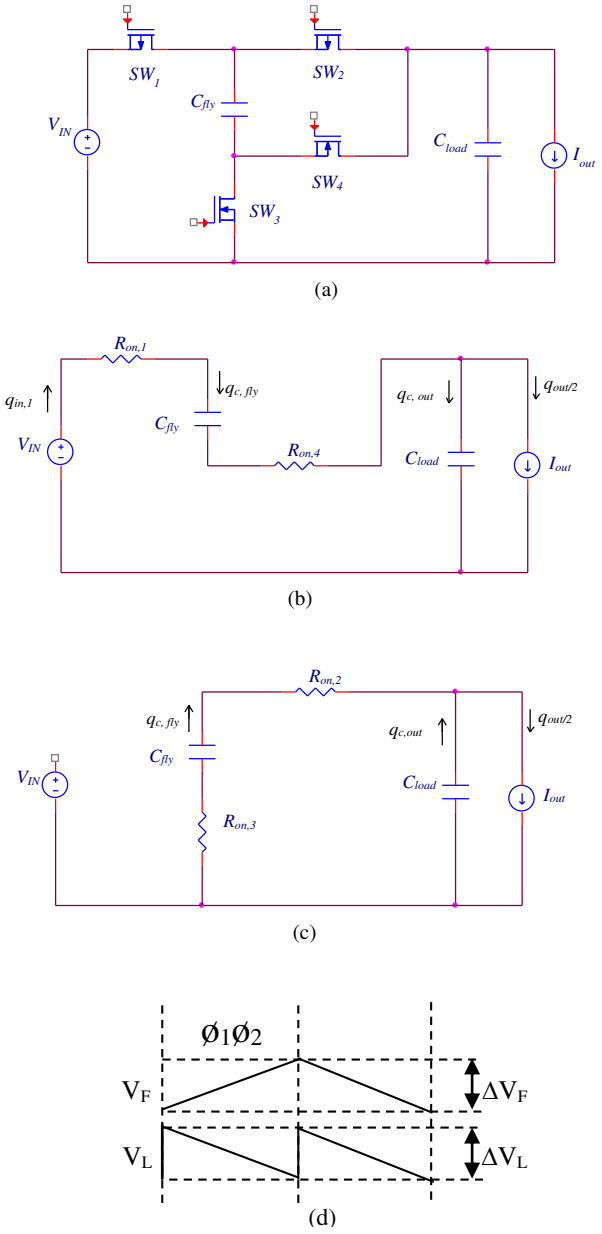



**Fig. 3** (a) Single-phase 2:1 series-parallel SC converter (b) Phase-1 operation (charging) (c) Phase-2 operation (discharging) (d) Flying and load capacitors voltage waveforms

Further, as per the definition of conservation of charge,

$$a_{out}^1 + a_{out}^2 = 1 \tag{5}$$

With the knowledge of $a^1$, $a^2$ capacitor characteristics and the switching frequency, the *SSL* output impedance can be calculated. The calculation of output impedance uses Tellegen's theorem [12] to prove the orthogonality between vectors representing branch voltages branch currents satisfying Kirchoff's voltage and current laws. Both input and output are modelled as independent voltage sources. To evaluate *SSL* output impedance, the input supply voltage is shorted and the charge flow into the non-zero load is measured. Hence, the steady-state *SSL* output impedance is given by,

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{6}$$

In (6), $C_i$ represents the capacitance corresponds to $i^{th}$ capacitor and $a_{c,i}$ is the ratio of charge flow per period in $C_i$ to the total output charge flow in one period in steady state known as charge multiplier coefficient. To calculate the charge multiplier vectors for charging and discharging phase shown in Fig.3, *KCL* equations are used for both the states of switching cycle. Assuming converter operating at 50% duty cycle, the load draws the same current equal to $q_{out}/2$ in both the phases. The charge multiplier vectors for two states are given as

$$a^1 = [1/2 \;\; 0 \;\; 1/2 \;\; 1/2] \tag{7}$$

$$a^2 = [1/2 \;\; 0 \;\; -1/2 \;\; 0] \tag{8}$$

Using the charge flow diagram of a 2:1 series-parallel converter shown in Fig.3, total charge flow to the output is $q$, and the charge flow in both capacitors$C_1$ and $C_2$ is $q/2$. Thus $a_{c,1} = a_{c,2} = ½$. Using (6), the *SSL* impedance for single-phase 2:1 converter $(a_{c,i})^2 = ½$ is given by

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \frac{1}{2\, C_i f_{sw}} \tag{9}$$

Therefore, at low switching frequencies, the power loss is dominated by the conduction loss due to $R_{SSL}$, given in (9).

## 2.2 Fast Switching Limit Analysis

*FSL* occurs due to on-state impedances of switches and conductive interconnects which dominates at high switching frequency. At high frequencies, the capacitor never reaches an equilibrium state. While some switches and interconnects conducts during on-state, others conduct during the off-state of switching clock [13]. The duty cycle is an important parameter for *FSL* impedance, as the converter current flows for entire duration of charging and discharging operation. The duty cycle during phase-1 and phase-2 is $D_1$=*D*, and $D_2$=1-*D* respectively. For a particular switch *i*, the duty cycle $D_i = D_1$, if the switch is on during phase-1 and $D_i$=$D_2$, if the switch is on during phase-2. Although the optimal duty cycle of SC converter is close to 0.5 but due to inherent asymmetries in topologies, it deviates slightly from this value. In the *FSL* limit, capacitors are modelled as constant voltage sources, and current flowing through capacitors is assumed constant. The circuit loss is dependent only on conduction loss in resistive elements [14].

The conduction loss due to on-resistance of switch is calculated using the amount of charge flow in each switch ($q_r$), which is related to the output current flow ($I_{out}$) as

$$q_r^j = \; a_r^j q_{out} = a_r^j \frac{I_{out}}{f_{sw}} \tag{10}$$

The modelling of all other parasitic resistive losses like capacitor Equivalent Series Resistance (*ESR*) is done in the subsequent sections.

The charge multiplier vector for a switch can be calculated by examining the capacitor charge flow in both the phases. Switches which are in on-state carry the same amount of charge as flying capacitor and there is no charge flow through switches in off-state. In series-parallel 2:1 SC converter, out of the four switches, two are in on-state during phase-1and the other two conducts in the phase-2 of the clock. This combination of switches set up a path for charge flow through various capacitors as shown in Fig. 3. Hence, the charge multiplier vector for switches in phase-1 is given by

$$a_r^1 = [1/2 \;\; 0 \;\; 0 \;\; 1/2] \tag{11}$$

Similarly, the charge multiplier vector in phase-2 is given by

$$a_r^2 = [0 \;\; 1/2 \;\; 1/2 \;\; 0] \tag{12}$$

These vectors can be added by considering only non-zero elements of vectors corresponding to switches which are conducting.

Therefore, the resultant metric for switches becomes

$$a_r = [1/2 \;\; 1/2 \;\; 1/2 \;\; 1/2] \tag{13}$$

Using similar steps *FSL* output impedance can be expressed in terms of switch charge multiplier vector of every switch and the converter parameters $R_{on,i}$ and $D_i$ are given as

$$R_{FSL} = \sum_i \frac{R_{on,i}(a_{r,i})^2}{D_i} \tag{14}$$

where $R_{on,i}$ is the on-resistance of $i^{th}$ switch. For simplification, a 50% duty cycle may be assumed. Further, the *FSL* output impedance can be expressed as

$$R_{FSL} = 2\sum_i R_{on,i}\left(a_{r,i}\right)^2 \tag{15}$$

From (13), it is clear that $(a_r)^2$ =1. Substituting this value in (15), the *FSL* impedance becomes

$$R_{FSL} = 2R_{on,i} \tag{16}$$

From (16), it is clear that the *FSL* output impedance is dependent on switch characteristics and is independent of switching frequency.

### 2.3 Total output Impedance

The total output impedance of an SC converter is a combination of *SSL* impedance and *FSL* impedance. Although these impedances cannot be directly added as they are calculated under different operating conditions. Fig. 4 shows a bode plot for an example SC output impedance. The optimal efficiency is attained at the knee point between *FSL* and *SSL*, and hence this knee-point should be the chosen as the ideal operating point. The exact formulation of output impedance is difficult and hence quadratic sum approximation is common for many converters [16] where

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{17}$$

Intuitively, these *SSL* and *FSL* limits are determined by the ratio of the output voltage to output current and taking the limit when the switching frequency approaches zero for *SSL* and infinity for *FSL*

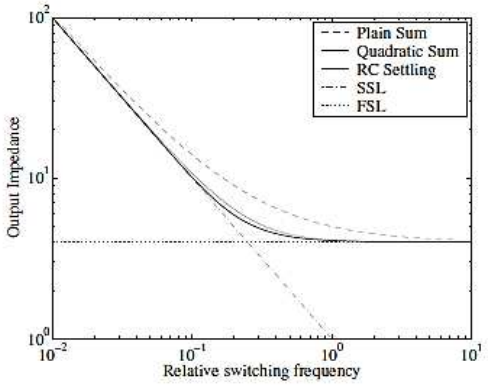



**Fig. 4** Output impedance when $R_{SSL} \approx R_{FSL}$ and approximations

## 3 SC Converter Power Loss Model

Every topology is characterized by voltage transformation ratio *n/m,* as illustrated in Fig.2. Reconfiguring (*n,m*), the converter can achieve coarse regulation. The desired regulation can be achieved by varying output resistance. The maximum achievable power stage efficiency is given as $V_{out,actual}/V_{out}$. Consequently, the dominant loss mechanism becomes the desired regulation mechanism. To investigate the impact of various factors that contribute to efficiency, this paper uses step-down DC-DC converter topology which is the most common in recent times for fully integrated systems. As discussed earlier, the key power-loss contributors in an SC converter are conduction and switching losses. As shown in Fig.2, power losses due to parasitic capacitances of flying capacitors and switches contribute to a shunt resistance loss denoted as $R_p$. Further, the series conduction losses due to on-resistance of switches and switching losses due to flying capacitor charging and discharging is represented by $R_{out}$. Shunt resistance ($R_p$) is independent of load current but depends upon converter switching frequency of operation [16].

### 3.1 Switch selection criterion

The realization of switches is based on their position in generalized switch network using *NMOS* or *PMOS* transistor. At high switching frequency, this switch selection method plays an important role in performance improvement through reduction in gate drive losses [17].

### 3.2 Proposed Two-phase SC converter operation

SC converters saves and transfer charge to the load by connecting flying capacitors in series or parallel, which act as voltage sources. Hence, the voltage conversion is achieved by the summation or subtraction of flying capacitor voltages of an SC stage and is determined by its topology. In a conventional n:1 series-parallel topology, n represents the nominal, unregulated step-down voltage ratio ($n = V_{in}/V_{out}$). The series-parallel topology consists of 3n-2 switches, and n-1 flying capacitors. In an SC converter, the total number of conversion ratio is determined by charge transfer phases per operation cycle and the number of flying capacitors. For fixed number of flying capacitors, more voltage conversion ratios can be realized by increasing the number of charge transfer phases [18]. Though, this restricts the net conduction time of each switch, resulting in greater switching loss and reduced efficiency. This work focuses on the efficient operation of an SC converter, therefore, a 2-phase non-overlapping clock is used owing to the simple drivers and control schemes.

Fig. 5 shows a two-phase 2:1 step-down SC DC-DC converter example considered to illustrate loss analysis and calculation of design parameters. There are two flying capacitors $C_1$ and $C_2$ in the network as shown in Fig. 5. There are total eight switches to control the charging and discharging of flying capacitors in accordance to the switching clock [18]. Out of eight switches, four are conducting in phase-1 while the remaining four will conduct in phase-2. In phase-1 of the switching clock, the top and bottom terminals of $C_1$ are connected to the input ($V_{in}$) and output ($V_{out}$) respectively, and gets charged from input source. While $C_2$ terminals are connected between output and ground, gets discharged through the load. The roles of two capacitors ($C_1$, $C_2$) are complemented in phase-2 such as $C_2$ is charged and $C_1$ is discharged as illustrated in Fig. 5(*b*). The capacitor $C_{load}$ is used as a load capacitor.

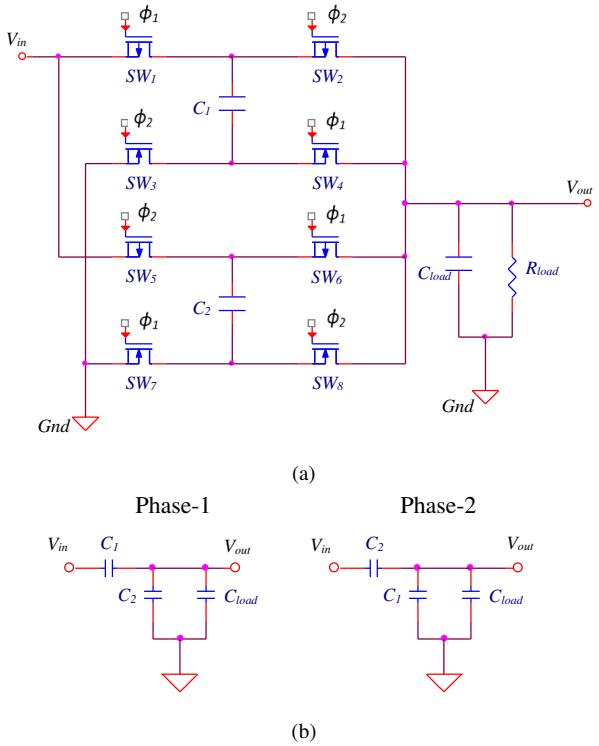



**Fig. 5** Two-phase 2:1 series-parallel converter: (a) Schematic (b) Circuit configuration in two different phases

### 3.3 Loss Analyses

As discussed earlier, SC DC-DC converter primarily consists of two categories of power loss, namely, conduction loss and switching loss. Switch conduction loss is due to the on-resistance of switches. Reduction in switch conduction loss is proportional to the switch size reduction but this leads to increase in shunt loss via parasitic capacitance of switch. On the other hand, the switching loss due to charging and discharging of flying capacitor produces ripple voltage ($\Delta V_F$) as shown in Fig.3(*d*). To simplify steady-state equations of SC converter, two approximations are used for flying capacitors, namely, (a) charge conservation principle, (b) small ripple approximation [18]. Small ripple approximation states that the capacitor voltages contain DC component and switching ripple at the switching frequency and its associated harmonics.

### 3.3.1 Analytical Conduction Loss Model

For the 2-phase series-parallel converter, the *SSL* impedance of two networks makes parallel connection and hence the resultant impedance is half the initial value of $R_{SSL}$ and can be calculated by selecting appropriate values of capacitor ($C_i$) and switching frequency ($f_{sw}$) given as

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \frac{1}{4\,C_i f_{sw}} \tag{18}$$

Similarly, the *FSL* impedance can be evaluated by choosing appropriate values for switch resistance ($R_{on,i}$), *i.e.*

$$R_{FSL} = R_{on,i} \tag{19}$$

The equivalent output resistance is the quadratic addition of $R_{SSL}$ and $R_{FSL}$, as direct addition results in total output impedance value higher than the estimated value. Hence, the total output impedance is given by

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{20}$$

The conduction power loss ($P_{RES}$) may be expressed in terms of the losses related to *SSL* and *FSL* impedances. The power loss due to *SSL* impedance is given by

$$P_{loss,SSL} = I_{out}^2 R_{SSL} \tag{21}$$

where, $I_{out}$ is the output current.
Power loss due to *FSL* impedance is given by

$$P_{loss,FSL} = I_{out}^2 R_{FSL} \tag{22}$$

Therefore, the total conduction power loss is expressed as

$$P_{RES} = \sqrt{\left(P_{loss,SSL}^2\right) + \left(P_{loss.FSL}^2\right)} \tag{23}$$

### 3.3.2 Analytical Switching Loss Model

In addition to conduction losses, an SC converter exhibits shunt losses that are independent of load current, including switch gate parasitic and bottom plate capacitor switching loss. In SC converter when a Metal Oxide Semiconductor (MOS) transistor switch is in off-state, the parasitic capacitance associated with the transistor switches get charged. On the other hand, when the switch comes to on-state, this parasitic capacitance discharged to zero abruptly. The switching clock drives MOS transistor to on and off states. Therefore, the power loss due to switch parasitic is given by

$$P_{loss,swcap} = f_{sw} C_{sw} V_{sw,cap}^2 \tag{24}$$

In (24), $f_{sw}$, $C_{sw}$, $V_{sw}$ represents switching frequency, switch parasitic capacitance and switch blocking voltage in non-conducting state respectively. There are total eight switches in a two-phase 2:1 series-parallel converter producing total loss equal to eight times that of single switch capacitor loss.

Similarly, the power loss due to bottom plate capacitance can be expressed as

$$P_{loss,bottcap} = f_{sw} C_{bott} V_{cap}^2 \tag{25}$$

In (25), $C_{sw}$ is the bottom plate capacitance of the flying capacitor, and $V_{cap}$ is the bottom plate capacitor voltage. The power loss due to the *ESR* of the flying capacitor is given as

$$P_{loss,esr} = I_{out}^2 R_{esr} \tag{26}$$

Total switching power loss becomes

$$P_{sw} = P_{loss,swcap} + P_{loss,bottcap} + P_{loss,esr} \tag{27}$$

### 3.3.3 Total Power Loss

The total power loss can be expressed as

$$P_{total,loss} = P_{RES} + P_{loss,swcap} + P_{loss,bottcap} + P_{loss,esr} \tag{28}$$

The output power is given by

$$P_{out} = \frac{V_{out}^2}{R_{load}} \tag{29}$$

where $V_{out}$ is the ideal output voltage and $R_{load}$ is the load resistance. Applying voltage division to the network model in Fig.2, the actual output voltage across load is given by

$$V_{out,actual} = V_{out} \frac{R_{load}}{(R_{load}+R_{out})} \tag{30}$$

where $R_{out}$ is the total output impedance considering both *SSL* and *FSL* asymptotic limits.

## 4 Efficiency Enhancement

The process of efficiency enhancement requires knowledge of working voltages for various components. This was not essential for output impedance analysis. In SC converter, the size of each capacitor and switch was optimized separately. In this section, the overall efficiency enhancement for SC converter is achieved for two design parameters namely, target load current $I_{out}$ and input voltage $V_{in}$ [15].

Three design parameters that are significant in integrated circuit implementations are

1. Switch size ($N_s$).
2. Load current ($I_{load}$)
3. Switching frequency($f_{sw}$)

The parameter $N_s$ represents the number of switches responsible for reduced on-resistance. Similarly, $I_{load}$ is the target load current for a given converter load voltage measured in *mA*. Finally, $f_{sw}$ is the switching frequency measured in *MHz*. The efficiency enhancement technique discussed here is applicable to discrete implementations also. The equivalent output impedance at the desired switching frequency and switch size at the preferred load current are the considered useful performance metrics. The optimization procedure minimizes the total power loss and limits the total capacitor area for specified design [19].

The efficiency η of the 2:1 series-parallel converter is given by

$$\eta = \frac{P_{out}}{P_{out}+P_{RES}+P_{loss,swcap}+P_{loss,bottcap}+P_{loss,esr}} \tag{31}$$

where,
$P_{out}$ is output power
$P_{RES}$ is combined resistive conduction loss (*SSL* and *FSL*).
$P_{loss,swcap}$ is switch capacitance parasitic loss
$P_{loss,bottcap}$ is bottom plate capacitance loss
$P_{loss,esr}$ is *ESR* loss

For two-phase 2:1 SC circuit analysis, ideal switches with constant on-resistance are assumed. We investigate losses due to bottom plate capacitance, *ESR* of flying capacitors, and switch parasitic capacitor as shown in Fig. 6. These losses degrade the efficiency performance significantly at high frequencies.

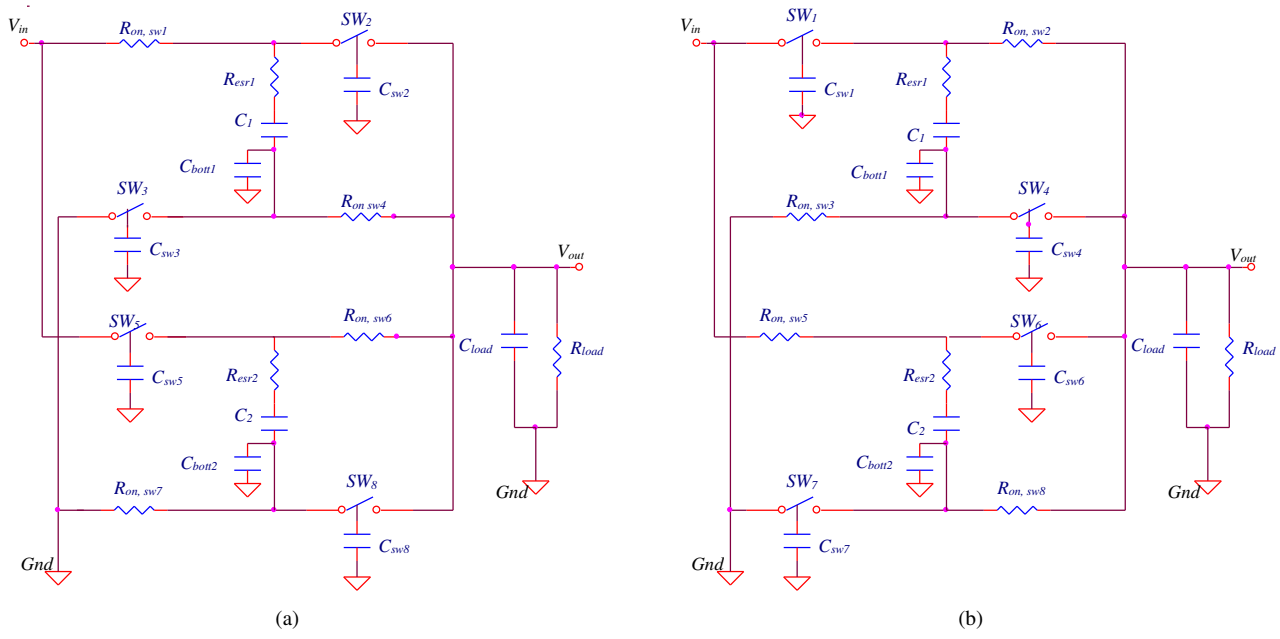



**Fig. 6** Two-phase 2:1 series-parallel converter circuit showing parasitic (*ESR*, bottom plate capacitor, switch gate capacitor): (a) Phase-1 operation (b) Phase-2 operation

Figs.7-8 shows the plot of efficiency with variation in $N_S$ and $N_C$. Initially, with the increase in $N_S$ and $N_C$, there is a sharp increase in the efficiency but as the parasitic loss start dominating, the efficiency either stop improving (in case of variation with $N_S$ when $N_C$ and $f_{sw}$ are constant) or even reduces (in case of variation with $N_C$ when $N_S$ and $f_{sw}$ are constant). Commonly, these parasitic capacitors cause significant increase in switching energy loss, by limiting both turn-on and turn-off transient behaviour of switches.

The power loss due to bottom plate capacitance is given by

$$P_{loss,bottcap} = N_c C_{bott} f_{sw} V_{cap}^2 \tag{32}$$

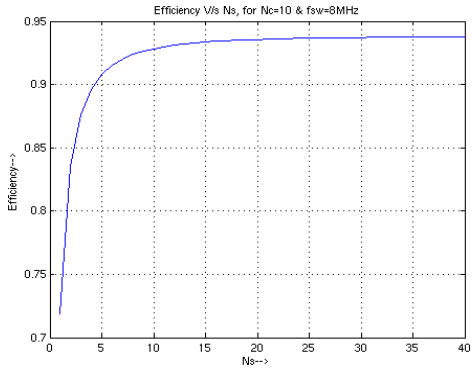



**Fig. 7** Efficiency v/s number of switches ($N_S$)

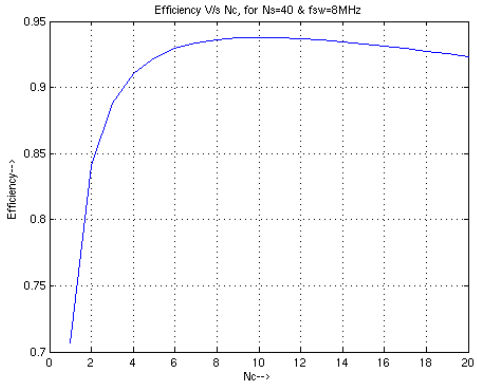



**Fig. 8** Efficiency v/s number of capacitors($N_C$)

The optimum value of switch size and switching frequency is chosen that maximizes efficiency for given load current and target output voltage. The mathematical formulation is realized for conduction, switching power loss and efficiency. Discrete values of $N_s$, $R_{load}$ and $f_{sw}$ (as shown in Table 1) are chosen by observing various contour plots showing variation in efficiency with $N_s$ and $I_{load}$ for *ESR* value of 10 Ω and switching frequency ranging from 150$MHz$ to 375$MHz$.

Efficiency maximization does not require minimization of the total output impedance through proper selection of device technology for specific application. It is desirable to minimize the effect of various parasitic associated with SC converter [15], [16]. The comparison of efficiency and output voltage is given in Table 1 for variation in $N_S$, $R_L$ and $f_{SW}$. These parameters are varied as follows

i. Number of switches ($N_s$): [6, 7, 8]
ii. Load Resistance ($R_{load}$) in Ω: [320, 540, 720]
iii. Switching Frequency ($f_{sw}$) in $MHz$: [200, 300, 400]

Transistor level circuit configuration used for simulation is given in Fig.5, and all the parasitic losses operating in two phases (charging and discharging) are incorporated as shown in Fig.6. The current value of $I_{load,max}$ equal to 2.67$mA$ per cell is used based on power density considerations. The value of $R_{load}$ is taken as 318.35 Ω which equivalent to $I_{load}$ amount of 2.67 $mA$ for target voltage $V_{out}$ of 0.85$V$. The $R_{on}$ value of 80 Ω corresponds to *PMOS/NMOS* switch size of 0.48$\mu$/0.03$\mu$ @110$C$, and $V_{GS}$ equals to 0.9$V$ are considered [20-21]. The performance is investigated for different values of primary switches using PSpice.

Switch parasitic capacitance ($C_{sw}$) represents the total gate capacitance ($C_{gs}$+$C_{gd}$) for each switch and is taken as 15fF. Bottom plate capacitance is defined as the ratio of flying capacitance to some constant value, i.e., $C_{bott}$=$C_{fly}$/constant. Assuming the value of constant equal to 125, the value of $C_{bott}$ becomes 0.32$pF$. With the increase in number of cells, the target $I_{load}$ which is the product of $I_{load}$ per cell and number of cells, also increases [11].

**Table 1**
Efficiency and output voltage with variation in $N_S$, $R_L$ & $f_{SW.}$

| Combination Number | $N_s$ | $R_L$ (Ω) | Frequency (*Hz*) | Efficiency | $V_{out,actual}$ (*V*) |
|---|---|---|---|---|---|
| 1 | 6 | 320 | 2.00E+08 | 0.9119 | 0.8456 |
| 2 | 6 | 320 | 3.00E+08 | 0.9085 | 0.8547 |
| 3 | 6 | 320 | 4.00E+08 | 0.8995 | 0.8584 |
| 4 | 6 | 540 | 2.00E+08 | 0.9167 | 0.8670 |
| 5 | 6 | 540 | 3.00E+08 | 0.9009 | 0.8726 |
| 6 | 6 | 540 | 4.00E+08 | 0.8825 | 0.8749 |
| 7 | 6 | 720 | 2.00E+08 | 0.9106 | 0.8750 |
| 8 | 6 | 720 | 3.00E+08 | 0.8871 | 0.8793 |
| 9 | 6 | 720 | 4.00E+08 | 0.8624 | 0.8810 |
| 10 | 7 | 320 | 2.00E+08 | 0.9140 | 0.8486 |
| 11 | 7 | 320 | 3.00E+08 | 0.9108 | 0.8584 |
| 12 | 7 | 320 | 4.00E+08 | 0.9018 | 0.8626 |
| 13 | 7 | 540 | 2.00E+08 | 0.9168 | 0.8688 |
| 14 | 7 | 540 | 3.00E+08 | 0.9008 | 0.8749 |
| 15 | 7 | 540 | 4.00E+08 | 0.8819 | 0.8774 |
| 16 | 7 | 720 | 2.00E+08 | 0.9098 | 0.8764 |
| 17 | 7 | 720 | 3.00E+08 | 0.8856 | 0.8810 |
| 18 | 7 | 720 | 4.00E+08 | 0.8603 | 0.8830 |
| 19 | 8 | 320 | 2.00E+08 | 0.9151 | 0.8506 |
| 20 | 8 | 320 | 3.00E+08 | 0.9120 | 0.8611 |
| 21 | 8 | 320 | 4.00E+08 | 0.9029 | 0.8656 |
| 22 | 8 | 540 | 2.00E+08 | 0.9164 | 0.8701 |
| 23 | 8 | 540 | 3.00E+08 | 0.8999 | 0.8765 |
| 24 | 8 | 540 | 4.00E+08 | 0.8805 | 0.8793 |
| 25 | 8 | 720 | 2.00E+08 | 0.9085 | 0.8774 |
| 26 | 8 | 720 | 3.00E+08 | 0.8836 | 0.8823 |
| 27 | 8 | 720 | 4.00E+08 | 0.8576 | 0.8844 |

Similarly, the target switch size is equal to the product of switch size per cell and the number of cells. In this paper, the analysis is done for a single cell (two-phase converter) configuration. For various control scenarios, the conversion efficiency at light load is estimated using the MATLAB simulation and is plotted in Figs. 9-12.

### 4.1 Optimum switch size

The switching devices (*MOS* transistors) operate in linear region. The on-resistance ($R_{on}$) of switch can be expressed as ($K_R/W$) where the value of $K_R$[Ω-μm] depends upon whether the switch type is *PMOS* or *NMOS* and $W$ is the width of switching device. The smaller switch size is desirable to minimize the charge injection and clock feedthrough caused by overlap capacitance associated with switches. Similarly, the capacitance can be modelled as $k_CW$ where $k_C$ is a constant coefficient in $fF/\mu m$. In the design using *MIM* capacitors, a substantial gain in light load efficiency can be achieved by scaling the width of the *MOSFETs* [17], [21-22]. Fig.9 shows efficiency variation with increase in switch size. It is observed that switch size of 6, 7 and 8 produces output voltage $V_{out,actual}$ and efficiency higher than 0.85*V* and 90% respectively.

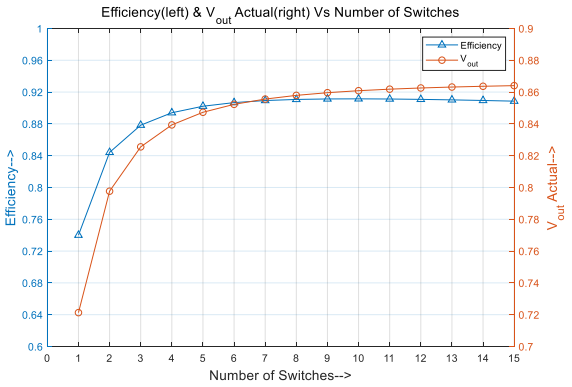



**Fig. 9** Efficiency variation with $N_s$ and $V_{out,\ actual}$ for frequency =250 *MHz* and $R_{load}$ =327Ω

Further, the switch counts ($N_s$) greater than eight does not improve performance significantly as switch gate parasitic losses start dominating. The various circuit and control parameters used for simulation are summarized in Table 2.

**Table 2**
Simulation parameters

| Input Parameter | Value |
|---|---|
| $R_{load}$ | 327 Ω (2.6$mA$) |
| $f_{sw}$ | 250 $MHz$ |
| Switch size | .48$\mu$/.03$\mu$, *PMOS/NMOS* |
| $R_{on}$/switch | 80 Ω |
| $N_s$ (Switch multiple Sweep) | 1 to 15 |

When the switches are connected in parallel, the equivalent switch resistance is given by (33). With the increase in $N_s$, switch conductance increases and is given by

$$R_{FSL} = \frac{R_{on}}{N_s} + \frac{R_{esr}}{N_c} \tag{33}$$

In (33), $R_{sw}/N_s$ is the equivalent switch resistance of $N_s$ switches connected in parallel. Also, the *ESR* value is divided by number of *MIM* capacitors connected in parallel.

The power loss due to parasitic switch capacitance and bottom plate capacitance are given by

$$P_{loss,swcap} = N_s\, f_{sw} C_{sw} V_{sw,cap}^2 \tag{34}$$

From (34), it is clear that power loss is directly proportional to $N_s$ as switch capacitance increases with an increase in switch size [17]. This put an upper bound on switch size to limit the parasitic power loss. Also $f_{sw}$, $C_{sw}$,$N_s$and $V_{sw,cap}$ represents the switching frequency, parasitic switch capacitance, switch count, and switch blocking voltage respectively.

## 4.2 Optimum switching frequency

The efficiency variation with switching frequency is plotted in Fig.10. The various simulation parameters are summarized in Table 3. With the increase in switching frequency, parasitic losses increase as given by (32) and (34). In addition, it decreases conduction loss due to the flying capacitor charging and discharging cycle as it is inversely proportional to the switching frequency [18]. Hence, the selection of switching frequency depends upon desired application. It is observed that switching frequency ($f_{sw}$) beyond 300 $MHz$ yields output voltage ($V_{out}$) greater than 0.85$V$ for a given switch size and load resistance ($R_{load}$) pair. On the other hand, switching frequency between 200 $MHz$ to 300 $MHz$ achieve efficiency more than 90%.

**Table 3**
Simulation parameters

| Input Parameter | Value |
|---|---|
| $R_{load}$ | 320 Ω |
| Unit switch size | .48$\mu$ /.03$\mu$, *PMOS/NMOS* |
| $R_{on}$/switch | 80 Ω |
| $N_s$ (Switch multiple) | 6 |
| $f_{sw}$ (Sweep) | 50 $MHz$ to 1 $GHz$ |

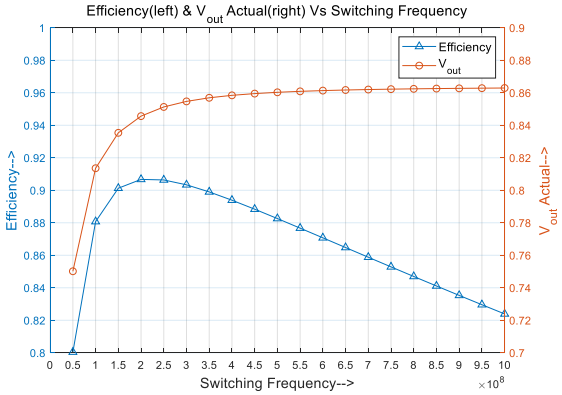



**Fig. 10** Efficiency variation with $f_{sw}$ & $V_{out,\,actual}$ for fixed $R_{load}$=320Ω and $R_{on}$= 80/6 (6 switches)

## 4.3 Efficiency versus $R_{load}/I_{load}$ Tradeoff

The various simulation parameters used are given in Table 4. It is clear from Figs. 11 and 12 that load resistance ($R_{load}$) variations between 320 Ω to 720 Ω corresponds to load current ($I_{load}$) ranging from 1.2$mA$ to 2.6$mA$. This produces the output voltage ($V_{out,actual}$) beyond 0.85$V$. Further, the load resistance between 320 Ω to 540 Ω increases efficiency beyond 90%.

**Table 4**
Simulation parameters

| Input Parameter | Value |
|---|---|
| $f_{sw}$ | 250 $MHz$ |
| Unit switch size | .48$\mu$ /.03$\mu$, *PMOS/NMOS* |
| $R_{on}$/switch | 80 Ω |
| $N_s$ (Switch multiple) | 6 |
| $R_{load}$ (Sweep) | 80 Ω to 1800 Ω |

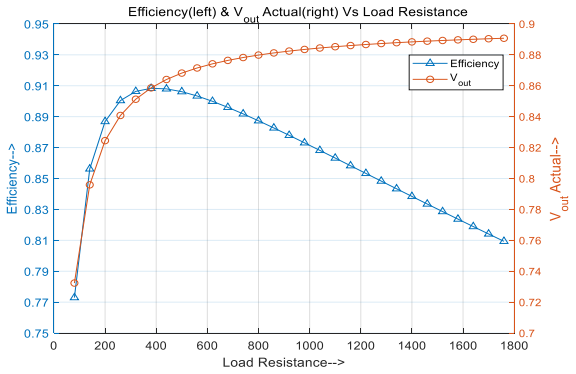



**Fig.11** Efficiency variation with $R_{load}$ & $V_{out}$ at for fixed $R_{on}$=80/6 Ω (6 switches) and frequency= 250 *MHz*

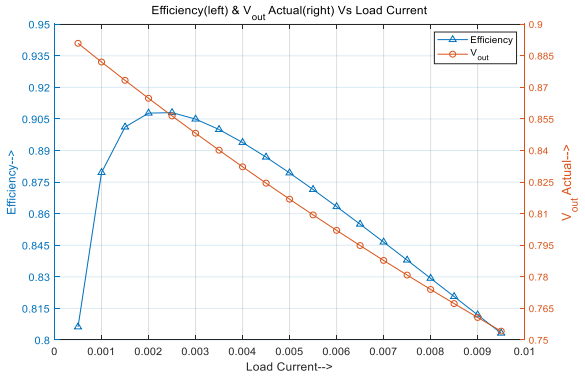



**Fig. 12** Equivalent $I_{load}$ characteristics

## 5 Simulation Results and Observations

In this section, a step-down 2:1 series-parallel SC converter is simulated over a range of switching frequencies. The input voltage is assumed to be 1.8$V$. Fig. 13 shows the contour plot for optimum efficiency in 2:1 SC converter operating at switching frequency value of 250 $MHz$. The maximum efficiency of 91.486 % is achieved at the output voltage of 0.8583$V$ for 2.678$mA$ load current corresponding to $N_s$ value equal to 8. This results in the on-resistance value $R_{on}$ = 80/8 for the 10Ω switch. It is observed that a minimum of 250$MHz$ switching frequency is required for target efficiency more than 90% and target output voltage greater than 0.85$V$.

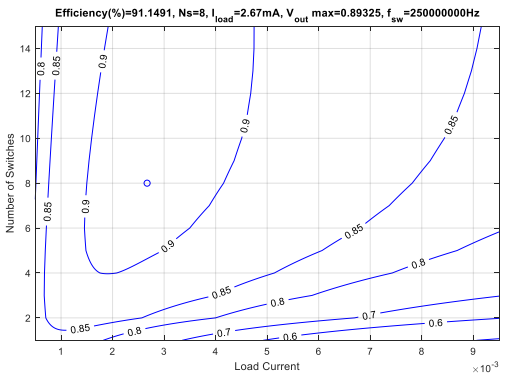



**Fig. 13** Efficiency variation with $N_s$ & $I_{load}$ for $f_{sw}$=250$MHz$

Fig.14 shows the maximum achievable efficiency and optimal switching frequency with the variation in capacitance value for fixed $N_C$ and $N_S$ values of 10 and 40 respectively. The increase in capacitance takes more time to charge as $R_{SSL}$ is inversely proportional to the capacitance. This leads to reduction in switching frequency. Due to reduced switching frequency, there is reduction in parasitic losses and consequently, this leads to higher efficiency.

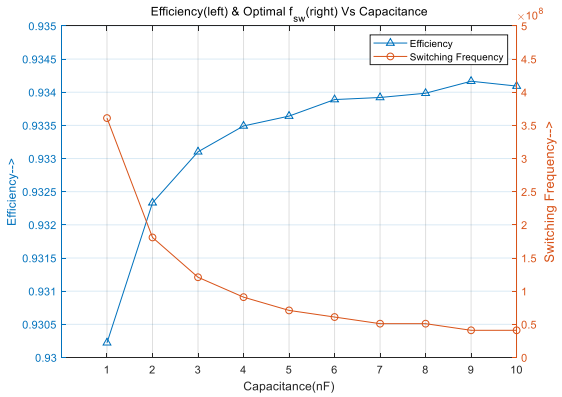
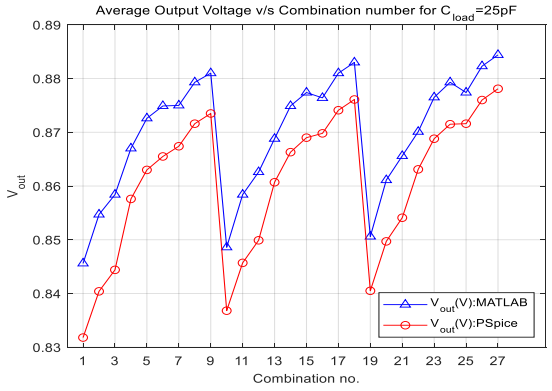
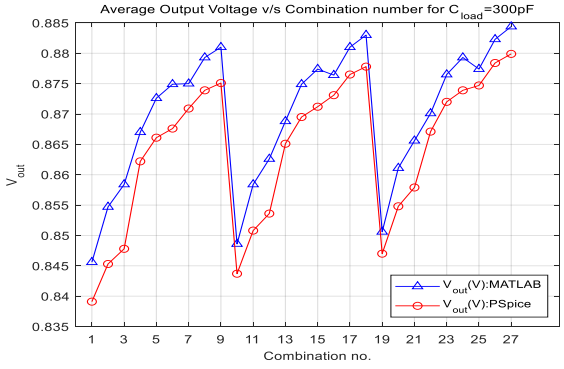



**Fig. 14** Variation of efficiency and switching frequency with capacitance

MATLAB and PSpice simulation results are compared for 27 different combinations of $N_s$, $R_{load}/I_{load}$ $(mA)$ and $f_{sw}$ $(Hz)$ as shown in Figs. 15-16. The value of $V_{out}$ is almost same for both cases and there is minor improvement in $V_{out}$ as $C_{load}$ increases from $25pF$ to $300pF$. Efficiency does not change significantly with variations in switching frequency. At higher switching frequency, there is only 4% deviation in MATLAB and PSpice simulations. Since high switching frequency can increase the switching loss in the converter, causing degradation of efficiency. Therefore, it is clear that the methods developed in this paper accurately predict the performance of any two-phase SC converter. Table 5 shows a comparison of proposed work with existing literature.

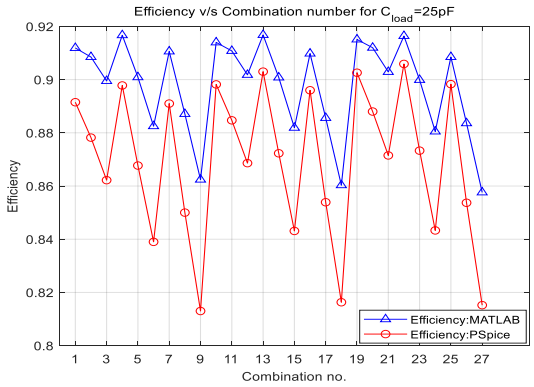



(a)

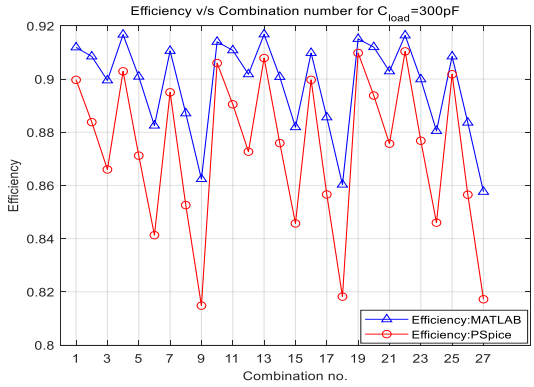



(b)

**Fig. 15** Plot showing *avg_Vout(V)* comparison between PSpice and MATLAB results for: (a) *Cload= 25pF* (b) *Cload= 300pF*




(a)




(b)

**Fig. 16** Plot Showing Efficiency comparison, between PSpice and MATLAB results for: (a) $C_{load}$ = *25pF* (b) $C_{load}$ = *300pF*

**Table 5**
Comparison of proposed and existing work

| Design | [17] | [15] | [22] | [23] | [24] | Proposed work |
|---|---|---|---|---|---|---|
| Result Type | Measured | Measured | Measured | Simulated | Measured | Simulated |
| Technology | 65*nm* | 32*nm SOI* | 250*nm* | 45*nm* | 180*nm* | 22*nm SoC* |
| Capacitor Type | Gate oxide | Gate oxide | *MIM* | *MIM* | Off-chip | *MIM* |
| Gain Ratio | 1/2, 1/3, 2/3 | 1/3, 1/2, 2/3 | 1/2, 3/5, 3/4 | 1/2 | 1/2, 1/3, 2/3 | 1/2 |
| Output Current | 0.02-5*mA* | - | 0.1*mA* | 0.1-4*mA* | 1-10*mA* | 2.67*mA* |
| Peak Efficiency | 85% | 79.8% | 76% | 85% | 70.8% | 91% |
| Switching Frequency | 12*MHz* | - | 5*MHz* | 20*MHz* | 100*KHz* | 250*MHz* |

## 6 Conclusion & Future Scope

In this paper, a steady-state performance modelling analysis method is developed to predict the output resistance and efficiency of an SC converter. This method relies on charge multipliers, the ratio of the charge flowing through each component to the output charge flow from an SC converter. The impact of various parasitic losses associated with switch capacitor, bottom plate capacitor and *ESR* are considered simultaneously unlike existing literature to investigate the performance of on-chip SC converter. The design technique modulates both transistor size and switching frequency for a given target load current to minimize the overall SC converter losses. Although the approach is investigated for two-phase 2:1 series-parallel SC converter, the efficiency improvement algorithm can be extended to any SC topology. A minimum of 250*MHz* switching frequency is required to achieve target efficiency greater than 90% and the target voltage greater than 0.85*V* having a switch size (unit cell) corresponding to $R_{on}$ equal to 10Ω. MATLAB results are compared with PSpice model and it is concluded that $V_{out}$ and the efficiency are almost the same using both the tools at the lower switching frequency. At higher switching frequencies, a deviation of 4% occurs in MATLAB and PSpice simulations due dominating effect of parasitic losses. A MATLAB-based model can automate these design techniques to enable rapid optimization of SC topologies.

In future, the series-parallel analysis done in this paper can be extended to other SC topologies. The two-phase converters analysed for optimum efficiency can be extended to analyse multi-phase converters. Further, the impact of pre-driver parasitic, leakage current can be investigated. Also, the ideal switches can be replaced with practical ones for better results.

## Nomenclature

| | |
|---|---|
| $V_{out}$ | target voltage ($V$) |
| $I_{load}$ | load current ($mA$) |
| $f_{sw}$ | switching frequency ($MHz$) |
| $N_s$ | switch size (number of transistors connected in parallel for scaling transistor width) |
| $R_{SSL}$ | slow switching limit impedance ($\Omega$) |
| $R_{FSL}$ | fast switching limit impedance ($\Omega$) |
| $R_{out}$ | output resistance ($\sqrt{R_{SSL}^2 + R_{FSL}^2}$, $\Omega$) |
| $C_1$& $C_2$ | flying/tank capacitors ($pF$) |
| $C_{bott}$ | bottom plate capacitance of the flying capacitor ($fF$) |
| $C_{sw}$ | switch parasitic gate capacitance ($fF$) |
| $R_{esr}$ | the equivalent series resistance of flying capacitor ($\Omega$) |
| $R_{on,\,i}$ | on-resistance (drain to source) of an $i^{th}$ switch ($\Omega$) |
| $q_c^j$ | capacitor charge flow in the $j^{th}$ phase ($C$) |
| $q_r^j$ | switch charge flow in $j^{th}$ phase ($C$) |
| $q_{out}^j$ | output charge flow in the $j^{th}$ phase($C$) |
| $q_{out}$ | total output charge flow ($C$) |
| $a_c^j$ | capacitor charge multiplier in the $j^{th}$ phase |
| $a_{out}$ | charge multiplier for total output charge flow |
| $a_{in}$ | charge multiplier for total input charge flow |
| $C_i$ | capacitance for $i^{th}$ flying capacitor ($pF$) |
| $a^1$ | capacitor charge multiplier vector in phase 1 |
| $a^2$ | capacitor charge multiplier vector in phase 2 |
| $a_r^1$ | switch charge multiplier vector in phase 1 |
| $a_r^2$ | switch charge multiplier vector in phase 2 |
| $a_{r,\,i}$ | charge multiplier of $i^{th}$ switch |
| $a_r$ | total switch charge multiplier vector |
| $D_i$ | a duty cycle of the $i^{th}$ switch |
| $n/m$ | converter transformation ratio |
| $\varphi_1$&$\varphi_2$ | phase 1 and phase 2 (non-overlapping clock phase generation) |
| $V_{in}$ | supply voltage ($V$) |
| $P_{loss,ssl}$ | power loss due to SSL impedance ($W$) |
| $P_{loss,fsl}$ | power loss due to FSL impedance ($W$) |
| $P_{RES}$ | total conduction/resistive power loss ($W$) |
| $V_{sw,\,cap}$ | switch blocking voltage (off state, $V$) |
| $P_{loss,swcap}$ | power loss due to parasitic switch capacitor ($W$) |
| $V_{cap}$ | bottom plate capacitor voltage ($V$) |
| $P_{loss,bottcap}$ | power loss due to the bottom plate capacitor ($W$) |
| $\alpha$ | the ratio of $C_{fly}/C_{bott}$ |
| $P_{loss,esr}$ | power loss due to ESR ($W$) |
| $P_{sw}$ | total switching power loss ($W$) |
| $V_{out,\,actual}$ | actual output voltage including $R_{load}$($V$) |
| $V_{out}$ | ideal output voltage ($V$) |
| $V_{out,actual}/V_{out}$ | maximum power stage efficiency |
| $P_{out}$ | total output power ($W$) |
| $P_{total,\,loss}$ | total power loss ($W$) |
| $\eta$ | SC converter efficiency |
| $k_R$, $k_C$ | process constant |
| $W$ | width of the transistor ($NMOS/PMOS$) |

## Declarations

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**Conflicts of interest/Competing interests** – On behalf of all authors, the corresponding author states that there is no conflict of interest.

**Availability of data and material** – Data will be made available on reasonable request.

## References


[1] Somalinga, S.S., Santha, K. (2021). Modified high-efficiency bidirectional DC–DC converter topology. *J. Power Electron.* 21**,** 257–268.

[2] Kesarwani, K., Sangwan, R. (2015). Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation. *IEEE Trans. Power Electronics*, 30, 6966 – 6977.

[3] Tiwari, K., Saini, D.S. & Bhooshan, S.V (2018). Efficient Detection for Improving ASEP Performance of MIMO Composite Fading Channel with Generalized Noise. *Wireless Pers Commun* 98, 2913–2923.

[4] Lavanya, A., Jegatheesan, R. & Vijayakumar, K (2021). Design of Novel Dual Input DC–DC Converter for Energy Harvesting System in IoT Sensor Nodes. *Wireless Pers Commun* 117, 2793–2808.

[5] Villar-Pique, G., Bergveld, H., Alarcon, E. (2013). Survey and benchmark of fully integrated switching power converters: SC versus inductive approach. *IEEE Trans Power Electronics*, 28(9), 4156–4167.

[6] Rahim, N.A., Amir, A., El Khateb, A. et al. (2016). Gain and efficiency analysis of 2-stage switched capacitor (SC) boost based dc-dc converter. In *Proceedings of 4th IET Clean Energy and Technology Conference (CEAT)* (pp.1-5).

[7] Suciu, V. M., Salcu, S. I., Pintilie, L. N., Teodosescu, P. D., Mathe, Z. (2018). Theoretical efficiency analysis of a buck-boost converter for wide voltage range operation. *2018 10th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)* (pp.1-4). s

[8] Sanders, S. R., Alon, E., Le., H. P., et al. (2013). The Road to Fully Integrated DC-DC Conversion via the SC Approach. *IEEE Trans Power Electronics*, 28(9), 4146–4155.

[9] Rikhtegar Ghiasi, R., Sahafi, A., Sobhi Geshlaghi, J. *et al.* (2015). A 2:1 switched-capacitor DC–DC converter for low power circuits. *An International Journal of Analog Integrated Circuits and Signal Processi*ng, 84, 215–222.

[10] Burton, E. A., Schrom, G., Paillet, F., et al. (2014). Fully integrated voltage regulators on 4th generation intel core SOCS. In *Proceedings of 2014 29th IEEE conference on Application Power Electronics* (pp. 432-439). IEEE.

[11] Seeman, M. D. (2009). *A design methodology for SC DC-DC converter*. Ph.D. Thesis, University of California, Berkeley.

[12] Bhattacharyya, K., Mandal, P. (2014). An approach to design and implementation of on-chip clock generator for the switched capacitor based embedded DC–DC converter. *Computers & electrical engineering*, 40(4), 1042-1052.

[13] Seeman, M. D., Sanders, S. R. (2008). Analysis and optimization of SC dc-dc converters. *IEEE Trans Power Electronics*, 23(2), 841–851.

[14] Le, H. P., Sanders, S. R., Alon, E. (2011). Design techniques for fully integrated SC DC-DC converters. *IEEE J solid-state circuits*, 46, 2120-2131.

[15] Makowski, M. S., Maksimovic, D. (1995). Performance limits of SC dc-dc converters. In *Proceedings of 1995 international conference on Power Electronics Spec.* (pp. 1215–1221).

[16] Zanwar, M., Sen, S. (2016). Switch selection and sizing in CMOS implementation of variable output switched capacitor step down DC-DC converter. In *Proceedings of 2016 IEEE international conference on electronics, circuits and systems (ICECS)* (pp. 1-4). ICECS.

[17] Mohammed, S. A., Dogan, H., Ozgun, M. T. (2017). An 85% efficiency reconfigurable multi-phase SC DC-DC converter utilizing frequency, switch size and interleaving scaling techniques. *Microelectronics*, 67, 155-161.

[18] Souza, R. D., Barbi, I. (2015). Minimum power losses operation for SC converters. In *Proceedings of 2015 17th European conference on power electronics and applications* (pp. 1-9).

[19] Jan, C. H., Bhattacharya, U., Brain, R., et al. (2012). 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra-low power, high performance and high density SoC applications. In *Proceedings of 2012 IEEE International conference on electron devices meeting (IEDM)* (pp. 1-4). IEEE.

[20] Jain, R., Geuskens, B. M., Kim, S. T., et al. (2014). A 0.45-1 V fully integrated distributed SC DC-DC converter with high-density MIM capacitor in 22nm tri-gate. *IEEE J solid-state circuits*, 49, 917-927.

[21] Saadat, A., Murmann, B. (2015). A 0.6V-2.4V input, fully integrated reconfigurable switched capacitor DC-DC converter for energy harvesting sensor tags. In *Proceedings of 2015 IEEE conference on solid-state circuits (A-SSCC)* (pp. 1-4). IEEE.

[22] Jung, I. S., Kim, Y. B., Chai, M. (2011). The novel SC DC-DC converter for fast response time and reduced ripple. In *Proceedings of 2011 IEEE 54th International Midwest Symposium on circuits and systems (MWSCAS)* (pp. 1-4). IEEE.

[23] Nurhuda, H. F., Yang, Y. (2014). A three topology-based, wide input range SC DC-DC converter with low ripple and enhanced load line regulation. In *Proceedings of 2014 IEEE 14th International Symposium on integrated circuits (ISIC)* (pp. 18-16). IEEE.