Modeling and Simulation of Low Power Single Event Upset-resilient SRAM cell

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ABSTRACT

Radiation induced soft errors impact memory circuits and their response gets transposed or disturbed which makes it crucial to protect the memory unit. Radiation-immune memory devices have extensive applications in space, biomedical, smart devices, and wearable devices. A radiation hardened by design circuit using Dual Interlocked Storage Cell (DICE) is implemented with varied transistor sizing to propose the design that has optimum performance and power dissipation. The design is tested for Single Event Upsets using the double exponential current model for current source of maximum amplitude 1 A. The proposed design is validated in Cadence 180nm CMOS technology node at ±10% of V_{DD} = 1.8 V. The sensitivity of the circuit to process, voltage and temperature variations are shown with the help of Monte Carlo simulations. Various iterations performed during simulations make the proposed circuit suitable for use in critical applications.

Keywords: radiation hardening, transistor sizing, soft error, parametric variation, single event upset.

1. INTRODUCTION

With the continued reduction in pipeline depth, downscaling of nodal capacitance and supply voltages, radiation induced soft errors are gaining attention and will soon be as critical as directly induced errors [1]. Radiation induced soft errors continue to affect the reliability of semiconductor devices at ground level [2-3]. The errors induced from radiation are collectively termed as single-event effects (SEE). The most common cause of their occurrence is heavy ion interactions with nitrogen or oxygen atoms in the atmosphere leading to the active area of a VLSI circuit being hit by neutrons or ionizing particles.

Transient SEEs are the major problem in modern VLSI circuits, although permanent SEEs like latch up, shifts in threshold voltage and destructive burnouts in power semiconductors [4-6] also continue to be a concern. A single-event transient pulse, typically having a pulse width of 0.1-1ns range at the output occurs when the reverse biased junction of a transistor is hit by an ionizing particle leading to charge deposition along its track [7]. If the transistor that gets affected turns out to be a component in a storage element like an SRAM cell or a latch, that transistor might flip its state and lead to an upset called the Single Event Upset (SEU). Another cause of occurrence of an SEU could be if the transistor that gets hit is a part of combinational logic because of an SET that is strong enough to propagate and reach where a storage element is latched. Despite that, SEU induced errors are transient(correctible) rather than permanent, and hence called as soft errors. SEU effects have been identified as the utmost threat to electronic systems operating reliably in the future by the Semiconductor Industry Association Roadmap [8-9].

Radiation-induced soft errors are a threat to the basic functionality of any logic cell. Data corruption and system failures because of the inability to eliminate radiation induced soft errors might have dangerous results in mission critical systems such as mainstream servers, automobile, and spacecrafts [10-11]. With technology scaling reaching deep submicron dimensions of less than 250nm, frequency of operation reaching to 100MHz and the increased speed and complexity of around a million gates in a circuit, Single Event Transient (SET) issues became a commonly occurring problem by the end of the 90s [12]. Therefore, SET tolerance needs to be a part of all logic circuits, especially in critical applications [13].

The increased packing density has made the memory and logic circuits more susceptible to be attacked by soft errors. The SRAM cell is, especially, most prone to soft errors because it has a wide range of delicate part for each bit [14]. These errors can be categorized as cumulative effects of the dose received, known as Total Ionizing Dose (TID) and effects of a single particle hitting the device, named Single Event Effects (SEE).

When a highly energetic ionized particle crashes with a memory cell, the logic stored in it changes and a bit flip results. This situation is defined as a Single Event Upset (SEU). Static Random-Access Memories (SRAMs) are most exposed to these SEUs induced through radiations [15]. When a SET propagates to the output resulting in storage of incorrect value, then it is referred as an SEU. The cause for the occurrence of a Single Event Upset (SEU) can be the charged particle striking the memory element directly or an SET causing the transient disturbance in a logic gate which propagates to reach the memory element and is then latched by this memory element.

While a design engineer works on circuit level strategies, the emphasis is on memory cells with such resilience that there will be no bit flip even when a radiation strike hits multiple nodes of the cell. A number of schemes to tolerate errors have been designed and proposed which are known as Radiation Hardened by Design (RHBD) techniques. RHBD techniques can be in the form of spatial redundancy or temporal redundancy. Dual Interlocked Storage Cell (DICE) design is a spatial redundancy technique that increases the reliability of the system [16].

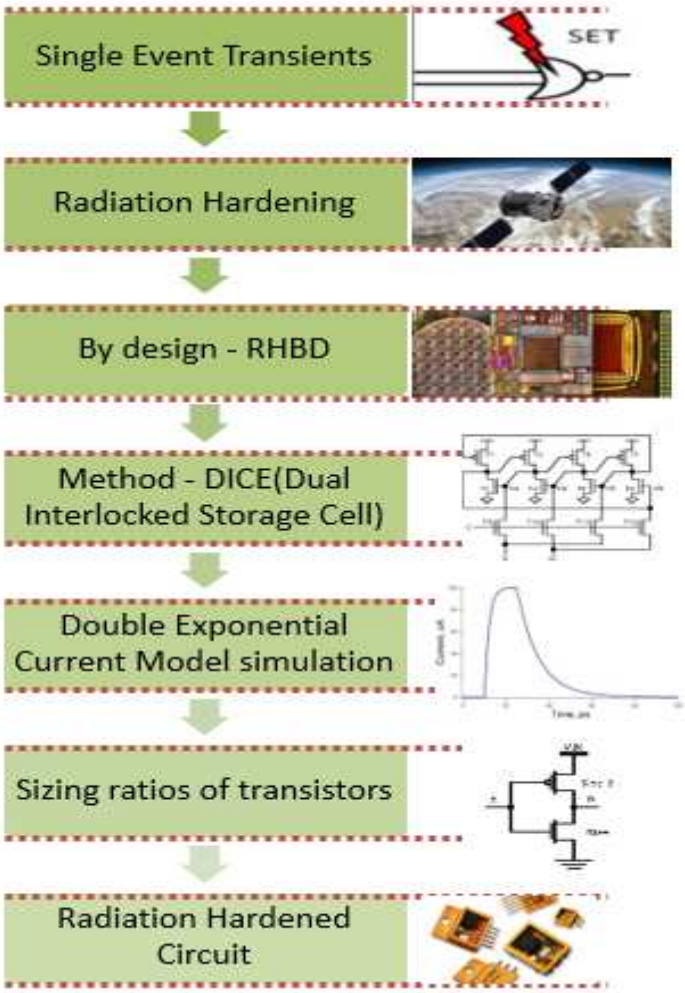


Fig. 1 Flowchart for a resilient design

2. SINGLE EVENT TRANSIENTS

Whenever a radioactive particle strikes a circuit, electron-hole pairs are generated. The holes and electrons are then separated by the electrical field and a current is created. If the current induced is adequate, it might lead to a change in the logic state of the transistor. Amplitude and duration of the current pulse are the key factors to ascertain whether the error propagates and if it can cause logic failure in the digital circuit. The following four conditions need to be fulfilled in order that an SET propagates and induces error in any memory element [17-19].

i) The node at which the SET is generated should be sensitive.
ii) It should either be a node of the memory circuit or propagate to reach a memory element.
iii) The amplitude and duration of the striking pulse should be able to change the memory state, and
iv) The cell should be vulnerable when the pulse reaches the memory element so that a bit flip can actually occur as a result of the incident pulse.

When a particle strikes an element, N- type Metal Oxide Semiconductor (NMOS) transistors generate the widest pulses. So, an NMOS transistor reacts to the current impulse more than a P-type Metal Oxide Semiconductor (PMOS) transistor. Hence, it is a more probable source of propagation of error [20].

Critical charge is defined as the minimum amount of charge necessary so as to flip a binary "1" to a "0" or vice-versa but it has to be less than the total charge that is stored. Q_{crit} (critical charge) is basically the difference between the charge at the storage node and the least value of charge required so that the sense amplifier can read correctly [21]. In the case of SRAM circuits, Q_{crit} also depends on the temporal shape of the current pulse and not only on the charge that gets collected at a certain node.

3. DOUBLE EXPONENTIAL TRANSIENT CURRENT MODEL

The physical phenomenon that is taking place during the occurrence of an SET is the generation of a double exponential current pulse from particle strike. This is the most widely used analytical model to approximate the transient current waveform that is induced at the struck node [22-24]. It has a rapid rise time and gradual fall time [25-27].

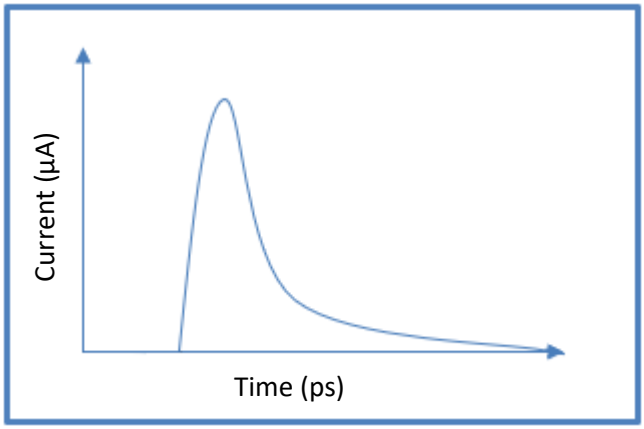


Fig. 2 A double exponential current

Expression of the pulse shown in Figure 2 is given as:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \quad (1)$$

where, I(t) denotes the transient current waveform, Q denotes the negative or positive charge deposited by the particle strike, τ_α is the fall time of current pulse, and τ_β is the rise time. The time constants τ_α and τ_β are process technology dependent parameters [28]. According to reference work [29], the time taken to collect charge for bulk CMOS technology is calculated as

$$\tau_\alpha = \frac{k\epsilon_0}{q\mu DN} \tag{2}$$

where $k \epsilon_0$ denotes the substrate dielectric constant, q is the electron charge, μ is the carrier mobility, D is the doping concentration, and N is a scaling factor, that scales doping concentration D to the rate of generation of electron-hole pairs. The values for τ_α are normally in the range of 50-100 ps. On the other hand, τ_β values are a few picoseconds usually. The typical value for τ_β is generally 10^{-11} s. The collection time constant is deemed as a more important parameter as compared to τ_β [30].
It has been reported previously as well [31] that current pulses with varying durations can occur because of particle strikes and critical charge can be expressed as an integral of equation (1) as:

$$Q = I_0 \int_0^\infty \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) dt = I_0 \times (\tau_\alpha - \tau_\beta) \tag{3}$$

where I_0 is the current pulse due to critical charge. This parameter critical charge is used to evaluate the SEU tolerance and it is defined as the minimum charge that leads to the state flip [32]. Iterations performed with small increments in the injected charge are used to determine the critical charge required for the occurrence of a soft error at every node. Before evaluation of the effects of SET in any design, charge collection current and time constants need to be found out for a given technology.

The voltage pulse generated at the node where the SET strikes is dependent on the supply voltage used in the circuit and the resistance as well as capacitance of the struck node. It is denoted as V(t) and the expression is given in Equation (4) as follows:

$$V(t) = \frac{I_0 - \tau_\alpha R}{\tau_\alpha - R}\left(e^{-t/\tau_\alpha} - e^{-t/RC}\right) \tag{4}$$

where R and C denote the resistance and capacitance of the struck node respectively.

There is a minimum value of amplitude voltage of pulse, below which it cannot propagate through subsequent stages. The pulse will slowly die down and there won't be a logic upset if the value of voltage generated by the upset is less than that threshold voltage value. The second factor for SET propagation is pulse duration (T_{wmin}) for which the magnitude of the pulse should be greater than V_m in order to simulate SETs. Pulse width decreases with sizing and then saturates when (W/L) is further increased. It is safe to assume that an SET may propagate in larger digital gates even if the transient pulse strikes for a small duration.

4. RESULTS AND DISCUSSION

4.1 Experimental Setup

The proposed radiation hardened DICE based SRAM cell is implemented and verified for improved performance through simulations on IC6.1.5 release of the Virtuoso Front-end to Back-end design environment of Cadence tool. Transistor sizes are varied to reach the optimum sizing ratios for performance of the circuit. The operating voltage is kept as 1.8V. Spectre based fault-injection simulations were carried out for determining the SEU-susceptibility of the proposed circuit. Simulations based on Spectre can be carried out faster than 3D model simulations. Therefore, any digital circuit made up from a possible combination of the elementary target circuits can be investigated for SET behavior thoroughly and reasonably fast using Cadence. In the case of our DICE based SRAM cell circuit, inverter is the basic unit. All schematics are designed using 180nm NMOS and PMOS device models. Table 1 shows the chosen (W/L) (width/length) ratios for both NMOS and PMOS devices.

TABLE 1. Sizing ratios for the chosen circuit

Device	Aspect ratio (W/L)	W_p/W_n (Width of PMOS/Width of NMOS)
PMOS	605nm/360nm	1.374
NMOS	220nm/180nm	
Access Transistor	420nm/180nm	

A single event upset is emulated on the circuit with the help of a double exponential current source. This source enables us to find out how the electrical characteristics of the circuit change when a high energy particle strikes the circuit. Figure 3 represents the formation of a charge cloud at the sensitive node in the circuit where the particle strikes.

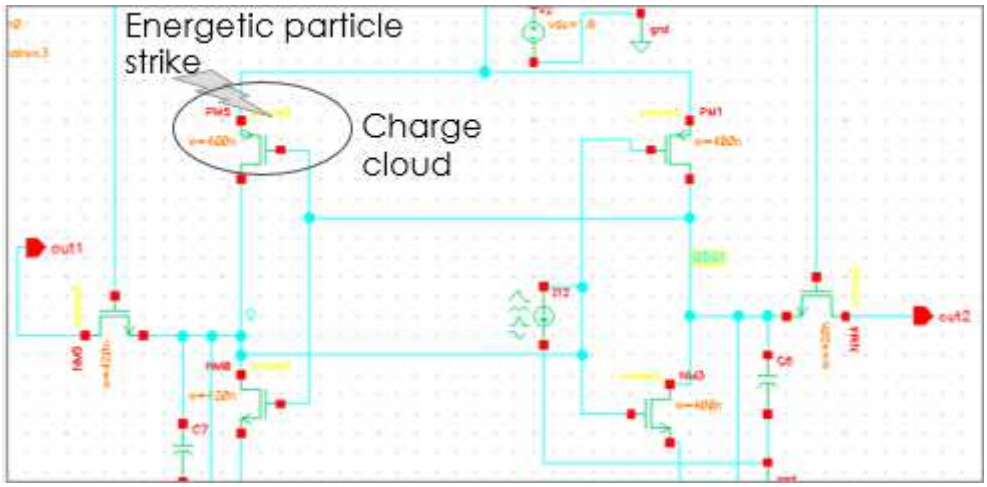
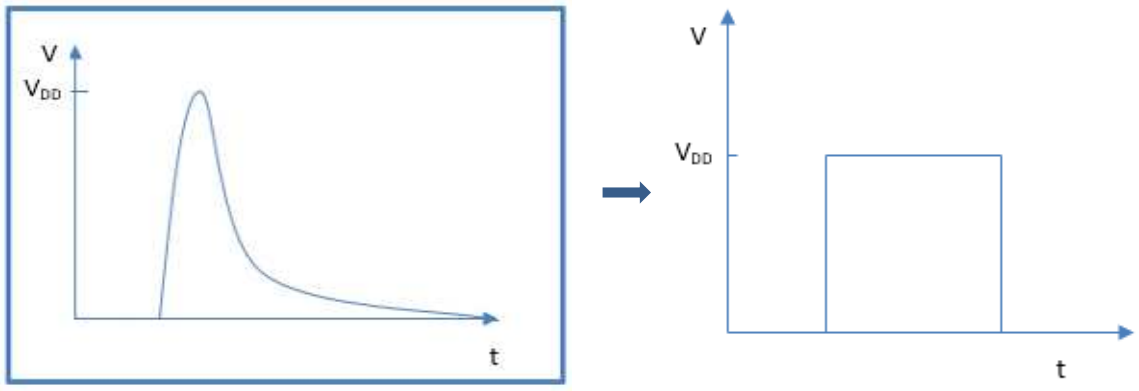


Fig. 3 A particle strike shown on the schematic of the circuit

Figure 4 shows the injection of a transient fault on a sensitive node to represent a flip from logic high to logic low (1→0). Some earlier works have also used similar approaches [33-35]. τ_α and τ_β values are kept as 16.4ns and 500ns respectively for our proposed design. These are the typical values for a single event upset-hardened circuit. Figure 4(a) denotes the double exponential pulse that has been used in the proposed design.



(a) (b)

Fig. 4(a) A double exponential current source with parameters as: I_{peak} = 100 µA, Rise Time(τ1) = 2ps, Fall Time(τ2) = 10ps, Rise Time delay (t_{d1}) = 10ps, Fall Time delay (t_{d2}) = 5ps **(b)** The pulse after getting shaped into a square wave

The circuit response after the transient pulse has propagated through some library cells is shown in Figure 4(b). The SET gets shaped into a square wave. The schematic of a DICE based SRAM cell is shown in Figure 5.

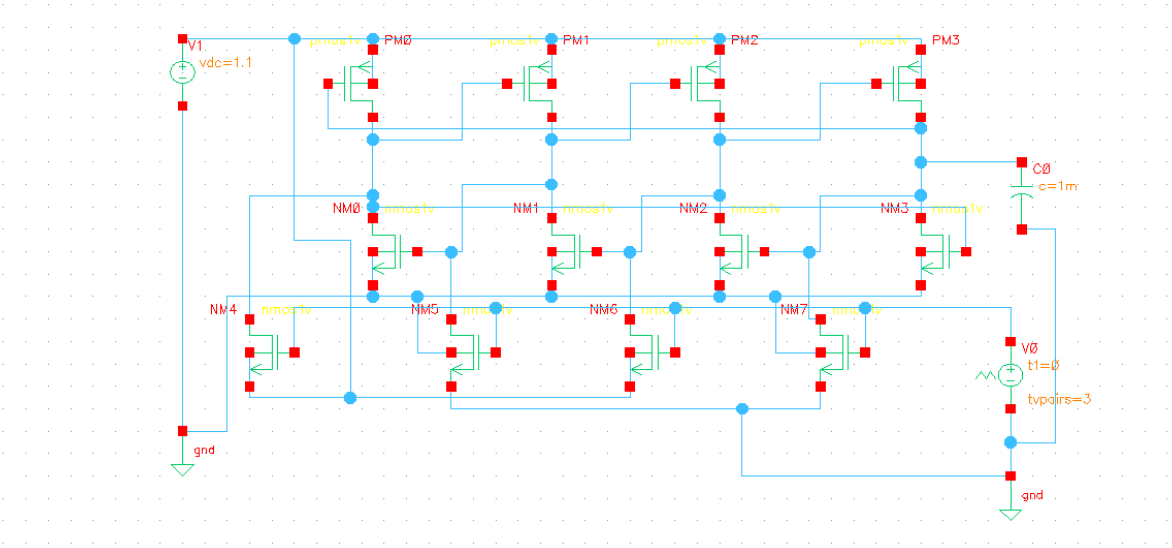


Fig. 5 Schematic of the proposed DICE based SRAM circuit

4.2 Simulation Results

The fluctuation of the threshold, channel length and width caused by process variations and mismatch in a device can lead to variation in parameters which can be found out before fabrication through statistical analysis. The rise time and fall time for the circuit implemented are taken as 2ps and 10ps, respectively. An important problem in the Deep Sub Micron (DSM) era is the surge in process variations. Due to the continuous scaling of devices and interconnects, there is a tremendous increase in variations in parameters such as channel length, threshold voltage, oxide thickness, wire width and wire height. Variations are present in every individual component and the characteristics of the circuit vary because of sum of the variations of components. Monte Carlo simulations have been carried out for different number of runs using Cadence Spectre at 180nm technology and the results are presented in Table 2. The power dissipation of DICE circuit is simulated for various process corners such as nominal (NN), fast slow (FS), slow fast (SF), fast fast (FF) and slow slow (SS) for supply voltages varying in the range of ±10% of V_{DD}. The temperature variation range is kept from 0^0 C to 100^0 C for testing memory circuits [36].

TABLE 2 Power dissipation in proposed DICE circuit under PVT (Process Voltage Temperature) variations

Parameter		Power Dissipation
Supply Variation	1.62 V	284.9pW
	1.8 V	343.2pW
	1.98 V	408.3pW
Process Variation (for 1000 samples at 85^0C)	SS	124.1nW
	NN	125nW
	FS	132.9nW
	FF	134.8nW
	SF	135.6nW

Temperature Variation	0^0C	343.2pW
	27^0C	1.052nW
	85^0C	124nW
	100^0C	695.4nW

The power dissipation of the circuit increases for higher voltage supply value. For temperature also, the minimum power dissipation is obtained for the circuit operating at the lowest temperature taken as 0^0C. Figure 6 shows the graphical representation of the results presented in Table 2.

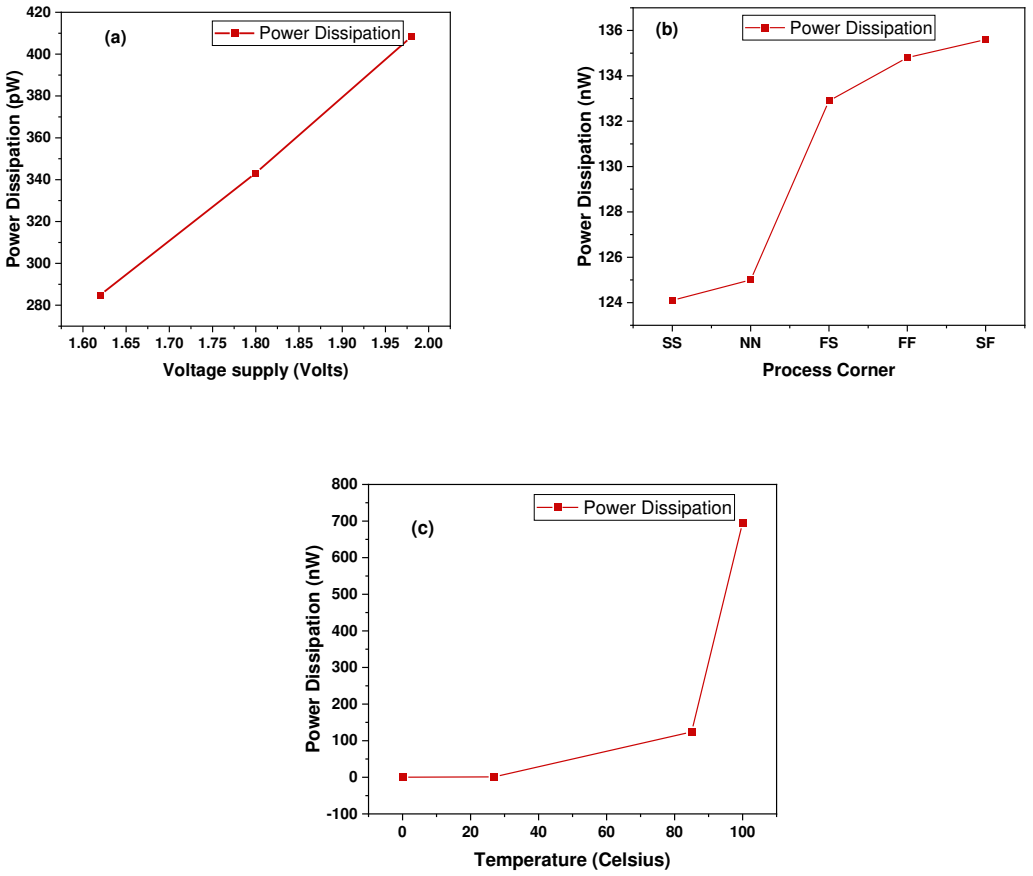


Fig. 6(a) Response of Power dissipation to supply voltage variations **(b)** Response of Power dissipation to process corners **(c)** Response of power dissipation to temperature variations

4.3 Comparison based on Performance and Power

A highly fault tolerant circuit in SEU hardened memories makes use of adding redundant circuitry at the cost of some compromise in performance and power dissipation. Mean(μ), median and standard deviation(σ) of the circuit play a role in measuring the sensitivity of the circuit. This is an even more important factor in circuits where radiation hardening is the goal. The ratio of mean and standard deviation(μ/σ) can be used as a measure of the sensitivity of circuits to process variation [37]. The circuit showing higher value of μ/σ denotes lesser variation with process changes. The sensitivity of the proposed circuit to both process and mismatch variations can be observed from the μ/σ values. Table 3 below represents highest sensitivity to variations in the circuit proposed.

TABLE 3 Comparison of sensitivity with varying number of samples and existing similar work

Design	Number of Samples	Minimum Power (pW)	Maximum Power (μW)	Mean(μ) (nW)	Standard Deviation(σ) (μW)
Proposed	1000	12.65	15.53	1.472	1.153
	500	14.32	15.12	1.365	1.246
	200	16.17	11.35	1.112	1.335
Liu et al [38]	-	-	-	455.2	-
T. Calin et al [39]	1000	-	-	0.00139	0.15

The sensitivity of the circuit which is proportional to the factor calculated above denoted as σ/μ changes with parametric variations like process corner, voltage supply and temperature. This variation is graphically represented in Figure 7.

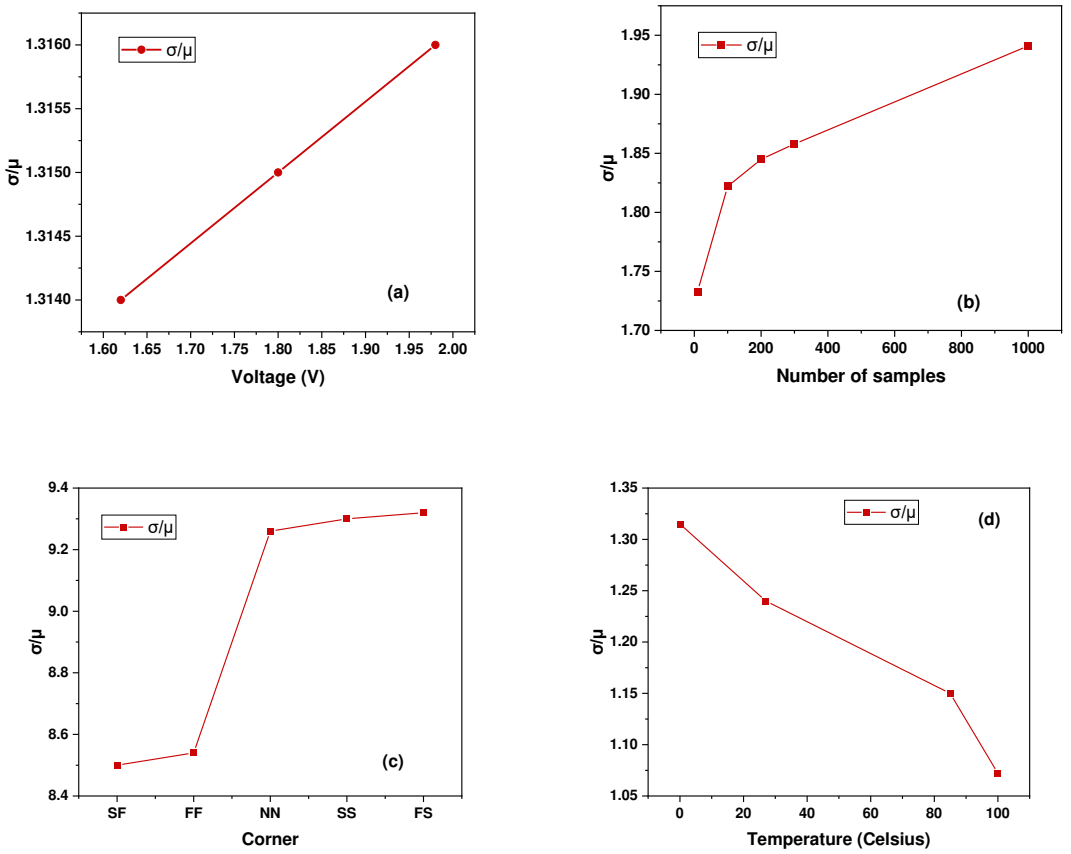


Fig. 7(a) Variation in sensitivity with respect to voltage **(b)** Variation in sensitivity with increasing number of samples **(c)** Variation of sensitivity for various process corners **(d)** Variation of sensitivity at varying temperatures.

5. CONCLUSION

This paper proposes a radiation hardened by design-based SRAM circuit which makes use of redundancy. Transistor sizing has been used to find the circuit design parameters which offer the lowest power dissipation and optimum circuit performance. The functionality of the circuit under the effect of double exponential current source is tested and validated. Effects of parametric variations and sensitivity of the circuit are considered. The circuit is sensitive to process, voltage and temperature variations as shown through Monte Carlo simulations. The rise in use of electronic systems for safety-relevant applications related to medical devices, or in automated systems targeting active driver safety (e.g. Automatic Braking System, Electrical Submersible Pump) has enhanced the importance of reliability.

Declarations

Funding and Conflicts of Interest/ Competing Interests

The authors have no relevant financial or non-financial interests to disclose.
The authors have no conflicts of interest to declare that are relevant to the content of this article.

Availability of Data and Material
Not applicable

Code availability
Not applicable

Ethics Approval
Not Applicable

Consent to Participate
Not Applicable

Consent for Publication
Not Applicable

Author's contributions
Neha Pannu is the corresponding author of the manuscript. She prepared the first draft of the manuscript after compiling the results achieved from experiments and simulations. Neelam Rup Prakash suggested the flow of work and both the authors read and approved the final manuscript.

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Not Applicable

References

[1] Shivakumar P, Kistler M, Keckler SW, Burger D, Alvisi L. Modeling the effect of technology trends on the soft error rate of combinational logic. InProceedings International Conference on Dependable Systems and Networks 2002 Jun 23 (pp. 389-398). IEEE.
[2] Wrobel F, Dilillo L, Touboul AD, Pouget V, Saigné F. Determining realistic parameters for the double exponential law that models transient current pulses. IEEE Transactions on Nuclear Science. 2014 Mar 6;61(4):1813-8.
[3] Krishnaswamy S, Markov IL, Hayes JP. Design, analysis and test of logic circuits under uncertainty. Springer Science & Business Media; 2012 Sep 21.
[4] Normand E. Single-event effects in avionics. IEEE Transactions on nuclear science. 1996 Apr;43(2):461-74.
[5] Dyer C, Rodgers D. Effects on spacecraft & aircraft electronics. InProceedings ESA Workshop on Space Weather, ESA WPP-155 1998 Nov (pp. 17-27).

[6] Schwank JR, Shaneyfelt MR, Paillet P, Beutler DE, Ferlet-Cavrois V, Draper BL, Loemaker RA, Dodd PE, Sexton FW. Optimum laboratory radiation source for hardness assurance testing. IEEE Transactions on Nuclear Science. 2001 Dec;48(6):2152-7.
[7] Varadan Savulimedu Veeravalli, Thomas Polzer, Ulrich Schmid, Andreas Steininger, Michael Hofbauer, Kurt Schweiger, Horst Dietrich, Kerstin Schneider-Hornstein, Horst Zimmermann, Kay-Obbe Voss, Bruno Merk, Michael Hajek, An infrastructure for accurate characterization of single-event transients in digital circuits, Microprocessors and Microsystems, Volume 37, Issue 8, Part A, 2013, pp. 772-791. https://doi.org/10.1016/j.micpro.2013.04.011.
[8] Allan A, Edenfeld D, Joyner WH. J., Kahng, A., Rodgers, M., and Zorian, Y.(2002). 2001 Technology Roadmap for Semiconductors. Computer.;35(1):42-53.
[9] Wang HB, Bi JS, Li ML, Chen L, Liu R, Li YQ, He AL, Guo G. An area efficient SEU-tolerant latch design. IEEE Transactions on Nuclear Science. 2014 Oct 16;61(6):3660-6.
[10] Nicolaidis M, editor. Soft errors in modern electronic systems. Springer Science & Business Media; 2010 Sep 24.
[11] Pal S, Divya D, Ki WH, Islam A. Radiation-hardened read-decoupled low-power 12T SRAM for space applications. International Journal of Circuit Theory and Applications. 2021 Jul 15.
[12] Li J, Draper J. Accelerating soft-error-rate (ser) estimation in the presence of single event transients. In2016 53nd ACM/EDAC/IEEE Design Automation Conference (DAC) 2016 Jun 5 (pp. 1-6). IEEE.
[13] Prasad G, Mandi BC, Ali M. Low power and write-enhancement RHBD 12T SRAM cell for aerospace applications. Analog Integrated Circuits and Signal Processing. 2021 May;107(2):377-88.
[14] Zhao W, Cao Y. Predictive technology model for nano-CMOS design exploration. ACM Journal on Emerging Technologies in Computing Systems (JETC). 2007 Apr 1;3(1):1-es.
[15] Xu H, Zhu J, Lu X, Li J. An advanced SEU tolerant latch based on error detection. Journal of Semiconductors. 2018 May;39(5):055003.
[16] Diehl SE, Vinson JE, Shafer BD, Mnich TM. Considerations for single-event immune VLSI logic. InPresented at the 20th IEEE Ann. Conf. on Nucl. and Space Radiation Effects 1983 May.
[17] Diehl-Nagle SE, Vinson JE, Peterson EL. Single event upset rate predictions for complex logic systems. IEEE Transactions on Nuclear Science. 1984 Dec;31(6):1132-8.
[18] Friedman AL, Lawton B, Hotelling KR, Pickel JC, Strahan VH, Loree K. Single event upset in combinatorial and sequential current mode logic. IEEE Transactions on Nuclear Science. 1985 Dec;32(6):4216-8.
[19] Limbrick DB, Mahatme NN, Robinson WH, Bhuva BL. Reliability-aware synthesis of combinational logic with minimal performance penalty. IEEE Transactions on nuclear science. 2013 Feb 18;60(4):2776-81.
[20] Robinson P, Lee W, Aguero R, Gabriel S. Anomalies due to single event upsets. *Journal of Spacecraft and Rockets.* Mar-Apr 1994 ;31(2):166-171.
[21] Pickel JC, Blandford JT. Cosmic ray induced in MOS memory cells. IEEE Transactions on Nuclear Science. 1978 Dec;25(6):1166-71.
[22] Neto EH, Ribeiro I, Vieira M, Wirth G, Kastensmidt FL. Using bulk built-in current sensors to detect soft errors. Ieee Micro. 2006 Oct 16;26(5):10-8.
[23] Bajura MA, Boulghassoul Y, Naseer R, DasGupta S, Witulski AF, Sondeen J, Stansberry SD, Draper J, Massengill LW, Damoulakis JN. Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs. IEEE Transactions on Nuclear Science. 2007 Aug 20;54(4):935-45.
[24] Garg R, Khatri SP. 3D simulation and analysis of the radiation tolerance of voltage scaled digital circuit. In2009 IEEE International Conference on Computer Design 2009 Oct 4 (pp. 498-504). IEEE.
[25] Baumann RC. Soft errors in advanced semiconductor devices-part I: the three radiation sources. IEEE Transactions on device and materials reliability. 2001 Mar;1(1):17-22.
[26] Baumann R. Soft errors in advanced computer systems. IEEE Design & Test of Computers. 2005 Jun 6;22(3):258-66.
[27] Baumann RC. Radiation-induced soft errors in advanced semiconductor technologies. IEEE Transactions on Device and materials reliability. 2005 Dec 5;5(3):305-16.
[28] Sayil S. Soft error mechanisms, modeling and mitigation. Springer International Publishing; 2016 Feb 25.

[29] Velamala J, LiVolsi R, Torres M, Cao Y. Design sensitivity of single event transients in scaled logic circuits. In2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC) 2011 Jun 5 (pp. 694-699). IEEE.
[30] Ness DC, Hescott CJ, Lilja DJ. Improving nanoelectronic designs using a statistical approach to identify key parameters in circuit level SEU simulations. In2007 IEEE International Symposium on Nanoscale Architectures 2007 Oct 21 (pp. 46-53). IEEE.
[31] Mukherjee S. Architecture design for soft errors. Morgan Kaufmann; 2011 Aug 29.
[32] Jain P, Zhu V. Judicious choice of waveform parameters and accurate estimation of critical charge for logic SER. InProc. DSN 2007.
[33] Fazeli M, Patooghy A, Miremadi SG, Ejlali A. Feedback redundancy: A power efficient SEU-tolerant latch design for deep sub-micron technologies. In37th Annual IEEE/IFIP International Conference on dependable systems and networks (DSN'07) 2007 Jun 25 (pp. 276-285). IEEE.
[34] Mitra S, Zhang M, Waqas S, Seifert N, Gill B, Kim KS. Combinational logic soft error correction. In2006 IEEE International Test Conference 2006 Oct 22 (pp. 1-9). IEEE.
[35] Shao Y, Dey S. Separate dual-transistor registers: a circuit solution for on-line testing of transient error in UDMC-IC. In9th IEEE On-Line Testing Symposium, 2003. IOLTS 2003. 2003 Jul 7 (pp. 7-11). IEEE.
[36] HE N, Harris D. CMOS VLSI design: A circuits and systems perspective. Addison-Wesley; 2011.
[37] Morgenshtein A, Yuzhaninov V, Kovshilovsky A, Fish A. Full-Swing Gate Diffusion Input logic—Case-study of low-power CLA adder design. Integration. 2014 Jan 1;47(1):62-70.
[38] Liu P, Zhao T, Liang F, Zhao J, Jiang P. A power-delay-product efficient and SEU-tolerant latch design. IEICE Electronics Express. 2017;14(23):20170972-s.
[39] Calin T, Nicolaidis M, Velazco R. Upset hardened memory design for submicron CMOS technology. IEEE Transactions on nuclear science. 1996 Dec;43(6):2874-8.

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