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Research Article

Design of a Fully Integrated VHF CP-PLL Frequency Synthesizer with an All-Digital Defect-Oriented Built-In Self-Test.

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Abstract

This paper presents the design of an on-chip charge pump phase-locked loop (CP-PLL) with a fully digital defect oriented built-in self-test (BIST) for very-high frequency (VHF) applications. The frequency synthesizer has a 40 to 100 MHz tuning range and uses a ring voltage-controlled oscillator for frequency synthesis. The PLL exhibits a phase noise of -132 dBc/Hz at 1 MHz and consumes 1.8 mW on a 3 V supply. The BIST implementation uses fewer external input or output, is capable of efficient fault diagnosis, and is compact, posing a low area overhead. The integrated circuit design was realized in the AMI 0.6 μ complementary metal oxide-semiconductor process.

Keywords: CP-PLL; BIST; Defect-Oriented; VHF; CMOS; Synthesizer; All-digital.

Introduction

The PLL is a very essential and ubiquitous component of modern electronics and finds a widespread use in communication systems where it is used for frequency synthesis or clock generation/synchronization/recovery. Other applications include frequency modulation and demodulation. Its use is indispensable for clock distribution, particularly in complex high performance synchronous systems where it is very difficult to distribute clean, low-skew high-frequency, phase synchronous, tunable clock signals reliably throughout various devices and package technologies (single-chip modules, multichip modules, cards etc.). A PLL-based system design allows the distribution of a relatively low-frequency reference clock to each or group of components. Each component's PLL multiplies the reference to the required high frequency signals for use while maintaining proper phase alignment.

A PLL is described as a non-linear system that uses negative feedback to 'lock' an output signal in phase (hence frequency) with a reference signal. The loop combines a voltage-controlled oscillator (VCO) and a phase/frequency comparator so connected that the oscillator maintains this constant relative phase angle relationship. Other basic components include a frequency divider, charge pump and a loop filter. The VCO generates an output signal based on the input reference clock. VCOs used in PLL frequency synthesizers are commonly realized using LC-tanks [1, 2] or ring topologies [3, 4]. Generally, LC-VCOs consist of an inductor L and voltage-tunable capacitor C forming a parallel tank which oscillates at $\frac{1}{2\pi\sqrt{LC}}$. They also feature active elements which compensate for losses in the inductor. Ring VCOs rely on an interconnection of amplifiers or inverters to achieve a 360° phase shift, which causes the structure to oscillate. In the designs, where single-ended inverters are used, the number of delay stages are required to be odd to achieve the ringing effect. LC VCOs have the lower in-band phase noise and power consumption of the two but has a rather limited tuning range and occupies large die area in fully integrated PLLs. On the other hand, ring oscillators offer easier design or integration, smaller area, and traditionally wider tuning ranges at the cost of higher phase noise and power expenditure. Some works have demonstrated the design of low noise ring VCOs. However, their power consumption remains higher than that of their LC counterparts [5]. The phase/frequency detector (PFD) is a tri-state device which compares the phase difference between the reference input and the VCOs output signal. The PFD produces feedback error pulses proportional to the phase difference, to correct the discrepancy. The generated error signal is smoothed out by the CP integrator (CP + loop filter) and applied to the VCO to generate the desired signal. The PFD structure may be a simple XOR gate, latch-based or of the pre-charge type [6]. Finally, a PLL may require a feedback divider, programmable or fixed, to bring the VCO output to the range of the reference signal. The VCO signal can be tuned in integer steps of the reference clock or in fractional amounts. Figure 1 shows the architecture of a basic CP-PLL.

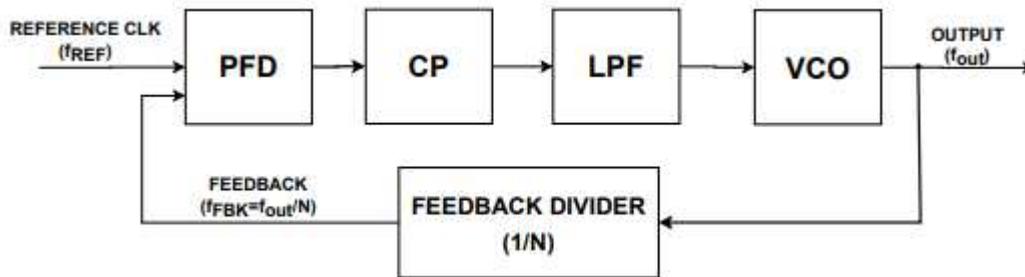


Fig. 1 Architecture of the charge-pump PLL

The basic BIST concept involves the design of test circuitry around or into a system to allow automatic measuring of system properties by generating and/or applying appropriate test stimuli and observing the response of the host system. This testing approach attempts to migrate parts of Automated Test Equipment (ATE) functionalities onto the chip for facilitated testing and reduced test cost. Various testing procedures are involved at three main phases of the hardware products design and manufacturing cycle: Pre-silicon verification, manufacturing tests, and post-

silicon validation. Fault diagnosis during manufacturing is very crucial and can greatly ease the workload on post-silicon validation. This is where BIST becomes relevant. A basic BIST structure introduces three hardware blocks into a host circuit: a test stimulus generator (TSG), a test controller and a response analyzer (Figure 2).

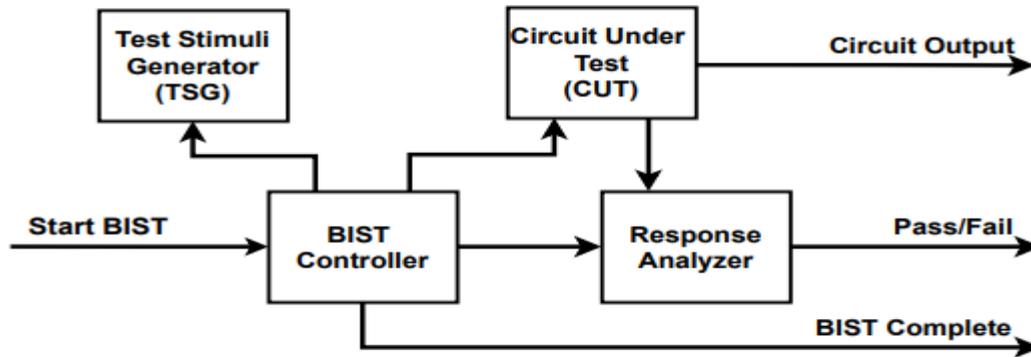


Fig. 2 Typical BIST structure [27]

The TSG produces a set of test vectors for a given circuit under test (CUT) depend on the specific faults being tested for and the required fault coverage. A TSG may come in the form of a read-only-memory (ROM) with stored patterns, a linear feedback shift register (LFSR), or a counter. The BIST controller manages all transactions in the self-testing procedure. BIST controllers typically have a single-input single-output external interface. An input signal activates self-test sequence after which the controller puts the CUT in test mode by allowing the TSG and the controller itself to drive the CUTs inputs directly though isolation circuitry like a multiplexer (MUX) or some other switching mechanism. Depending on the BIST paradigm, the controller feeds the TSG with signals required to generate test sequences. In some other cases, the TSG and the controller may even be fused into one block [7]. The controller also interacts with the response analyzer to ensure that the CUTs responses to the test suite are properly collected and compared with known outputs. The outcome of the comparison which informs whether the CUT is faulty or otherwise is compacted into a single pass/fail response using functions such as signature analysis or syndrome counts. Fault-free CUT responses are sometimes stored on- or off-chip for future reference. Hardware implementations of response analyzers include LFSRs, multiple-input shift registers (MISRs) or comparator logic with a ROM-based lookup table.

BIST paradigms are broadly classified as either defect oriented or functional. Defect-oriented schemes focus on the detection of possible structural flaws in a chip [8] whereas functional methods target direct on-chip measurement of performances [9–11]. Furthermore, a BIST scheme may be designed and appropriate for generic use or as a one-off solution. That is, the scheme may be applicable to any circuits class [12, 13], specific to a given class [14, 15], or even tailored to individual intra-class circuit architectures [16, 17]. Generic defect-oriented paradigms employ topology transforming techniques by integrating oscillation-based mechanisms [10, 18] or using structures such as pull-up/pulldown transistors [8]. Embedding BIST schemes into integrated circuits/systems is quite a complex task as an effective strategy must satisfy some very challenging requirements. The integration of

the BIST infrastructure should not require significant redesign or reconfiguration and it must be transparent to the main circuitry without degrading its performance. Furthermore, the test infrastructure must pose minimal overhead in terms of die real-estate and power consumption. Intuitively, a small footprint of BIST within the chip die reduces manufacturing costs as well as the probability of defect occurrence, considerably. An elegant way of achieving this goal is by re-purposing existing IC blocks as part of the test circuit where possible. The test paradigm should also have a fast response time to enable low-latency error detection. The speed criterion is also useful during the design phase because it allows for large-scale defect simulations in reasonable time and enables performing simulations for multiple test design iterations. Next, the BIST circuitry should be more rugged than the IC to guarantee low failure probability. As a good strategy, some BIST designs even attempt to include checker facilities to test the infrastructure itself [12, 19]. Finally, the BIST should also interface easily with standard test access mechanisms and must be portable across technology nodes without requiring significant reconfiguration.

In this paper, the design of a fully integrated PLL frequency synthesizer which operates from 40MHz to 100MHz is presented. The designed PLL exhibits phase noise of -132dBc/Hz at 1 MHz, which is low enough for a wide array of applications in the VHF band. An all-digital BIST is designed into the PLL core. The entire system is designed in a typical CMOS process using a 3 V power supply which is commonly found in today's portable products. The remainder of this paper is organized as follows: Section 2 presents the related works; section 3 considers the design of the CP-PLL core and the BIST including a stepwise description of their building blocks as well as the PLL-BIST integration. Experimental verification of the proposed design is described and discussed in Section 4. The paper is concluded in Section 5.

Literature Review

PLL since its inception has been integral especially in communication technology. In recent times, its advancements in integrated circuit (IC) technology have made it an indispensable tool in areas such as wireless systems [20], micro-electro-mechanical systems (MEMS) [21], consumer electronics [22], motor control [23], and many more. PLL employs a negative feedback architecture that enables economic multiplication of crystal frequencies by larger variable numbers. Information obtained from this field prompted a few studies aimed at developing phase locked loops with a handful of models and testing techniques developed. Classical VLSI testing methods have been employed in testing PLLs in the past. Off-chip testing process by means of Automatic Testing Equipment (ATE) is no exception. However, these systems have proved to be time consuming, expensive and do not provide sufficient high fault coverage. On-chip testing techniques emerged with Design-for-Test (DFT) and Built-in-self test (BIST) as modern and efficient means for testing PLLs. DFT scan designs had considerable limitations such as high-power dissipation and slow clock problems. BIST designs have made advances over DFT even though not much work has been done in recent years.

[24] presented a method for parametric built-in-self-test with realistic design constraint. In this model, the N and M dividers were initialized, and the test control unit awaited PLL synchronization. This synchronization was achieved by a lock signal generated by the phase detector. Built-in-self-test was then performed by using LFSRs (Linear-Feedback Shift Registers) and MISRs (Multi-Input Signature Registers) of the circuit under test (CUT). The original response of the test was then compared to a golden signature. The value of N is stored in the output register and subsequently incremented, provided the test was passed, else the test was restarted as long as N does not exceed N_{\max} and the test does not fail. The maximum frequency of the circuit under test can then be determined. The PLL utilized in this system was however not optimized for a large bandwidth. Hence detection of faults through direct and indirect measurements were not fully exploited.

[25] proposed a BIST technique which employs a two-step AC and DC testing technique. In this technique, the defective circuit under test is checked by monitoring fault signatures through output voltage signal characteristics. Based on the output signal characteristics according to the equation $v(t) = V_{DC} + V_m \sin(\omega t + \Phi)$, the AC testing was achieved by detecting changes in V_m whereas DC testing by changes in V_{DC} . V_m and V_{DC} are tested consecutively hence the name. Though this strategy is cost effective, it is only aimed at achieving on-chip testing in the pre-screening of defective chips before higher precision testing is carried out which makes it less robust.

Methodology

CP-PLL Core Design

The CP-PLL was designed as a fully integrated mixed signal core with digital blocks such as the PFD and purely analog parts like the VCO. The specifications for the integer-N design are listed below in Table 1. The division ratio N was fixed as 32. The design is based on a linearized model of the second-order CP-PLL. An in-depth non-linear analysis of the CP-PLL is rigorously discussed in [20]. The linearized form however suffices for this design.

Table 1: CP-PLL specifications.

Parameter	Value
Lock range	40 MHz - 100MHz
Phase noise (at 1 MHz)	< -100 dBc/Hz
Lock time	< 30 μ s
Supply voltage	3 V
Power budget	2 mW

As was established in Section 1, a simple odd chain of inverters oscillates at a fixed frequency $f_{vco} = f_{out}$. To create a variable f_{vco} oscillator, a simple tuning mechanism is to control the current through the inverters. Such a current source is driven by a control voltage V_{cntl} which determines an inverter's charge-discharge times. This current-

starved inverter topology was used in the VCO design. The VCO used seven-stage inverter network to produce signals in the 40 - 100 MHz frequency range as shown in Figure 3.

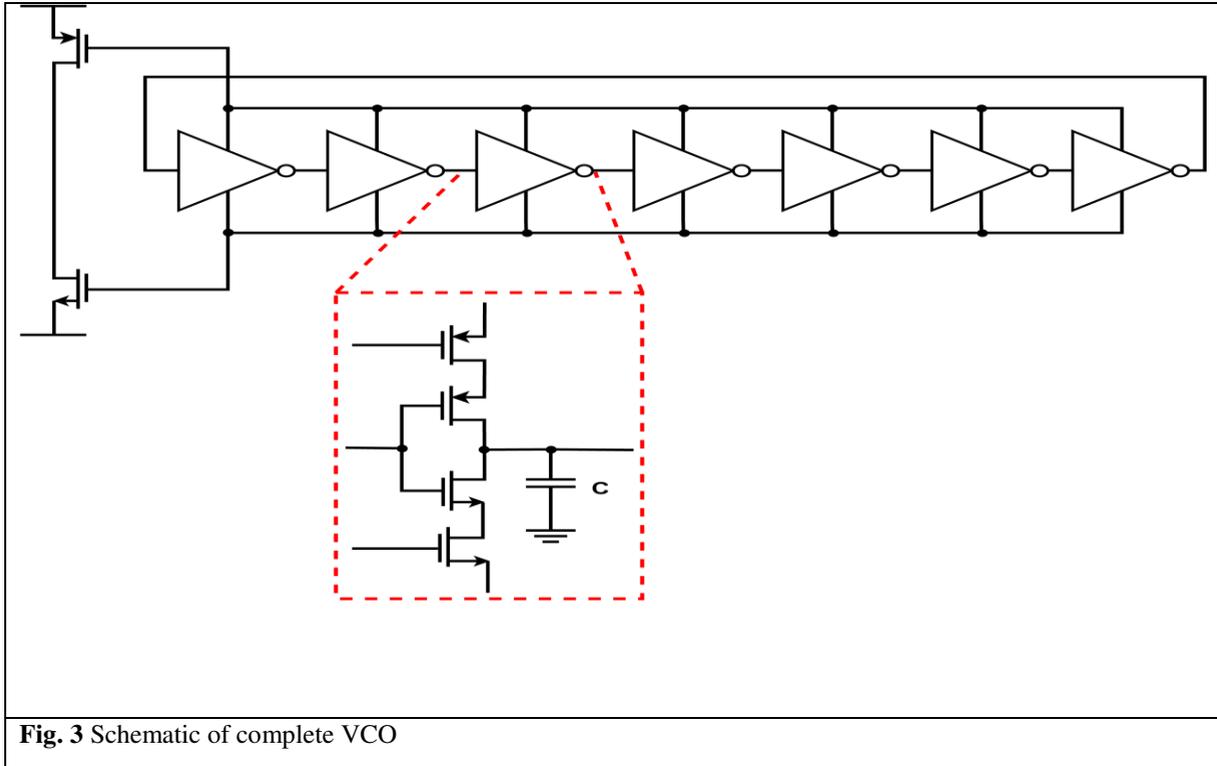


Fig. 3 Schematic of complete VCO

The oscillator was designed for a wider 30 - 105 MHz band to accommodate the extremes of the PLL's tuning range (f_{min} and f_{max}). The range was designed by appropriately sizing the inverter's transistors. The VCO's output waveform was improved by loading each inverter stage with a 220 pF capacitor. However, such as load increases the charge-discharge times of the stage and ultimately diminishes f_{vco} . An optimum trade-off was struck via simulations. A sweep of the VCO output signal's frequency is shown in Figure 4.

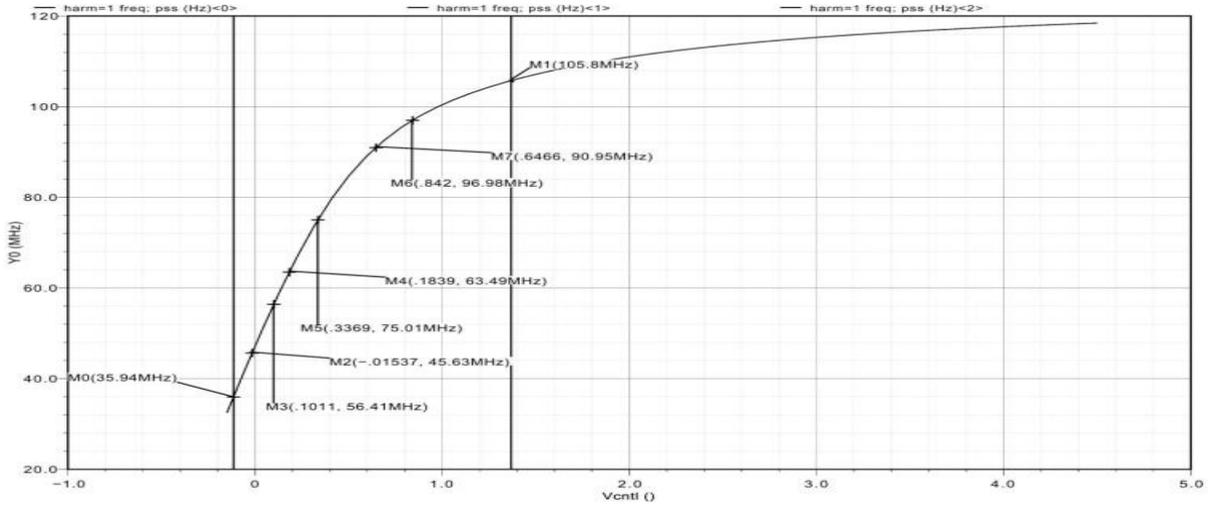


Fig. 4 VCO output frequency plot [27]

From the graph, the V_{cntl} range was found to be approximately 1.3 V. The VCO's gain K_{vco} is found to be:

$$K_{vco} = \frac{2\pi(f_{max}-f_{min})}{V_{cntl}} \approx 290Mrad/Vs \quad (1)$$

K_{vco} may be calculated by averaging the gradients of multiple shorter linear sections in the plot's non-linear operating region. The PFD was designed using a sequential phase and frequency detecting logic illustrated in Figure 5.

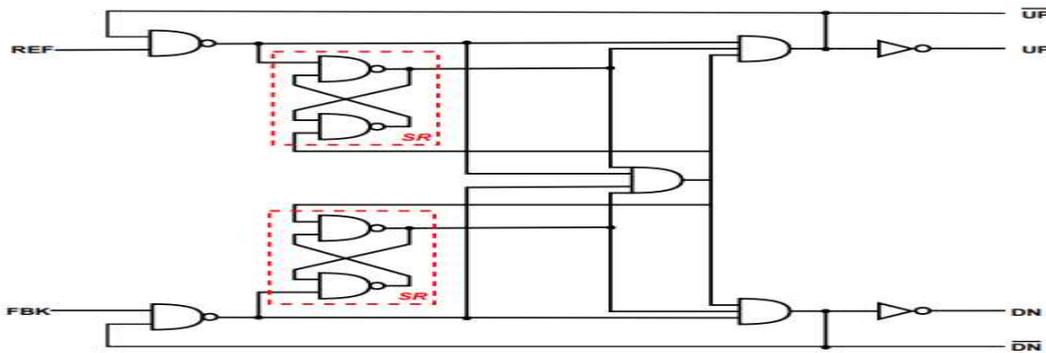


Fig. 5 Implemented dead-zone free phase detector

The detector generates short length UP and DOWN pulses for controlling the charge pump by comparing the input reference and feedback clock. For perfectly synchronized input waveforms, the PFD produces identical output pulses, causing their respective currents at the charge pump's output to cancel out. Contrarily, unequal UP and DOWN pulses produce a nonzero charge pump current which charges/discharges the loop filter to adjust the feedback clock phase or frequency. The charge-pump used in this design is shown in Figure 6.

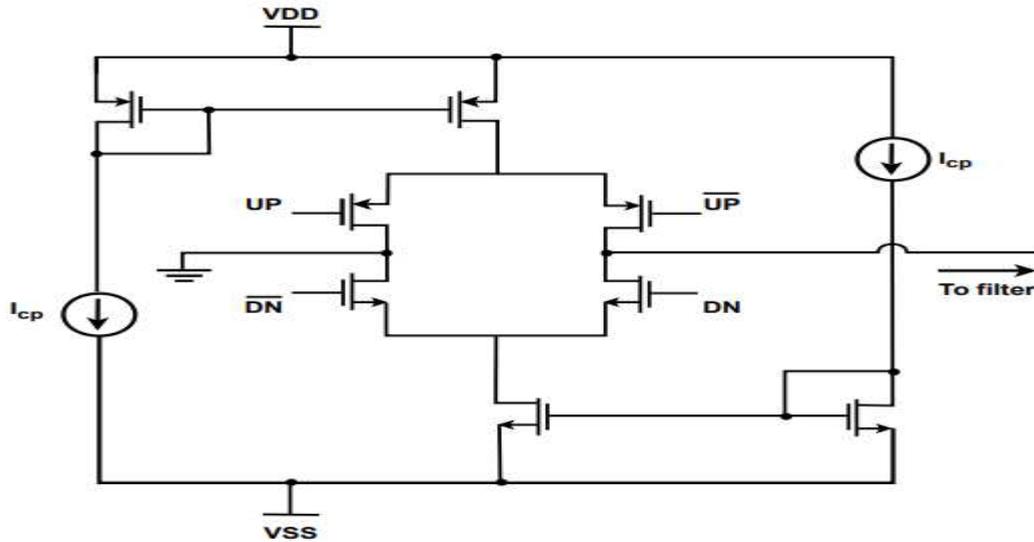


Fig. 6 Schematic of charge pump.

The presented PFD eliminates the dead-zone non-ideality by introducing delays into the loop, which work to turn both sources on simultaneously. It also has a lowered sensitivity to duty cycle variation. The critical path of the PFD circuitry is limited to three gate delays: one from the 4-input reset NAND and two from the two cross-coupled gate pairs (SR latches). With such a strategy, there is the risk of spurious noise injection to the output control node in the case of a current mismatch due to the PFD's pulses. To remedy the possible I_{cp} fluctuations, high impedance cascode current sources were used. In some cases, the switching UP or DOWN pulses may result in extra charge injections, a sluggish response and further I_{cp} fluctuations (due to finite output impedances of current sources). To solve this problem, the charge pump's output node is buffered. This technique was not applied to this design for simplicity because the current topology sufficed. Finally, to keep the PFD's gain constant during charge/discharge of the loop filter, I_{cp} sources were designed to supply equal currents.

For proper functioning of the CP-PLL, the CP's output voltage should keep the current generator transistors in the saturation region. To achieve this, a very low impedance to ground (GND) or a dc rail is required. For a purely passive solution, the loop filter should have a GND-referenced capacitor. In this design, a second order passive filter network was used (Figure 7).

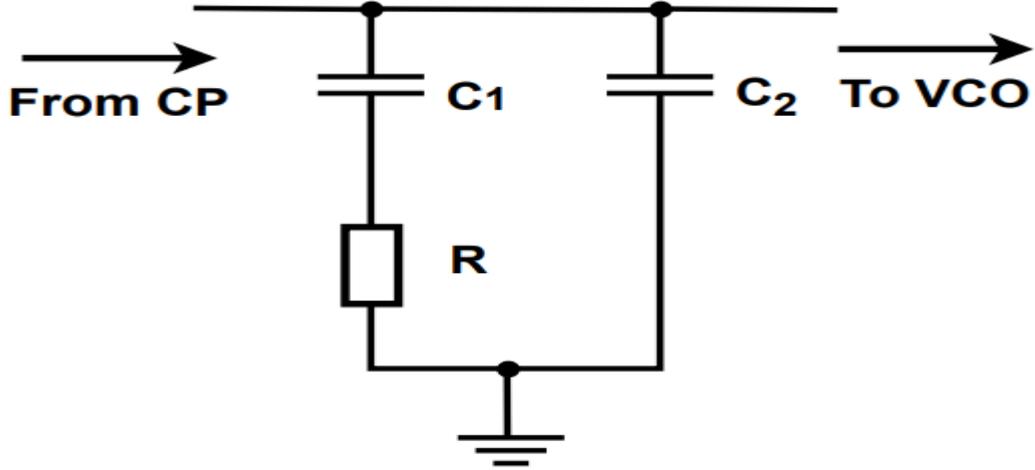


Fig. 7 Low Pass Loop Filter

The series RC arm dampens the resonance of the overall filter response without degrading the bypass effectiveness at high frequencies. The series resistor R introduces a zero in the LPF's transfer function which makes it possible to control the damping of the PLL HF response separately from its speed. On the other hand, the so-called secondary capacitor C_2 has a reduced effect on the loop's dynamics and as such is sometimes ignored in the mathematical modeling of the LPF behavior [27]. To determine the values of the LPF elements, the desired loop dynamics should be known or determined. This dynamic is studied in the form of the CP-PLL's natural frequency ω_n or the loop bandwidth ω_{3dB} . The ω_n of a CP-PLL, employing a passive LPF, is related to ω_{3dB} by

$$\omega_n = \frac{0.075\omega_{3dB}}{\left[2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}\right]^{0.5}} \quad (2)$$

where ζ is the damping factor ($\zeta \in [0.5, 2]$ for generally good dynamics). A good speed-stability compromise is usually achieved with $\zeta = 0.707$. To uphold the continuous time approximations of the CP-PLL's dynamics, ω_{3dB} should be at most a tenth of ω_{REF} . However, ω_{3dB} is preferred to be as wide as possible to aid suppression of the VCO's phase noise. A good noise-stability trade-off is to design ω_{3dB} to be 7.5% of ω_{REF} . Therefore, designing for $\zeta = 0.707$, ω_n becomes approximately 0.036 ω_{REF} . Designing for a 3 MHz resolution, ω_n was 0.69 Mrad/s. By setting I_{cp} , the values of C_1 and R , are found using Equations 3 and 4 respectively. Conventionally, the value of C_2 is chosen to be about 10% that of C_1 . This allows for reducing R values to reasonable levels. Furthermore, the setup requires a large dc blocking C_1 to avoid excessive dissipation of the unwanted ripple energy on R . Generally, a high I_{cp} is desirable for higher loop gain and hence a more stable CP-PLL. However, it produces a large C_1 requirement (Equation 3) which translates into large die areas. I_{cp} for this design was chosen as 25 μ A through a short calculative iteration for a decent loop gain and C_1

$$C_1 = \frac{K_{vco} I_{cp}}{\pi \omega^2 N} \quad (3)$$

$$R = \frac{2\zeta}{C_1\omega_n} \quad (4)$$

Therefore, the design values of the LPF elements were: $C_1 = 76.9$ pF, $C_2 = 7.5$ pF, and $R = 26.9$ k Ω . Finally, the fixed-ratio N-divider was designed. The $N = 32$ frequency divider was constructed as a chain of five power-of-2 integer dividers as illustrated in Figure 8.

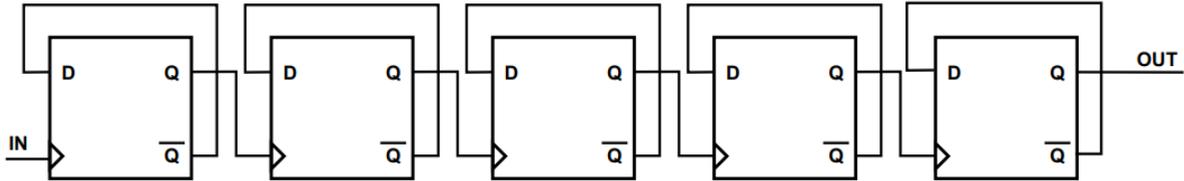


Fig. 8 $N = 32$ feedback divider

Each divider cell was an asynchronous binary counter created from a D-FF whose inverted output Q was tied to the data input D . The signal to be divided is fed to the clock input. The FFs were implemented using true single phase clocking latches for low power high speed operation. The topology required minimum sized transistor and hence, was also efficient in terms of die area.

BIST Paradigm

A fully digital charge-based frequency measurement BIST scheme was designed with focus on and embedded into the CP-PLL. The BIST strategy presented here is defect-oriented and an improved version of the scheme first presented in [28]. The test strategy is implemented with minimal hardware, requires fewer external signals, and is highly integrable. An all-digital architecture was chosen due to their well-known robustness [12]. The PLL-under-test (PUT) is subjected to testing by undertaking some fundamental checks. Although the BIST is defect-oriented, it takes advantage of component/system functionality and dynamics to achieve testing. The checks are:

A. *START sequence check:*

This check verifies that the PUT can be tuned up to frequency within a specified time from system startup. It also includes the demonstration of phase locking.

B. *Normal mode check:*

Here, checks ascertain if output signal produced by the PUT, post-lock, is of the desired or correct frequency. It also involves PUT reprogramming to effect and study the PUT response to dynamic frequency changes.

C. *Mode-switch check:*

This check establishes the ability of the PUT to be operated in and switched from its various operation modes: normal mode, system test mode, etc.

D. STOP sequence check:

This verifies that the PUT can be stopped when a specific sequence of signals is applied to the appropriate inputs. Together with the START sequence check, it can be demonstrated that the PUT would correctly cease and resume operation in tandem

The test strategy is conceptually straightforward. The scheme is initialized, and the PUT is exercised to stimulate all its blocks and register their interactions. The responses are collected in the form of frequency variations. That is, the PUT is charged from a very low frequency f_o towards a predetermined maximum frequency f_{max} threshold, preferably the top of the synthesizer’s tuning range. The final frequency attained is measured and compared to the known standard, f^* . The PUT is fault-free if $f_{max} = f^*$ (allowing a little error margin), otherwise the device is faulty. A similar process is carried out in the discharge phase of the PLL as a foolproof check. The test procedure occurs in five successive steps and is described as follows (Figure 9):

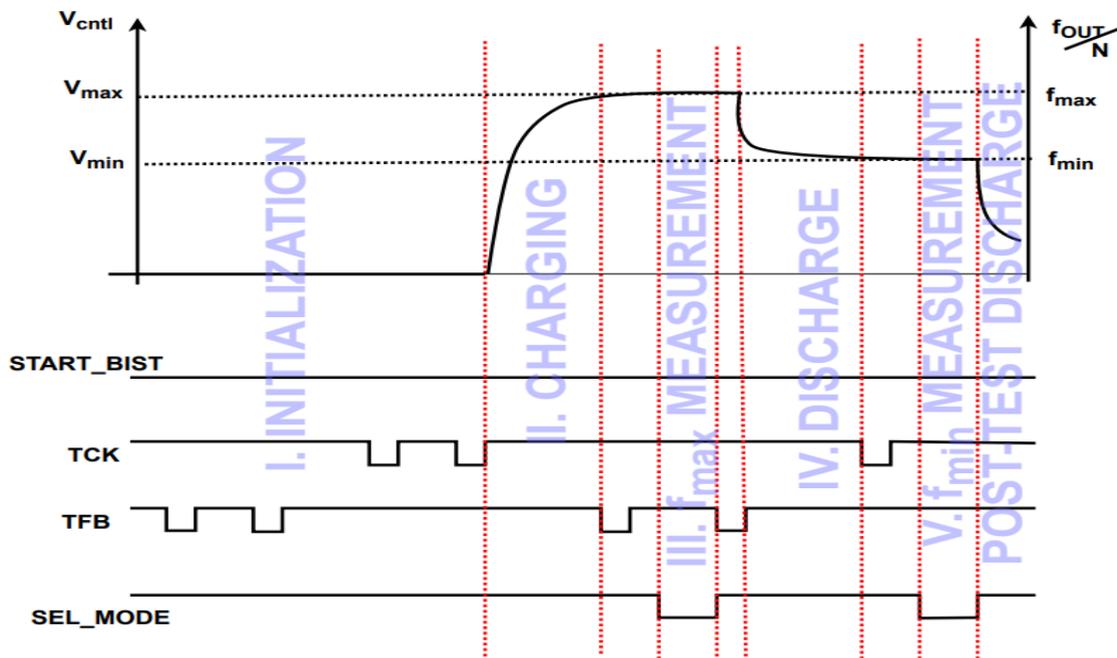


Fig. 9 A high-level abstraction of the BIST procedure and related test stimuli.

I. *Initialization and STOP sequence check:* This PUT undergoes an initial discharge phase where the device is brought to f_o to ensure that CP-integrator is drained, and the charge stage commences from a frequency as close to the minimum VCO output frequency f_{out} as possible. These ushers the PUT into a state where the output current is dc. If successful, this stage essentially stops the normal operation, establishing the STOP sequence check described above.

II. *Charge:*

In this stage, the PUT frequency is raised from f_o to f_{max} by a steady increase V_{ctrl} , an action which corresponds to the START sequence. The PUT’s frequency is held constant for a specified time afterwards to verify phase locking.

III. Measurement of f_{max} :

The value of the post-charge frequency is measured by employing a counter to register the number of cycles within a given time interval. The count value is then shifted out and compared to f^* . This frequency measurement constitutes the normal mode check.

IV. Discharge:

Here f_{out} is gradually decreased from to a predefined frequency f_{min} using by steadily decreasing V_{cntl} .

V. Measurement of f_{min} :

The obtained frequency after step IV is determined and studied using the same method as in step III. The access and control mechanism of the test is achieved by applying appropriate digital stimuli to specific PUT blocks. Some of the stimuli are generated internally while others are supplied via external pins. To start the test procedure, a *START_BIST* signal is used to switch from the PUT's normal operation mode to the test mode and back, post-test. A low (logic 0) on the *START_BIST* line triggers the BIST mode whereas a high (logic 1) selects the normal mode. To generate the waveforms for the charge and discharge test phases, we refer to the basic operational principle of the PLL as described in Section 1. That is, the PLL is a feedback control system which compares the feedback signal to reference and adjusts $f_{FBK} = \frac{f_{vco}}{N}$ to meet f_{REF} . Therefore, provided $f_{REF} < f_{FBK}$, the PLL remains in a continuous charge state. Conversely, the PLL is in a continuous discharge state if $f_{REF} > f_{FBK}$. Test stimuli were designed based on this concept to be fed to the PFD inputs which charges and discharges the PUT for specified periods. These BIST patterns are illustrated in Figure 9 alongside their related test phases. The lines *TCK* and *TFB* represent the test clock and test feedback signals respectively. Additionally, this version of BIST features a new signal *SEL_MODE* for controlling the state of the response analyzer. A transition on this line controls the state of the response analyzer. The three signals are generated by the built-in TSG.

VHF CP-PLL with BIST

To make the frequency synthesizer testable, the CP-PLL architecture was modified slightly by introducing a few extra hardware whilst maintaining the core circuitry intact. The modified CP-PLL structure is illustrated in Figure 11.

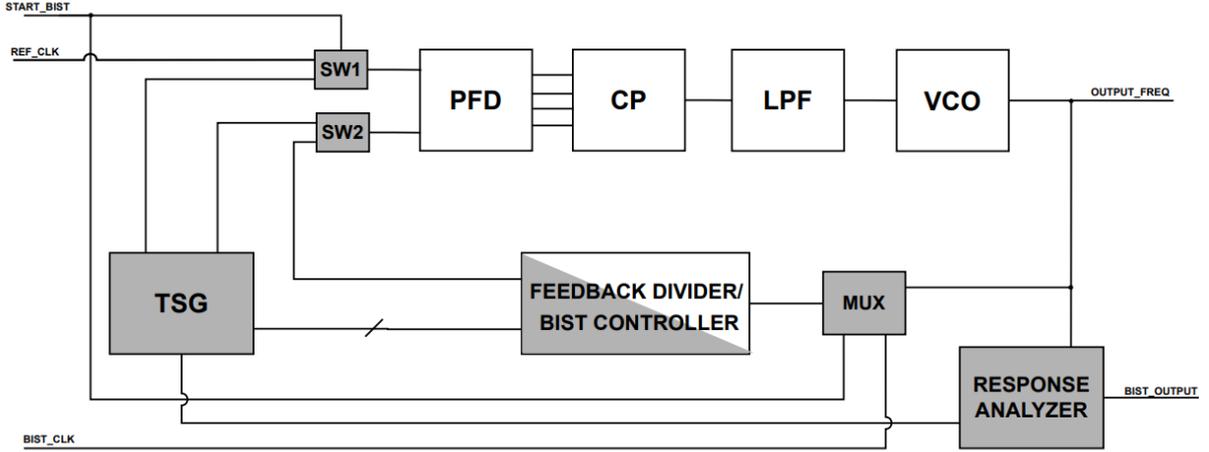


Fig. 11 Designed PLL with BIST.

Extra (digital) hardware introduced for the BIST integration include two identical 3-input switches, a 2×1 MUX, a response collector, and a TSG. The PLL’s feedback divider is repurposed as the BIST controller, hence the need for the MUX. Here, an additional D-FF stage is added as the BIST controller requires six asynchronous counter stages: A, B, C, D, E, and F. A state machine in the controller block manages the overall self-test procedure. The reference switch SW1 selects between the PLL’s reference clock (RCK) and the test clock (TCK) for the respective operational modes. Similarly, the feedback switch SW2 selects between the PLL’s feedback (RCK) and test feedback (TFB) signals respectfully. The two switches are connected to the PFD input and have a common $START_BIST$ input. For $START_BIST = X$, $RCK/FBK = Y$ and $TCK/TFB = Z$, the switch output is related to its inputs

$$TCK = AB\bar{D}\bar{E}F + ABC\bar{D}\bar{E}\bar{F} \quad (5)$$

$$TFB = AB\bar{D}\bar{E}\bar{F} + \bar{A}BDEF \quad (6)$$

$$SEL_MODE = B + E + F + C\bar{D} + \bar{C}D \quad (7)$$

as $XY + \bar{Z}$. This setup requires lesser number of gates (two 2-input NANDs) than a traditional 2×1 MUX, which also suffices for this function (with $START_BIST$ as the selector). This switching mechanism implies that the inverse of TCK/TFB is always supplied. The switching mechanism can only be used if it can be guaranteed that the circuit never enters the state: $START_BIS = 1$, $RCK/FBK = 0$, $TCK/TFB = 1$. The TSG is a combinational circuit which generates the test patterns based on the output of the controller, which operates on a 6.25 MHz test input clock. Since the controller generates $2^6 = 64$ unique states, one state per BIST clock cycle, each test runs for 10.24 μ s. The design of the TSG and hence the generated test waveforms were based on the following Boolean relations:

The $START_BIST$ signal remains low throughout the entire test run. As discussed in Section 1, classic response analyzers employ compaction. For a given test strategy, the functional CUT is first exercised through computer simulations or pre-tests to generate response sequences. These sequences are compacted and stored. During a BIST run, actual responses are compacted and then compared against the stored pattern for test evaluations. Although a practical solution for GHz range PLLs, the approach can be quite lossy and susceptible to aliasing. For relatively

lower frequency applications, the combination of a digital counter and shift register suffices as a response collector. In our test paradigm, the counter measures the frequency whereas the later shifts the result out. In this design, a simpler and lossless D-FF-based circuit that operates conjointly as both a counter and a shift register was used to reduce hardware cost (Figure 10).

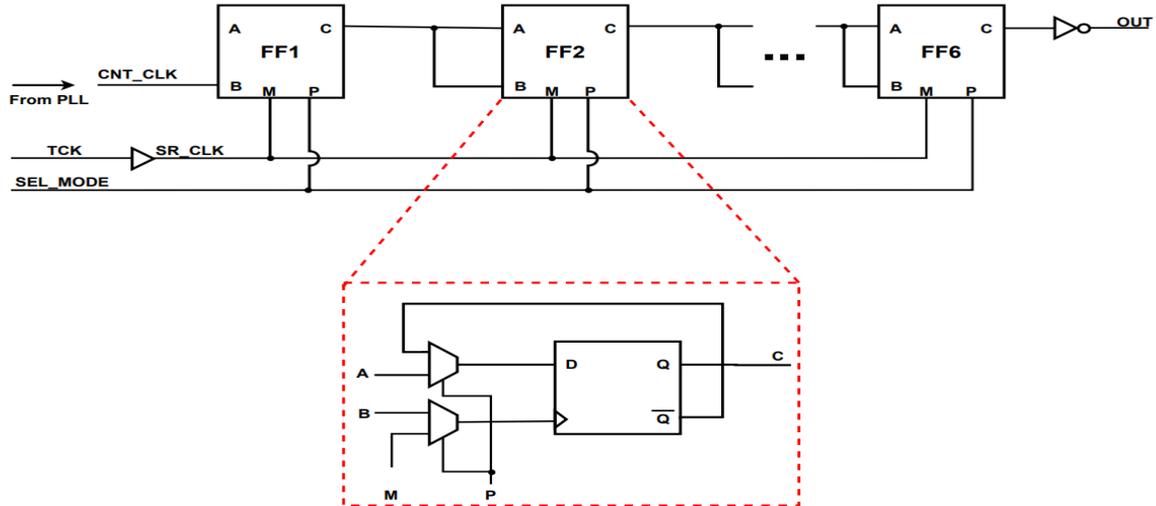


Fig. 10 Schematic of response collector.

The 6 FF network, which has a potential for wider fault coverage, exploits the inherent operability of FFs as counters or shift register, building both configurations into one device albeit separable using MUXs (Figure 10). Together, the 12 MUXs use the *SEL_MODE* line to select a given configuration (*SEL_MODE* = 0: counter, *SEL_MODE* = 1: shift register).

The collector is configured as a shift register during most of the test runtime. For each test cycle, the device switches configuration twice. First, all the FFs are reset low by tying the data input to VSS. During the measurement phase, the device switches to the 'count-mode' and holds for a predefined $0.32\mu\text{s}$ after which it reverts to serially shift out the result in 'shift-mode'. The delay element on the shift register's clock *SR_CLK* line is to remedy an inherent timing problem of the devices. This malfunction arises during the second configuration switch where the rising edges of the *SEL_MODE* and *SR_CLK* signal coincide since the two are ultimately fed from the same source. Here, the device is expected to operate as shift register even before *SEL_MODE* fully asserts. Thus, for the first cycle, the shift register does not function properly, leading to unpredictable results. Nonetheless, the device has a wide fault coverage potential and remains practical even for ultra-high frequency applications.

Results and Discussions

The proposed CP-PLL with built-in self-test was designed and tested in AMI 600 nm CMOS process technology using Cadence Design Environment. All building blocks of both PLL and BIST were verified through simulations

and the optimized circuits was laid out regarding good high frequency techniques. The entire design was then simulated post-layout to verify system-level functionality. The system was powered by ± 1.5 V supply rails.

The tuning sensitivity K_{vco} of the optimized VCO was calculated from a frequency sweep of its output against V_{cntl} as 302 Mrad/Vs using Equation 1 and a fine averaging of the effective region as described in Section 3.1.

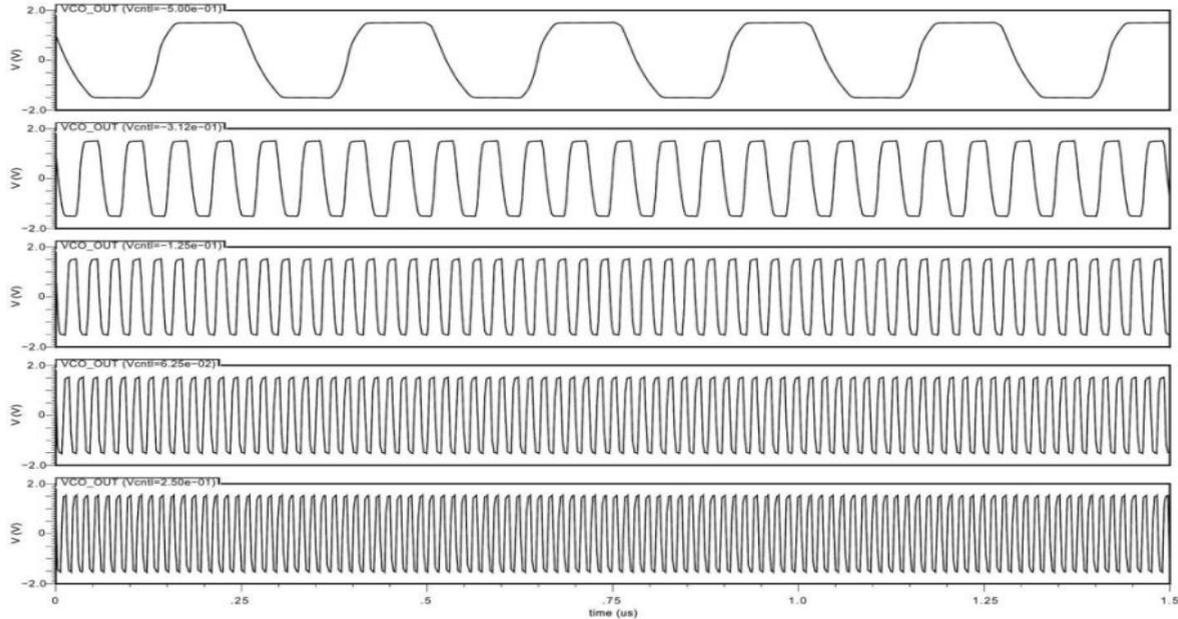


Fig. 12 Simulated VCO output at different V_{cntl} : -0.5 V, -0.312 V, -0.125 V, 0.0625 V, and 0.25 V (in order).

Figure 12 show the VCO outputs for five V_{cntl} values: -0.5 V, -0.321 V, -0.125 V, 0.0625 V, and 0.25 V. The short-term stability of the VCO was also determined in the form of the oscillator’s phase noise. The CP-PLL had a simulated phase noise of -71 dBc/Hz at 1 kHz and consumed 1.80 mW of power at full operation. To test the PFD, two ± 1.5 V square pulses A and B for the reference clock and the feedback signal respectively, were applied to the PFD input. Three distinct scenarios were studied:

- I. A and B are in-phase but have the different frequencies.
- II. A and B oscillate at the same frequency but are out-of-phase.
- III. A and B have the different frequencies and are out-of-phase.

For brevity, only case III’s results are shown in this paper. A case where the feedback has a higher frequency feedback signal with respect to A is simulated. For B’s frequency to match that of A, PFD must cause the VCO to adjust the feedback frequency downwards. It is seen in Figure 13 that the PFD generates *DOWN* pulses, which when fed to the charge pump, results in a discharge of the loop filter. The VCO control voltage V_{cntl} and the feedback signal’s frequency ultimately reduces. The PFD-CP-LPF blocks were simulated together to study the performances of the CP and loop filter, and to verify their interactions.

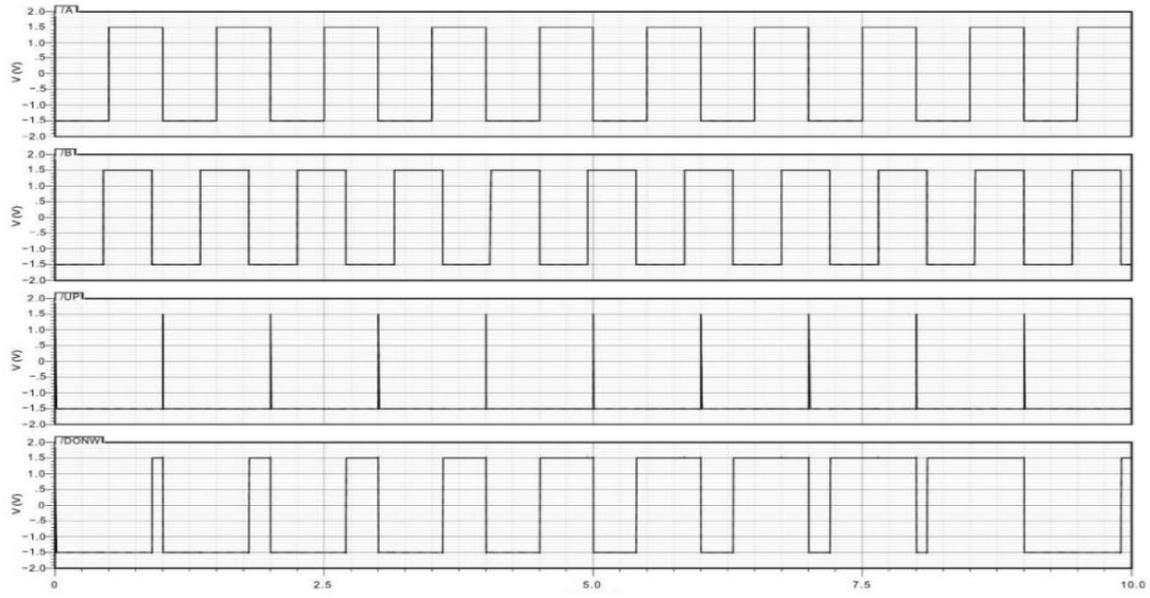


Fig. 13 Simulated PFD for case III

The average I_{cp} was measured over a relative long time for both charge and discharge phases of the loop filter. The CP pumped an average of $24.9 \mu A$ and drew $24.5 \mu A$ from the filter in the respective phases, as was expected from the design. On the other hand, the filter produced an output voltage that increased periodically provided the frequency of the feedback signal remain lower than the references. Plots capturing the PFD's input waveforms and the corresponding V_{cntl} output of the filter captured in a $10 \mu s$ window is shown in Figure 14.

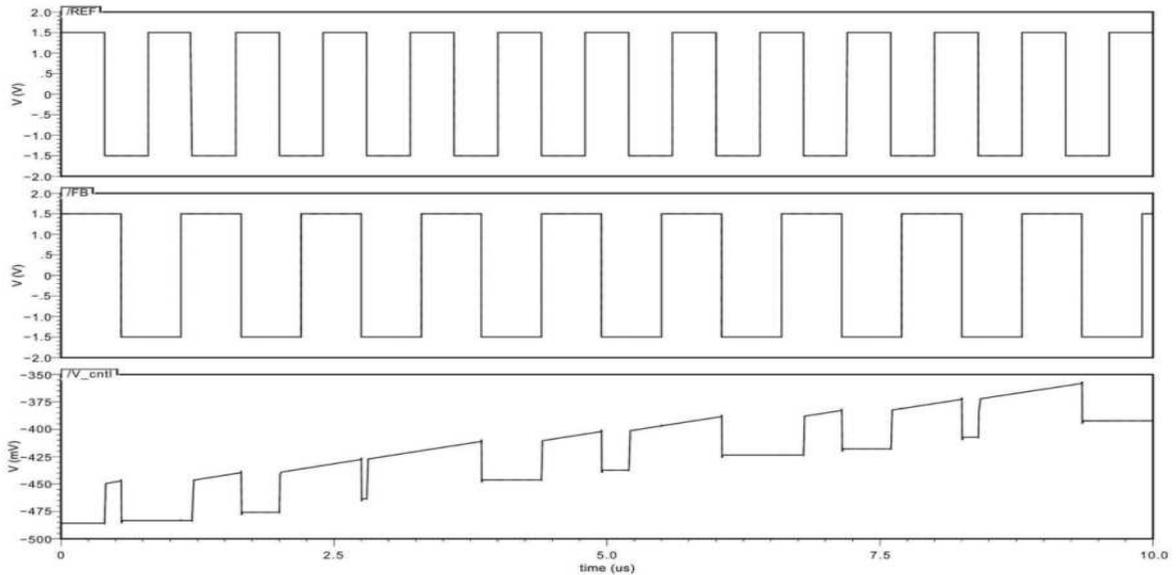


Fig. 14 V_{cntl} at loop filter output node and corresponding PFD inputs

The verification of the feedback divider was quite straightforward. A clock signal was applied to its input and the output of each of its five counter stages were measured to verify proper frequency division. Next, the CP-PLL was simulated to verify design correctness and proper operation. The PLL was used to synthesize five signals with frequencies sampled from the loop's operating range: $f_{out} = 40$ MHz, 55 MHz, 70 MHz, 85 MHz, and 100 MHz. Since the CPPLL uses a $N = 32$ divider: $f_{out}/32$ references. Figures 15 and 16 show the synthesis of the 40 MHz and 85 MHz signals.

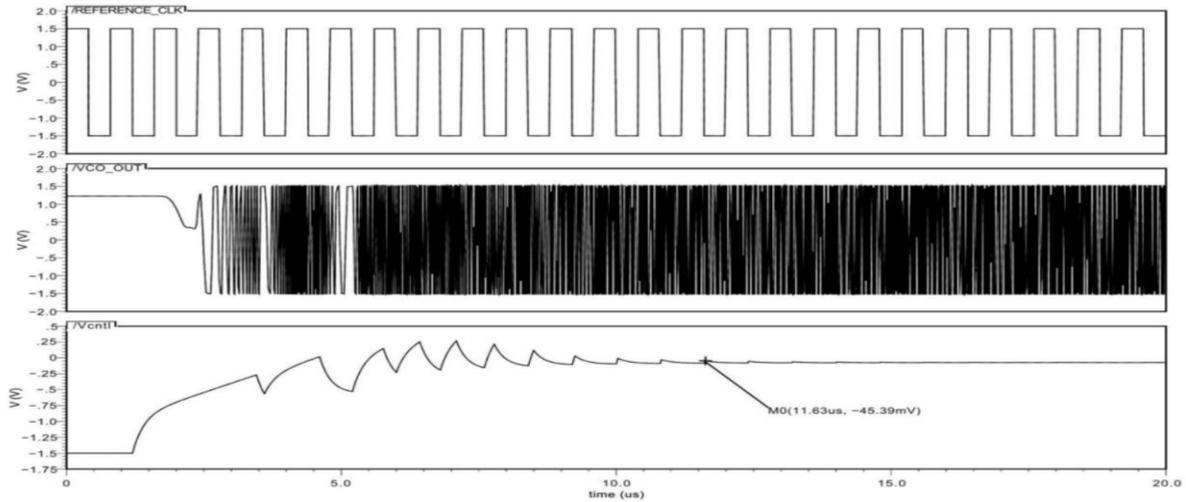


Fig. 15. A 40 MHz signal synthesized by CP-PLL from a 1.25 MHz reference

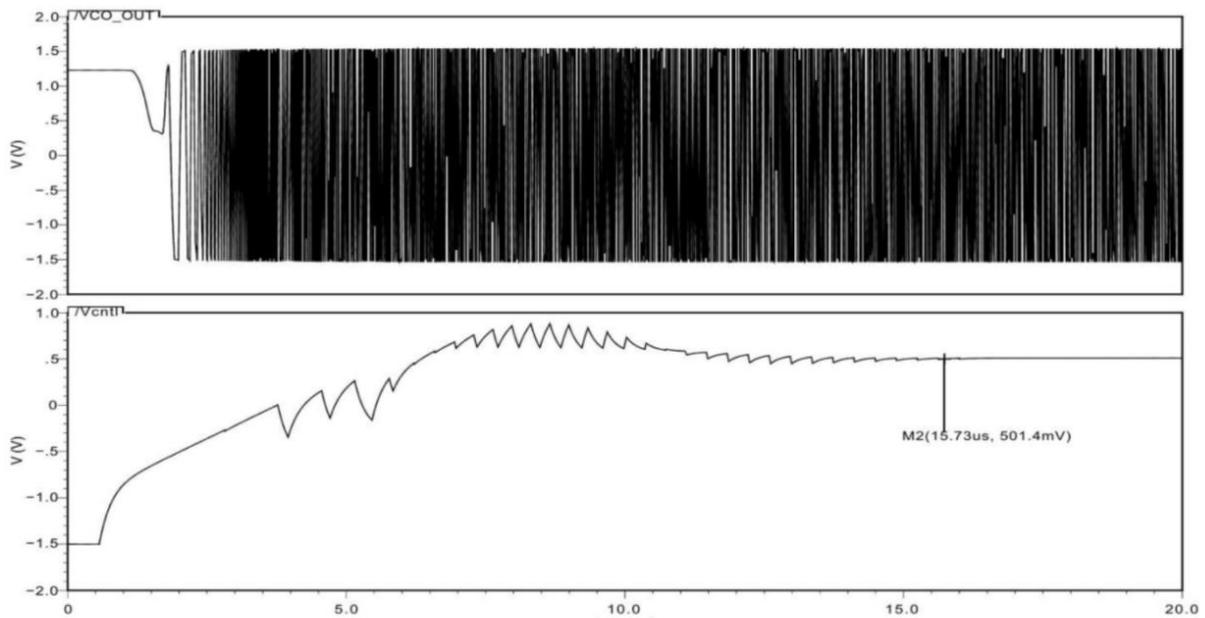


Fig. 16. An 85 MHz signal synthesized by the CP-PLL from a 2.66 MHz reference

The CP-PLL was able to generate the required f_{out} signals. For the 40 MHz case, the signal was acquired starting from under an initial 2 Hz frequency in 11.6 μ s. The acquisition times of all frequency locks are listed in Table 2

Table 2: Frequency syntheses and corresponding lock times

f_{out} [MHz]	f_{REF} [MHz]	Lock time [μ s]
40	1.25	11.6
55	1.72	12.2
70	2.18	10.9
85	2.66	15.7
100	3.25	25.1

Finally, the BIST hardware was checked, and fault simulations were conducted. We present the results from the TSG and the response analyzer only since the BIST controller is the same as the feedback divider while the remaining hardware are trivial. To test the TSG, the BIST controller was connected to a 6.25 MHz pulse source and the TSG output, alongside V_{cntl} and resulting f_{out} changes were observed for one test cycle. But for the exception of a few negligible glitches, the test stimuli generated were as expected. The counter/shift register operation was also verified. Simulations revealed that the BIST circuitry can generate the exact patterns of required test stimuli. It also performs all the unique checks of the strategy efficiently. The final test output is very consistent and produces the same results for a few different runs of the simulation. The overall check of the BIST scheme is summarized in Figure 17.

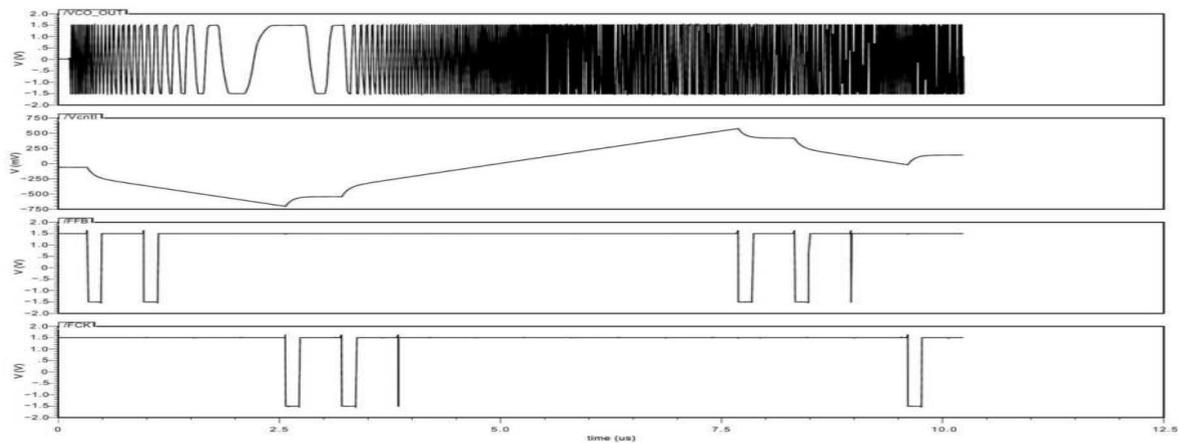


Fig. 17 Simulation results of BIST scheme

The PUT charges to $f_{max} \approx 84$ MHz. Then, there is a 0.48 μ s hold state where the f_{max} measurement is taken. The loop discharges to $f_{min} \approx 74$ MHz and f_{min} is measured in the next hold state. Consistent 011010 (26 decimal) and 010111 (23 decimal) values corresponding to f_{max} and f_{min} were obtained respectively for different test runs. Since

the response analyzer counts in a $0.32 \mu\text{s}$ time window, the measured outputs correspond to $f_{max} = \frac{26}{0.32} = 81.3 \text{ MHz}$ and $f_{min} = \frac{23}{0.32} = 71.8 \text{ MHz}$. With a tolerable error margin, the designed and simulated CP-PLL can be declared fault-free. Transistor level fault models developed in [28] were also used for both digital and analog components during simulations. These included transistor stuck-on, source open, drain open, gate-to-source short and gate-to-drain short faults. The described BIST scheme was very effective in detecting faults. Of simulated 316 faults simulated, only 8 remained undetected. All 8 undetected faults were found to be redundant.

Figure 18 shows the final layout of the CP-PLL with BIST in one IC. The BIST area overhead was estimated to be between 10% and 15%.

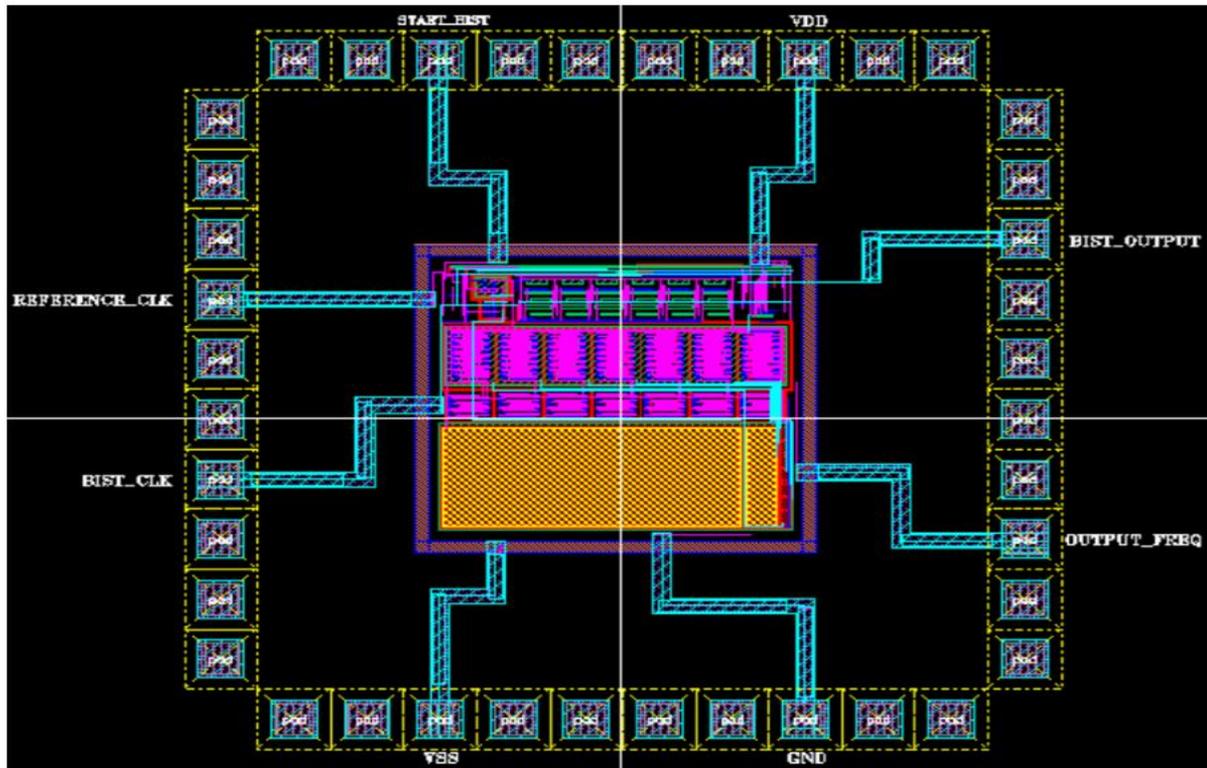


Fig. 18 Layout of CP-PLL with BIST in 600 nm CMOS

Conclusions

In this paper, the design of a VHF CP-PLL with built-in self-test has been presented. The PLL is implemented as a frequency synthesizer with a 40 MHz - 100 MHz tuning range. The building blocks of the PLL core as well as that of the embedded defect-oriented test scheme were designed and tested through simulations in 600 nm CMOS using the Cadence Design Environment. Experiments showed good synthesis of various frequencies within the

loop's operating range. The generated signals are obtained at the exact frequencies, have clean waveforms with no spikes/glitches whatsoever, and are acquired within reasonably short lock times. The CP-PLL exhibited a phase noise of -132 dBc/Hz at 1 MHz and with a 3 V supply, consumed 1.8 mW.

The designed BIST is a fully digital architecture with an output which can be read serially on a single pin. The simple digital output allows for a seamless interfacing of the test process with standard ATEs and makes it easier to integrate the final IC into larger electronic hardware. The design also features a very simple yet effective response collector on the BIST output which uses dynamic FFs for fast, lossless, and aliasing-free compaction of test results. The overhead posed by the BIST hardware was also kept minimal for practical and low defect-risk integration. Fault simulations revealed very high fault coverage for the BIST scheme, with most undetected faults being redundant. The implemented test scheme was designed to be as generic as possible and is easily portable across similar PLL architectures and technology nodes without requiring significant reconfiguration.

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List of Abbreviations

CP	charge pump
PLL	phase lock loop
VHF	very high frequency
BIST	built-in self-test
CMOS	complementary metal oxide semiconductor
VCO	voltage-controlled oscillator
PFD	phase frequency detector
PUT	pll under test
ATE	automated test equipment
TSG	test stimulus generator
CUT	circuit under test
ROM	read only memory
LFSR	linear feedback shift register
MISR	multiple input shift register
IC	integrated circuit
MEMS	micro-electro-mechanical system
VLSI	very large-scale integration
DFT	design for test

Availability of data and material

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study

Competing interests

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Authors' contributions

BK – idea, proposed design, and specifications and test and evaluation, read and approved final manuscript

EOA – Simulations and Verification, read and approved final manuscript

JY – idea, introduction, and experimental strategies, read and approved final manuscript

ASA – Experimental set ups, read and approved final manuscript

ETT – coordinator, abstract and conclusion, read and approved final manuscript

BYA – related works, drawings, read and approved final manuscript

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