Beyond 10 MHz Organic Electrochemical Transistors for Printed Multi-valued Logic Circuits

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Beyond 10 MHz Organic Electrochemical Transistors for Printed Multi-valued Logic Circuits

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ABSTRACT

Printable electronics requires solution-processable transistors that can perform high-speed operations with high gains, with which its applicability can embrace bio-interfacing, neuromorphic computing, and even high-functioning logical circuitry. Although organic electrochemical transistors (OECTs) with superior transconductance and biocompatibility have emerged as feasible candidates, the intrinsic coupling between ionic and electronic carriers leads to limited response times falling behind other transistor technologies. Here, we overcome such limitations by introducing a vertically stacked dual-channel architecture enabling an unprecedentedly high operation speed with multiple logic states. Specifically, a simple implementation of dual-ion penetration mechanisms allows facile manifestations of stable and equiprobable ternary logic states, to which state-of-the-art accessing frequency over 10 MHz is realized. Furthermore, printed arrays of ternary logic gates with full voltage swing within 1 V is demonstrated.

Keywords: electrochemical transistor, multivalued transistor, ternary logic, ion penetration, vertical transistor

INTRODUCTION

The emergence of organic electrochemical transistors (OECTs)^[1-3] has ushered in a new era of organic semiconductor-based printable electronics technology^[4], including biocompatible electronics^[5-7], conformable sensors^[8-10], and neuromorphic devices^[11-13]. The principle operating mechanism of OECTs, pertaining to direct ionic penetration in the channel layer, can help the system achieve a doping-induced high carrier concentration, leading to an exceptionally high transconductance that is desirable for various advanced applications^[14,15]. Furthermore, the use of ionic and electronic conduction allows such frameworks to be susceptible to various chemical environments, which can enable the use of such devices as chemical and biological sensors with a high efficacy^[16,17]. However, control of the ionic conduction during operation may induce adverse effects associated with the sluggish response of such devices to external electric fields, leading to the chronically low operation speed of OECT devices. Several researchers have attempted to develop novel materials and device geometries to mitigate the fundamental issues involving ionic movements^[18]. For example, certain novel electrolyte materials have demonstrated the potential of facilitating ionic rotation and infiltration in the semiconductor films, thereby enhancing the response time^[19]. Moreover, modification of the device geometry to achieve a more favorable dimensionality for ionic movement can help enhance the operating speed of OECTs. Using these methods, the fastest OECT with a -3 dB cut-off frequency ($f_{-3\text{dB}}$) of 380 kHz was developed in 2019 by using internal ion-gated organic electrochemical transistors (IGTs)^[8]. Although this operation speed is comparable to or even superior than that of other emerging organic transistor technologies, there remains scope for improvement. Notably, the RC time constant of an OECT ($t_{\text{RC}} = lC/\sigma_{\text{ion}}$) including an electrolyte with a common ion conductivity of $\sigma_{\text{ion}} = \sim 10^{-2}$ S/cm and a double layer with a specific capacitance of $C = \sim 10^{-5}$ F/cm², can reach up to 10 MHz when the gate distance (l) is scaled down to 1 μm ^[20]. However, owing to the liquid or gel-like nature of electrolytes and widespread use of bulky Ag/AgCl reference electrodes, achieving a scaled-down geometry of the devices is challenging, which is a bottleneck to realizing the theoretical speed.

Furthermore, the low operation speed and bulky geometry limit the applicability of OECTs in a broader range of printable electronics. In particular, conventional OECTs cannot be practically implemented in logical circuitry, which represents the fundamental application of transistors. Owing to the difficulty in realizing complex logic configurations and achieving the desirable response time in OECTs, the required level of the signal processing cannot be achieved for even coarse bioelectronic computing applications such as bio-interfacing. Consequently, the application of OECTs to more advanced logic components such as multivalued logic transistors (MVTs)^[21-24], a key direction of the More-than-Moore era^[25], has not been considered despite the foreseeable synergetic advantages. For example, owing to the limited material selection associated with restricted operating principles such as band-to-band tunneling, it is difficult to realize stable, tunable, and distinctive multistate electrical characteristics in conventional MVT technology. In contrast, in OECTs, the manifestation of intermediate electrical states can potentially be achieved by the physical presence of multiple electrochemical states, which are broadly tunable through the chemical versatility of organic materials^[26-30]. In particular, the use of multivalued logic architecture in OECTs can fundamentally enhance the level of

integration for OECT-based logic operations, which cannot be realized using conventional binary logic OECTs. Hence, by overcoming the chronic disadvantage of low driving speed of OECTs, the scope of applicability of such frameworks can be expanded, and devices with a broader material diversity can be established from the perspective of MVTs.

In this Article, we report a novel rational design of high-speed multivalued logic OECTs based on a vertically stacked dual-channel architecture, which can demonstrate a state-of-the-art operation frequency of more than 10 MHz. Simple consecutive deposition of widely used electrochemical materials, poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) and poly(3-hexylthiophene-2,5-diyl) (P3HT), was employed to construct the vertical channel layers of a dual-channel OECT (DuECT), which were then sequentially penetrated and doped by electrolyte ions by gradually increasing the gate voltage. In this manner, a cascade onset behavior in the electrical conductivity was induced, consisting of multiple distinctive and stable logic states. The short channel length of the vertical structure and high polarizability of large ions in the proposed architecture enabled an unprecedentedly high speed for accessing each of the logic states, and thus, a record-high f_{-3dB} value of 10 MHz in the field of OECTs was achieved. Furthermore, through moderate chemical modifications, the altered oxidation potential of PEDOT:PSS could directly modulate the gate driving voltages of DuECTs, thereby providing a facile route for electrical optimization. Based on the optimized DuECTs, an array of printable ternary logic circuits with a high operating speed and low driving voltage (< 1 V) was demonstrated.

RESULTS

Fig. 1A schematically illustrates the DuECT architecture. Patterned metal electrodes (Au or Cr/Au) are used as the drain electrode and contact pad. A consecutively solution-deposited P3HT/PEDOT:PSS heterostructure serves as the dual channel. Part of the PEDOT:PSS layer that is not covered by the ion gel functions as both the channel and source electrode. The ion gel is used as the electrolyte for redox reactions as well as the dielectric-forming electric double layer. Spray-coated and patterned solid-state Ag/AgCl (**Fig. S1**) is employed as the gate electrode of the DuECT and reference electrode for the electrochemical reaction. This Ag/AgCl framework exhibits functionalities comparable to those of conventional bulky aqueous reference electrodes (**Fig. S2**). In addition, the use of solid-state Ag/AgCl electrodes considerably decreases the operating window of the P3HT channel compared to that of the common metal gate electrodes (**Fig. S3**). The fabrication of DuECT is schematically illustrated in **Fig. S4**. The ionic and charge conduction mechanisms within the DuECT architectures and the characteristic electrical behaviors are shown in **Figs. 1B** and **1C**. When a low gate voltage is applied (top panel of **Fig. 1B**, $V_G = 0-0.5$ V), anions gradually migrate out of the P3HT channel, leading to a conductivity loss. Within this voltage range, the increased resistance of the P3HT channel determines the off-current level of a DuECT, thereby forming a constant intermediate logic state. As the gate voltage increases (bottom panel of **Fig. 1B**, $V_G = 1$ V), the reduction of PEDOT:PSS by penetrated cations leads to a secondary loss of the conductivity, constituting the complete off-state of a DuECT. The semi-logarithmic transfer curve of the actual DuECT (**Fig. 1C**) shows the expected three-state characteristics, with

a distinct intermediate logic state at $V_G = 0.45$ V ($I_D = 2.1$ μ A). This simple consecutive driving mechanism can allow high current levels even at low driving voltages, and the small penetration distances of vertical channels can enable fast responses. Moreover, the use of solid-state patterned Ag/AgCl electrode along with the facile solution processability of the device architecture can enable the scaled-down fabrication of devices and their arrays. The completed DuECTs exhibited a remarkably high performance in terms of the switching speed and transconductance, even in the scaled-down array framework (**Fig. 1D**).

We compare the performance of the proposed device to those of existing devices, as shown in **Fig. 1E** and **1F**. Notably, the operation frequency of DuECT can reach up 10 MHz (**Fig. 1E**), far surpassing what the research community perceived as the empirical upper limit of OECTs. The reason for this speed can be understood quantitatively from geometrical and materials perspectives^[20]. Specifically, the switching time (t_s) of a transistor can be expressed as $t_s = L^2/\mu V_D$ where L , μ , and V_D represent the channel length, electrical mobility of charge carriers, and drain voltage, respectively. The proposed geometry can achieve a switching speed of less than 1 ns. Moreover, the polarization time of the electrolyte, represented as t_{RC} , considerably influences the operation speed in OECTs. For DuECTs, C is $\sim 10^{-5}$ F/cm², and σ_{ion} is ~ 0.01 S/cm. Although the thickness of the electrolyte layer in the coplanar structure is 200 μ m, l can be assumed to be the shortest required ion penetration depth (~ 120 nm). Based on these estimations, the polarization time can be calculated to be within the range of 20 μ s to 12 ns. In practice, the cut-off frequency of DuECT is 10 MHz, whereas its transit frequency is considerably higher (the extension of the bode plot allows ~ 100 MHz), which are well within the range of theoretical expectations. Notably, the attained speed is higher than that of the existing OECT frameworks and represents state-of-the-art performance among all existing organic transistors. The frequency of DuECT approaches the theoretical limitation of OECT, corresponding to the characteristics of conventional materials. It is thus expected that the frequency can be further enhanced with material innovation. The first breakthrough point marked in **Fig. 1E** is identified based on this interpretation.

Furthermore, the DuECT achieves an excellent transconductance, which is of significance in the field of MVTs. Because OECT devices usually exhibit a high transconductance regardless of the composition of organic channels, they exhibit high normalized current levels comparable to those of other devices based on Si or graphene channels. For three-terminal devices, the correlation between the current level and gate voltage is shown in **Fig. 1F**. To enable a fair comparison, the current level of the intermediate logic state is normalized by the gate voltage. The values are measured based on peak currents in negative differential transconductance (NDT) devices and negative differential resistance (NDR) devices and inverter characteristics in graphene devices owing to the lack of off-states in such devices. Compared to organic devices, DuECT exhibits an enhanced performance, reaching a record-high value similar to that of a Si-based device. Therefore, the use of OECT for multivalued logic operation exhibits clear advantages over existing MVT technologies, which can be attributed to the capability of solution processing and large-area fabrication with minimal performance trade-offs and superior transconductance of intermediate logic states.

In general, to construct MVT-based logic gates with a stable intermediate state, the intermediate state of the transistor must be distinct from both sides of the on-current and off-current, and its gate voltage range

must be equiprobably assured. To this end, the intermediate states must be tunable, by either geometrical or chemical modulations. In the transfer characteristics of DuECT, the intermediate state is essentially the off-state of P3HT, the current level of which depends primarily on the thickness of P3HT in the vertical transistor accordingly to the operating principles mentioned previously. The linear transfer curves of DuECTs with different P3HT thickness values are shown in **Figs. 2A** and **S10**. As the thickness increases, the intermediate states occur at 42.6 μA , 2.15 μA , and 0.016 μA (**Fig. 2B**), with gradually reduced ranges of V_G for intermediate states (V_M) owing to the increased required voltage for turning-off thicker P3HT channels. The on-off current ratios of the on-intermediate state transitions and intermediate-off state transitions are shown on the bottom panel of **Fig. 2B**. To design an ideal ternary inverter, the current gap must be at least 10 times different for each side. Hence, the device performance achieved with a 23.7 nm thick P3HT layer, which corresponds to a current ratio of more than 100 for both sides, is within reasonable expectations.

In addition to the intermediate state optimization, the driving voltage ranges of a logic transistor must be controlled to construct advanced logic circuits. In particular, when high-level logic gates require the output voltage to be applied as the input voltage, it is necessary for a transistor to operate on the same range of drain and gate voltages. However, conventional OECTs, which frequently use PEDOT:PSS as the channel material, cannot easily achieve a symmetric driving range because the turn on voltage (V_{ON}) follows the electrochemical potential (sum of V_D and V_G). To address this problem, we introduce moderate chemical modifications in PEDOT:PSS^[31-33] to fine-tune the electrochemical potentials (chemical structures and corresponding oxidation potentials estimated from cyclic voltammetry are shown in **Figs. S12** and **S14**, respectively)^[34]. By using these PEDOT:PSS derivatives, V_{ON} can be gradually decreased from 1.66 V to 1.20 V (**Fig. 2C**), which is well within the range of operating V_D . **Fig. 2D** shows the comparison between the turn-on voltages estimated from the electrochemical potentials of PEDOT:PSS derivatives (Calculation details are presented in **Appendix S1**) and transfer characteristics of actual DuECT devices based on PEDOT:PSS derivatives at V_D of 1 V. The driving voltage can be easily tuned via the chemical modifications of PEDOT:PSS, which provides another basis for the application of OECT to logical circuitry. Furthermore, the lateral physical dimensionality of the DuECT can be modulated to further optimize V_{ON} . To confirm this hypothesis, the ion penetrating pathway is modeled, and the resultant voltage distributions are theoretically estimated (**Fig. 3A**) depending on the lateral dimensions by simultaneously solving continuity equations, 1D drift–diffusion equations and Poisson equations with fixed potential boundary conditions at the interfaces (Calculation details are presented in **Appendix S2**)^[22]. The lateral dimension is assumed to be dominant in the ionic conduction behavior, considering the thickness of the percolation path (12.8 nm) of the P3HT layers. Based on the starting potential for oxidation (0.89 V), the distance-dependent interface potential at a drain voltage of 1 V is used to estimate the changes in V_{ON} (**Fig. 3B**). The area-dependent transfer curves in **Fig. 3C** clearly indicate that larger lateral dimensions lead to increased V_{ON} , which is consistent with the theoretical estimations. Therefore, the DuECT architecture and its diffusion-limited operating mechanism can promote the scalability of logic gate fabrication.

Finally, we evaluate the speed to access the multiple logic states and applicability to logic gate construction. Because the vertical ion penetration pathway can alleviate the limitation of low ionic transport speed in OEECTs, it is reasonable to expect a significant improvement in the response time of DuECTs. **Fig. 3D** shows that the transient response (τ) of DuECT to a V_G pulse is 125 ns and 110 ns for on-off and off-on transitions, respectively. The operating speed can also be acquired from a bode-plot (**Fig. 3E**). f_{3dB} can be noted to be exceptionally high, with a value of more than 10 MHz (transient response of each frequency is shown in **Fig. S18**). According to the literature survey, f_{3dB} of 10 MHz is the highest value ever reported in the field of OEECTs and surpasses even the empirical upper limits. In addition to the geometrical advantage of the vertical architecture, the rapid driving can be attributed to the high polarizability of large ions in ionic liquids. As shown in **Fig. S19**, the cut-off frequency of a DuECT without patterned P3HT can reach a similar value with a slight discrepancy owing to the lack of direct penetration into PEDOT:PSS layers.

The results demonstrate that the DuECT exhibits facile tunability of multistate electrical characteristics, superior transconductance, and operating speed beyond empirical limits. Thus, the performance of this framework as a printed multivalued logic gate and corresponding arrays is evaluated. The most basic structure of these circuits is a NOT gate (i.e., an inverter). **Fig. 4A** shows a ternary inverter composed of DuECT. The turn-on voltage of DuECT in the inverter differs from that of a single transistor because of the application of the gate electrochemical potential. The gate electrochemical potential is the sum of the gate voltage and drain voltage, and thus, the resistance in a circuit decreases the drain voltage applied to the channel. Therefore, the current-drop-point (first V_{ON}) in an inverter occurs earlier than that in a single transistor. Hence, the intermediate state occurs at a gate voltage of less than 0.45 V (**Fig. 4A**, gray plot), consistent with the experimental results. The overall inverter exhibits a quasi-symmetric input–output voltage transfer curve (VTC) with a low driving voltage of less than 1 V. These symmetric inverter performances are close to ideal for the application of such devices to more complex logic circuits (i.e., XOR or LATCH) in which the output voltage is re-applied as the input voltage. The proposed multistate inverter exhibits gain values of 3.2 and 3.4 at a V_{DD} of 1 V, as shown in **Fig. 4B**. The gain value is close to zero between two peaks, which indicates that the intermediate state is rationally flat. The archetypal stability of an inverter can be evaluated considering the static noise margin in symmetric in-out VTC (**Fig. S22**). Furthermore, because the inverter with a stable intermediate state must be able to realize continuous ternary logic circuits, the dynamic switching property of the ternary inverter is demonstrated (**Fig. S23**). Finally, NMIN and NMAX logic gates (equivalent to NAND and NOR in binary logic circuits, respectively) are fabricated. The logic circuit diagram and corresponding optical microscopy images of the actual gates are presented in **Figs. 4C** and **4D**. Moreover, the temporal responses of the NMIN and NMAX logic gates under application of two input voltages ($V_{IN,A}$ and $V_{IN,B}$) are shown in **Fig. 4E**.

CONCLUSION

An unprecedentedly fast printable multivalued logic OEECT array with high on-off ratios and explicit intermediate logic states was realized. Two widely used electrochemical materials, PEDOT:PSS and P3HT,

were consecutively deposited to construct a vertical dual-channel architecture, enabling the manifestation of multiple distinctive logic states and high accessing speeds to each of the states. Specifically, as the gate bias was gradually increased, the thin P3HT top-layer exhibited the first turn-off behavior, followed by the secondary turn-off owing to the reduction of the PEDOT:PSS layer. Moderate chemical modulations of the oxidation potentials of PEDOT:PSS were implemented to demonstrate the tunability of intermediate states, i.e., voltage, current level, and on-off ratios in DuECTs. These modifications helped decrease the gate driving range from 1.66 V to 1.20 V at a drain voltage of 1 V. The feasibility of fine adjustments for the height and flatness of the intermediate state was demonstrated by the optimization of the device dimensionalities. In this manner, a low-voltage electrochemical MVT with high on-off ratios ($>10^2$) for each consecutive logic state was realized, with the capability of achieving f_{3dB} of 10 MHz, which represents state-of-the-art performance in the field of OECTs. The facile tunability for multiple logic states and superior operating speed demonstrate the feasibility of using the proposed OECT for logic circuitry, as highlighted by the stable operation of ternary NOT, NMIN and NMAX gates. The proposed vertical dual-channel ECT architecture and its remarkable properties as an MVT can provide a novel platform for harnessing the full potential of OECT and MVT technologies, thereby helping realizing breakthroughs toward the upcoming era of More-than-Moore electronics.

METHODS

Details of the experimental methods and calculation are presented in the Supplementary Information.

DATA AVAILABILITY

All the data generated or analyzed during this study are included in this published article and corresponding Supplementary Information.

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AUTHOR CONTRIBUTIONS

J.H.C. and D.U.L conceived the idea and initiated the project. D.U.L performed the fabrication and characterization of materials and devices. D.U.L and S.B.J conducted the physical analyses and wrote the manuscript. S.B.J and J.H.C. supervised the project. All the authors read and commented on the manuscript.

CONFLICT OF INTEREST

The authors declare no competing interests.

Fig. 1. Structure and properties of DuECT. (A) Schematic of DuECT with P3HT-PEDOT:PSS vertically stacked channels. (B) Penetration pathways of cations through DuECT channels. (C) Transfer characteristics of the DuECT (black line) and each subcell (red and blue dashed lines) in semi-logarithmic scales. (D) Photograph and optical image of the DuECT array on a glass substrate. Comparison of (E) operation frequencies and (F) scaled current levels of intermediate logic states of DuECTs to those of existing devices (blue and red stars pertain to patterned DuECT and P3HT-unpatterned DuECT, respectively). Configurations of the existing devices considered in (E) and (F) are summarized in Tables S1 and S2.

Fig. 2. Channel-dependent electrical characteristics of DuECTs. (A) Transfer characteristics of DuECTs in linear current scale. (B) Electrical characteristics of intermediate logic states of DuECTs depending on the thickness of the PEDOT:PSS channel. (C) Transfer characteristics and inverse of subthreshold swing in DuECTs based on oxidation-potential-modulated PEDOT:PSS channel layers. (D) Comparison between theoretical and empirical values of the turn-on voltages for intermediate logic states depending on the oxidation potential of PEDOT:PSS channel layers.

Fig. 3. Geometry-dependent electrical characteristics of DuECTs. (A) Schematic of ion penetration pathways in DuECTs. (B) Numerical estimations of potentials in dual-channel of DuECT (left side) and turn-on voltages at a drain voltage of 1 V (green bar, right side). (C) Transfer characteristics of DuECTs depending on electrode-covered-channel-area. (D) Temporal response of DuECTs (black, left) to a gate voltage pulse of 1 V (blue, right). (E) Current mode plot of DuECT operating at $V_D = 1$ V and $V_G = 1$ V.

Fig. 4. Printed ternary logic circuits based on DuECTs. (A) Simulated and measured voltage transfer characteristics, and (B) signal gains of DuECT-based ternary inverter. Logic circuit diagram and photographs of (C) NMN and (D) NMAX gates based on DuECTs. (E) Output voltages of NMN and NMAX gates with varying input voltages.

Supplementary Files

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