Double-Gate Operation of Metal Nanodot-Array-Based Single-Electron Device

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Abstract

Multidot single-electron devices (SEDs) can realize new types of computing technologies, such as reconfigurable and reservoir computing. The self-assembled metal nanodot-array film attached with multiple gates is a candidate for use in such SEDs to achieve high functionality. However, the single-electron properties of such a film have not yet been investigated in use with optimally controlled multiple gates because of structural complexity having many nanodots. In this study, Fe nanodot-array-based double-gate SEDs were fabricated and their single-electron properties modulated by the top- and bottom-gate voltages (VT and VB, respectively) were investigated. As reported in our previous study, the drain current (ID) exhibited clear oscillations against VB (i.e., Coulomb blockade oscillation) in a part of the devices, originating from a single dot among several dots. The phase of the Coulomb blockade oscillation systematically shifted with VT, indicating that the charge state of the single dot was clearly controlled by both the gate voltages despite the multidot structure and the metal multidot SED has potential for logic-gate operation. The top and bottom gates affected the electronic state of the dot unevenly owing to the geometrical effect caused by the dot shape and size of the surrounding dots.

Introduction

Multidot single-electron devices (SEDs) can realize new types of computing technologies, such as reconfigurable and reservoir computing. The self-assembled metal nanodot-array film attached with multiple gates is a candidate for use in such SEDs to achieve high functionality. However, the single-electron properties of such a film have not yet been investigated in use with optimally controlled multiple gates because of structural complexity having many nanodots. In this study, Fe nanodot-array-based double-gate SEDs were fabricated and their single-electron properties modulated by the top- and bottom-gate voltages (V_T and V_B, respectively) were investigated. As reported in our previous study, the drain current (I_D) exhibited clear oscillations against V_B (i.e., Coulomb blockade oscillation) in a part of the devices, originating from a single dot among several dots. The phase of the Coulomb blockade oscillation systematically shifted with V_T, indicating that the charge state of the single dot was clearly controlled by both the gate voltages despite the multidot structure and the metal multidot SED has potential for logic-gate operation. The top and bottom gates affected the electronic state of the dot unevenly owing to the geometrical effect caused by the dot shape and size of the surrounding dots.

Recently, new types of computing technologies using nanodot devices have attracted considerable attention, such as quantum[1–4], reconfigurable[5–7], and reservoir computing[8,9]. A single-electron device (SED) can realize these technologies because of its high functionality and ultralow power consumption[10–13]. The SED exhibits a unique characteristic, known as the Coulomb blockade oscillation, with which the drain current (I_D) is periodically modulated by the gate voltage (V_G). This Coulomb blockade oscillation is caused by the charging effect of a nanodot (also known as the single-electron island) contained in the SED and cannot appear for a conventional metal-oxide-semiconductor transistor. In several previous studies, efforts were made to arrange a single dot between the SED electrodes and the

basic characteristics of the device[14–18] were evaluated for the application associated with conventional logic circuits[11,12,19–24]. Using the Si-based SEDs, the inverter operation[20], half-sum and carry-out operation[21], and multivalue memories[22] have been demonstrated thus far.

Considering the single-nanodot SED, which contains one nanodot between the source and drain electrodes, multiple SEDs must be connected via wiring to form logic circuits. In this case, the one-by-one electron tunneling occurring in SEDs requires time for the wires to charge and the operation must be very slow. Additionally, the size variability of nanodots induces the scattering of SED characteristics. To overcome these difficulties, the nanodot-array-based SED containing multiple nanodots without wiring was proposed and its functionality was demonstrated under multigate operation[5,6,25–28]. For example, a flexible-logic-gate operation was realized using a Si-nanodot-array SED, highlighting that the nonuniform capacitive coupling between the dots and gate electrodes is a key factor for achieving the logic operations[25–27].

Besides nanodot fabrication using lithography adopted in several previous reports, the dispersion of chemically synthesized nanodots or self-assembled nanodot growth in thin-film deposition can be used to form nanodot-array devices[5,29–35]. In these cases, the array comprises randomly distributed nanodots and numerous conduction paths with different properties must be formed. Although the single-electron tunneling properties may be difficult to detect in such complex systems, the Coulomb blockade properties were frequently detected[29–38] and the modulation caused by the gate voltage was clear and simple in some cases[32,35,37,38]. To determine the potential of these complex-array SEDs, further investigations using multigate operation are required. However, the single-electron properties controlled by multiple gate voltages have not been studied yet, which are important fundamentals for functional SEDs.

In this study, an Fe nanodot single layer embedded in MgF_2 sandwiched between two gate electrodes was used for the SED fabrication and the modulation of I_D against the top- and back-gate voltages (V_T and V_B, respectively) were systematically measured using the SEDs with simple Coulomb blockade oscillation. The results show that I_D achieved a clear but uneven response to both V_T and V_B, indicating the application potential of the complex-array SED in functional devices, including logic gates. The unevenness of the gate operations depends not only on the thickness of gate insulators but also on the dot shape and the arrangement of surrounding nanodots.

Methods

Schematic and the scanning electron microscopy images of the fabricated Fe nanodot device are shown in Fig. 1. The source and drain electrodes (Au/Cr) with a gap length L of 50–400 nm were formed on the thermally oxidized SiO_2 (200 nm)/Si substrate. Afterward, an MgF_2 (45 nm)/Fe (film thickness t_{Fe} = 1.8–2.9 nm) layer was formed between the electrodes at room temperature using the electron-beam deposition technique (base pressure < 10^{-7} Pa). In this t_{Fe} range, dispersed Fe nanodots were formed owing to surface migration and the aggregation of Fe atoms on SiO_2. Finally, the gate-insulating SiO_2

(300 nm) layer was prepared on the MgF_2 layer via sputtering, followed by the top-gate electrode (Au/Cr) formation. Details of the device fabrication are given in a previous study[37]. The drain current between the source and drain electrodes (I_D) was measured using a semiconductor parameter analyzer (Agilent 4156C) by applying the voltages V_T and V_B to the Au/Cr top-gate and Si (substrate) back-gate electrodes, respectively, in a closed-cycle cryogenic probe station at the sample stage temperature T of 8 K.

Results And Discussion

Typical current oscillation characteristics as a function of V_B are presented in Fig. 2 for two SEDs which will be named Device A and Device B in this report. In both the graphs shown in this figure, three $I_D - V_B$ curves at the V_T values of 1.8, 10, and 20 V are superposed. The observed oscillation curves are clear, and they originate from a single dot, as discussed in our previous study[37]. The oscillation period was approximately 27 (Device A) or 37 V (Device B) corresponding to the back-gate capacitance C_B of 0.0059 (Device A) or 0.0043 aF (Device B), respectively. Because C_B of Device B is smaller, the dot contributing the current oscillation in this device should be smaller than that of Device A. In both devices, the current oscillations were added to the constant background current components (~520 pA (Device A) and ~1.0 nA (Device B)), which were attributed to the parallel conductive paths comprising the dots with the Coulomb blockade lifted. Such dots attributing to the background current are considered relatively large and/or have higher tunneling conductance than the quantized value ($2e^2/h$)[37]. By comparing the $I_D - V_B$ curves with different V_T values, a systematic shift in the current peak was identified. With increasing V_T values, the peak around 20 V for Device A gradually shifted to 14 and 3.3 V (Fig. 2a). Similar tendency was seen in Fig. 2b for Device B with a peak shift from 22 to 16 and then to 9.3 V. These peak shifts toward the negative V_B direction demonstrated that the current oscillation characteristics can be controlled by both the top and back gates even in the metal multidot SED, where the change in the nanodot charging state by V_T can be compensated by V_B and vice versa.

To clearly understand the details of the peak shift as a function of the two gate voltages, V_T and V_B, a contour plot of drain current was employed[27]. For this purpose, numbers of $I_D - V_B$ curves were measured using various V_T values from 0 to 30 V in 300 mV steps, where the V_B sweep was conducted in the sequences of 0–30 V, 30––30 V and −30–0 V. The current oscillations were well reproducible for the back-and-forth V_B sweeps. In addition, they were satisfactory stable over a few days against the peak shift due to charge offset drift, similar to the findings of a previous study[38]. The data measured from V_B = 30 to −30 V are plotted in Fig. 3a and 3b as two-dimensional (2D) contour maps of the drain current corresponding to the stability diagrams of the device. The current peaks shown in bright contrast are systematically shifted. That is, the phase of the current oscillation can be controlled using V_T and V_B. These contour maps are simple and periodic, as indicated by the yellow dotted lines, although there is an irregularity in Fig. 3b at V_T = 17 V, which is caused by charge noise that may be attributed to the effect of satellite nanodots acting as the single-electron traps[37]. These characteristics can confirm that the major

current oscillation certainly originates from a single dot[37]. Controllability of the charge state of the single dot by the double-gate is clearly confirmed despite the multidot structure. The investigation of linear peak shift dependence on the V_B and V_T values in the complex nanodot array conducted in this study is unprecedented and important, and it has been discussed using multigate SEDs with a simple dot configuration[28,39,40] concerning the logic operation. The results shown in Fig. 3 suggest that the SEDs comprising randomly dispersed metal multidots can operate as two-input logic-gate devices.

Here, the stability diagrams are analyzed to understand the characteristics of the randomly dispersed nanodot system. For the devices investigated in this study, the top and back gates are capacitively coupled to the SED and the current peak shift according to the V_B and V_T values follows the equation given below:

$$C_B V_B + C_T V_T = const, \quad (1)$$

where C_B and C_T are the capacitances between the single dot and back/top gates, respectively. When V_T changes by ΔV_T, the peak shift in the current oscillation (ΔV_B) is given by the following equation[39]:

$$\Delta V_B = -(C_T / C_B)\Delta V_T$$

2

.

Therefore, the gate capacitance ratio C_B/C_T of the dot is given as $-\Delta V_T/\Delta V_B$, which is evaluated using the slope of the observed current peak line presented in the contour map[40–44]. Using Figs. 3a and 3b, the gate capacitance ratio C_B/C_T between the single dot and back/top gates was evaluated as ~1.2 (Device A) or ~2.0 (Device B). Therefore, using the C_B value described above, C_T was given as ~0.0049 (Device A) or ~0.0022 aF (Device B). These results are plotted in Fig. 4 with data from two other devices. For the device structure investigated in this study, the back-gate insulator comprised 200-nm-thick SiO_2 and the top-gate insulator comprised 45-nm-thick MgF_2 and 300-nm-thick SiO_2. Assuming the parallel-plate capacitor structure and bulk dielectric constants (3.8 for SiO_2 and 5.2 for MgF_2)[45], the capacitance ratio C_B/C_T is ~1.7, as shown in Fig. 4. For a total set of devices, the evaluated C_B/C_T followed this relation. Furthermore, each C_B/C_T ratio was between 1.2 and 2.7, showing clear discrepancy from this rough estimation using the parallel-plane model. This discrepancy was caused by the geometric factors of the dot array, such as nanodot shape and the arrangement of dots. In the following paragraphs, this is discussed using a simple model.

The nanodot-array SED comprises numerous dots with various sizes. Because dots are formed on the substrate plane, the planar arrangement of hemispheric nanodots can be assumed as a model for this discussion. In addition, for easy calculations, the model was simplified into parallelly arranged half-columnar dots with infinitive axis length. An example of the cross-sectional schematic is presented in Fig. 5 where the column axis of the dot is perpendicular to the paper surface. The dot is half-circular in

this diagram (gray), and it will be called the half-circular dot in the following discussion. By adopting this model, we only require 2D electric field calculations with less parameters. A compact software (EStat) based on the finite element method was used to simulate the electric field and evaluate the capacitances (per unit length along the column axis) between the dot and top/back-gate electrodes. Although the model was simplified, the simulation results must provide the intrinsic features of the nanodot array. In the next paragraph, the simulation results are explained with details of the model.

A typical model for evaluation is shown in Fig. 5. Notably, the horizontal and vertical magnifications of this diagram are different from each other. The in-plane diameter of the metallic half-circular dot is 30, 20, or 14 nm, referred to as *L* (large), *M* (medium), or *S* (small), respectively, throughout this report. They are arranged horizontally to form a dot array. In Fig. 5, the dot arrangement is called *LSL* in the central part and *M* in other regions. The distance between the adjacent dot edges was kept constant at 10 nm. The dots are sandwiched between two 100-nm-thick SiO_2 layers acting as the top and back-gate insulators. On the surface of these SiO_2 layers, two metallic gates (gray) are attached. For simulations, one of the gate electrodes was biased by 1 V, while the dots and another electrode were grounded. Simulated potential distributions are shown in Fig. 5 as color maps, and the lines of the electric force are represented by white lines. As described below, remarkable difference is observed between Fig. 5a for voltage application to the top gate and Fig. 5b for voltage application to the back gate. The electric force lines shown in Fig. 5b are almost parallel like those in a parallel capacitor, except near the dot edges. Thus, C_B of each dot must be almost proportional to the dot size. Conversely, in Fig. 5a, the electric force lines are strongly curved and those near the central *S* dot are attracted by the adjacent *L* dots. Some of them are absorbed by the *L* dots; therefore, C_T of the central *S* dot becomes smaller in this dot arrangement while C_T of the *L* dot becomes larger. This is because of the geometrical difference between the upper (roundish) and lower (flat) dot surfaces. The dot shape in the nanometer scale can modulate the electric field, changing the charge distribution on the dot surface and capacitance with the gate electrode. This suggests that the Coulomb blockade oscillation characteristics in the multidot SED comprising the complicated dot array are expected to be modulated by the shape and distribution of the dots, including the surrounding dots.

These simulations were performed for various dot arrangements, and the gate capacitance ratios C_B/C_T of the central dots were evaluated. Examples of the *SSS*, *MSM*, and *LSL* arrangements are plotted in Fig. 6. To check the applicability of the calculations, simulation results of circular dots with the same arrangements are superposed in the graph. Because the dots are symmetric in this case, the C_B/C_T ratio should be 1.0 in all the cases, reflecting the thickness ratio of the top (100-nm-thick) and bottom (100-nm-thick) insulating layers. The simulation results fit well with this value. Considering the half-circular dots, the C_B/C_T value shows a large change from 0.95 to 1.27 depending on the adjacent dot size. This is because of the nonuniform distribution of the electric field between the top and bottom gates, which is attributed to the geometrical shape effect of the central dot and surrounding dots (Fig. 5). In the *SSS* arrangement, for example, the roundish shape of the surface facing the top gate gathers the electric force lines rather than the flat surface facing the bottom electrode. Therefore, C_T becomes larger than C_B and

C_B/C_T is <1. For the large adjacent dot, as in the *MSM* arrangement, some electric force lines are attracted by the *M* dots, making the C_T value small, ultimately resulting in C_B/C_T of >1. Lager adjacent dots in *LSL* attract the electric force lines very much from the *S* dot, and the deviation of C_B/C_T from 1 becomes large. Similar results were also identified for *M* or *L* as the central dot. These fundamental discussions using 2D simulations must also be valid for the three-dimensional dot shape and arrangement. Geometrical factors of the multidot system resulted in the variation of the C_B/C_T value from the average value (Fig. 4).

Conclusion

In summary, the double-gate Fe nanodot-array-based SED comprising the SiO_2–Fe–MgF_2 system was fabricated using the vacuum deposition technique and its electric characteristics were investigated. The fabricated Fe nanodot device showed clear current oscillations originating from a single dot[37]. Such current oscillation characteristics clearly demonstrated that the charge state of a single dot could be controlled by both the top and back gates even in the multidot structure. The gate capacitance ratio C_B/C_T of the dot, defining the Coulomb blockade oscillation property controlled by two gates, was influenced by two geometric factors, including the nanodot shape and the arrangement of the surrounding dots. These issues are not limited to the Fe nanodot system and are valid for various other nanodot systems applied to the multidot SEDs. This phenomenon modulates the Coulomb blockade oscillation and provides a complex response to the input (gate) voltage. It may be useful to realize flexible logic gates as highlighted in previous reports [25–27], although further comprehensive studies are required in the future.

Declarations

Acknowledgments

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Author Contributions

T.G., M.A.,and Y.T. conceived the research project and designed the experiments. T.G. and I.A. performed the experiments. T.G., M.A., and Y.T. analyzed the data. T.G., A.T.F., M.A., and Y.T. prepared the manuscript. All authors discussed the results and reviewed the manuscript.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Figures

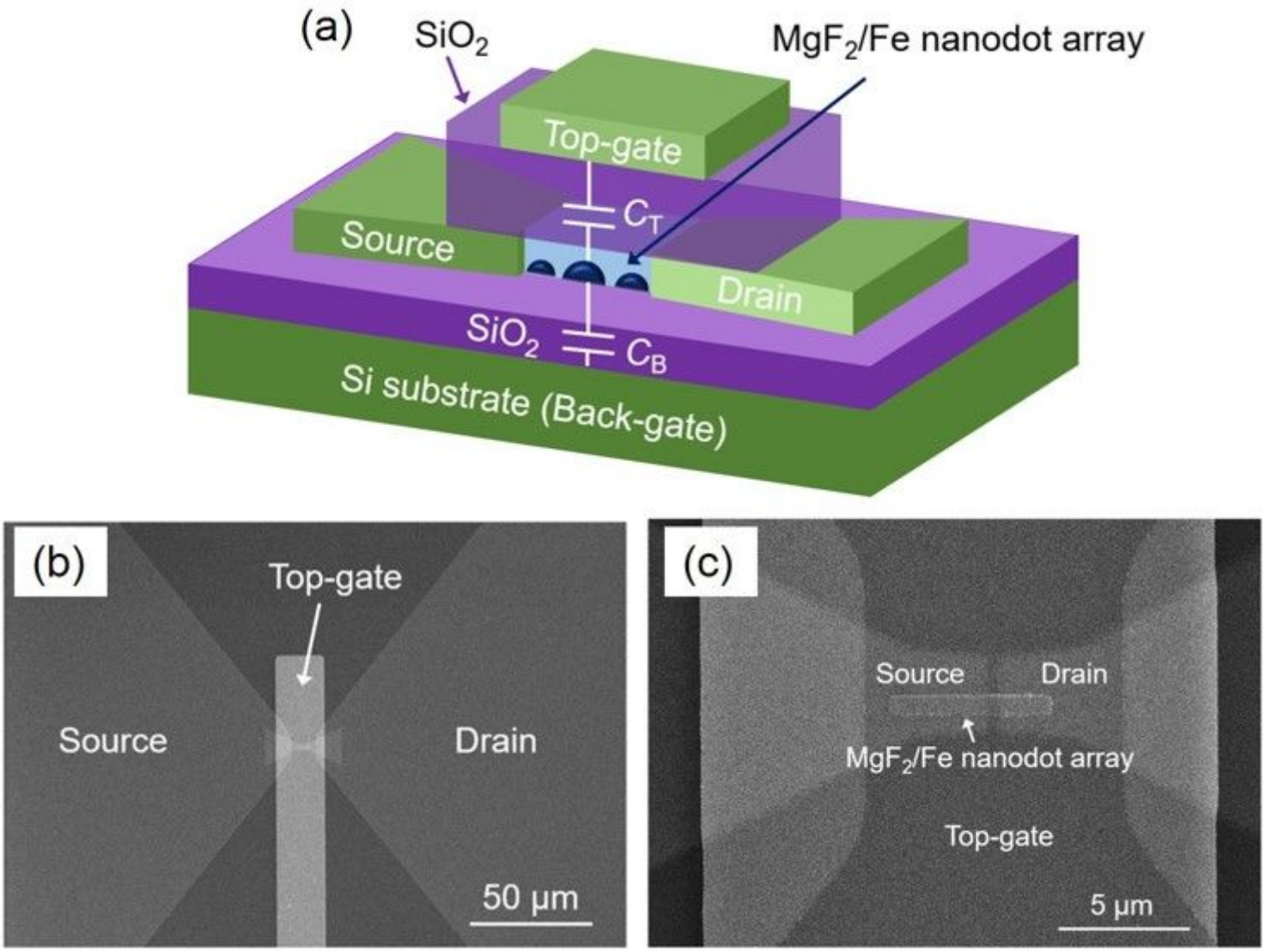

Figure 1

(**a**) Schematic and (**b**) and (**c**) scanning electron microscopy images (plan view) of the fabricated Fe nanodot array device.

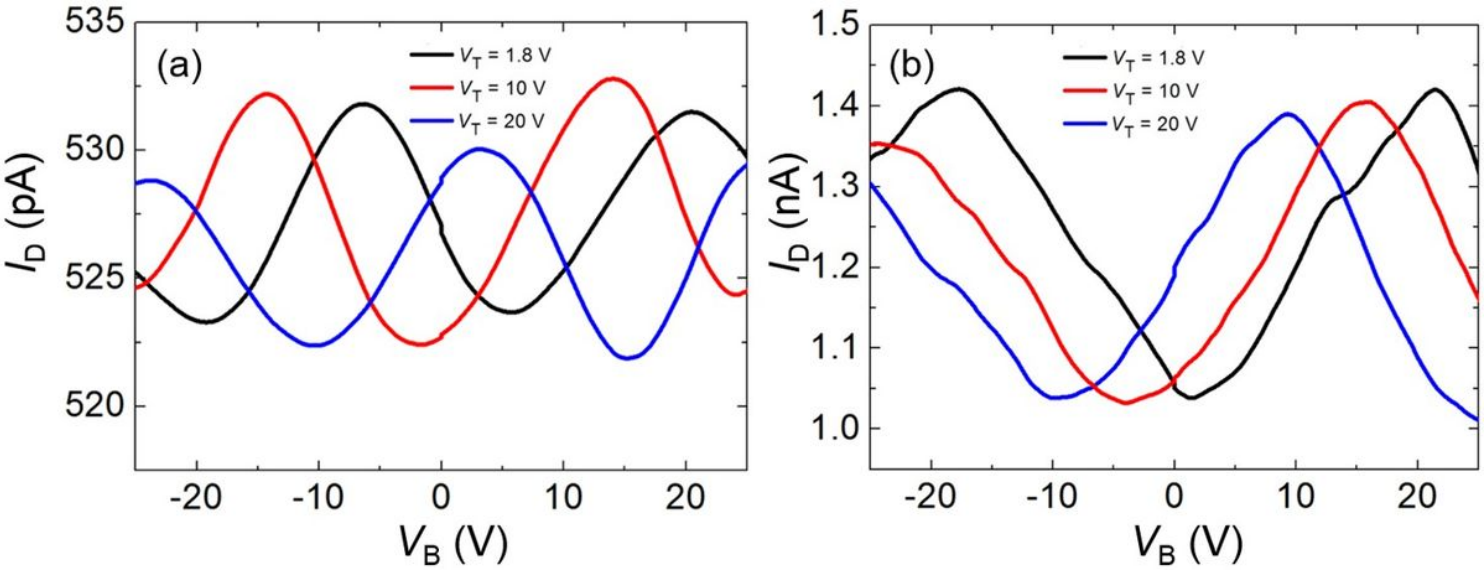

Figure 2

Current oscillations originating from a single dot measured as a function of the back-gate voltage V_B for (**a**) Device A (t_{Fe} = 2.4 nm and L = 50 nm) at drain voltage V_D = 20 mV and (**b**) Device B (t_{Fe} = 2.4 nm and L = 400 nm) at V_D = 2 mV. The top-gate voltage V_T was constant at 1.8, 10, and 20 V.

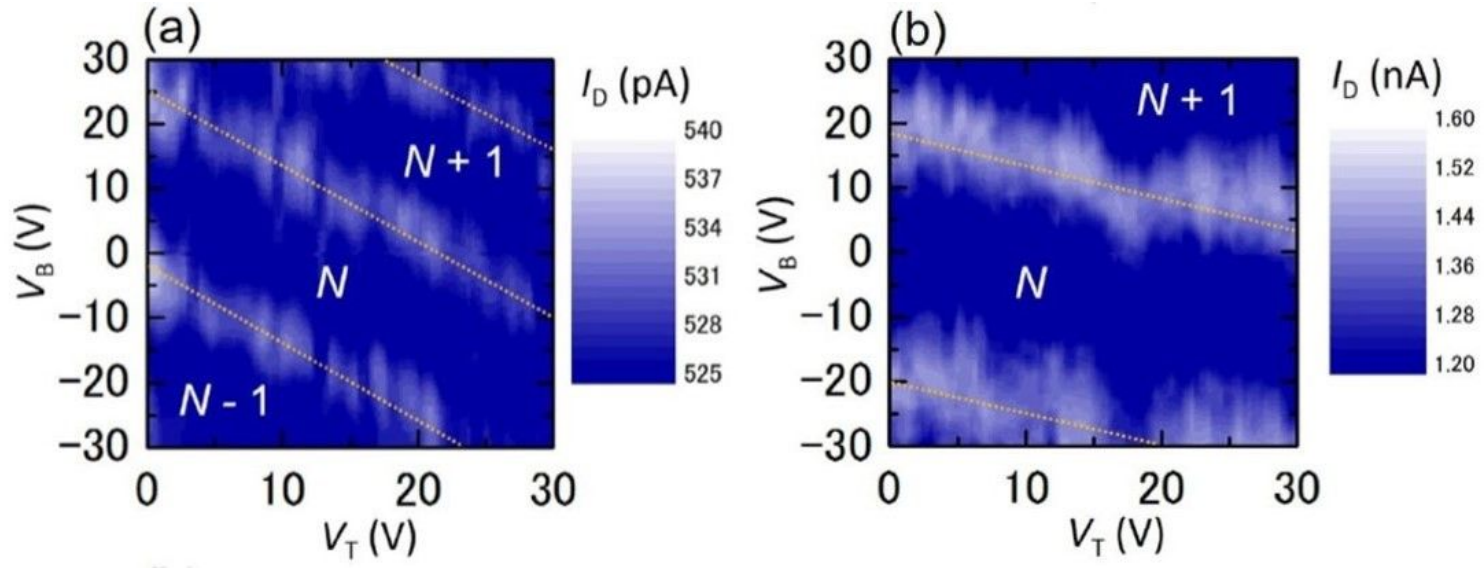

Figure 3

Typical two-dimensional contour-line maps of drain current I_D as a function of V_B and V_T. (**a**) Device A at V_D = 20 mV and (**b**) Device B at V_D = 2 mV. N is the number of electrons in a single dot.

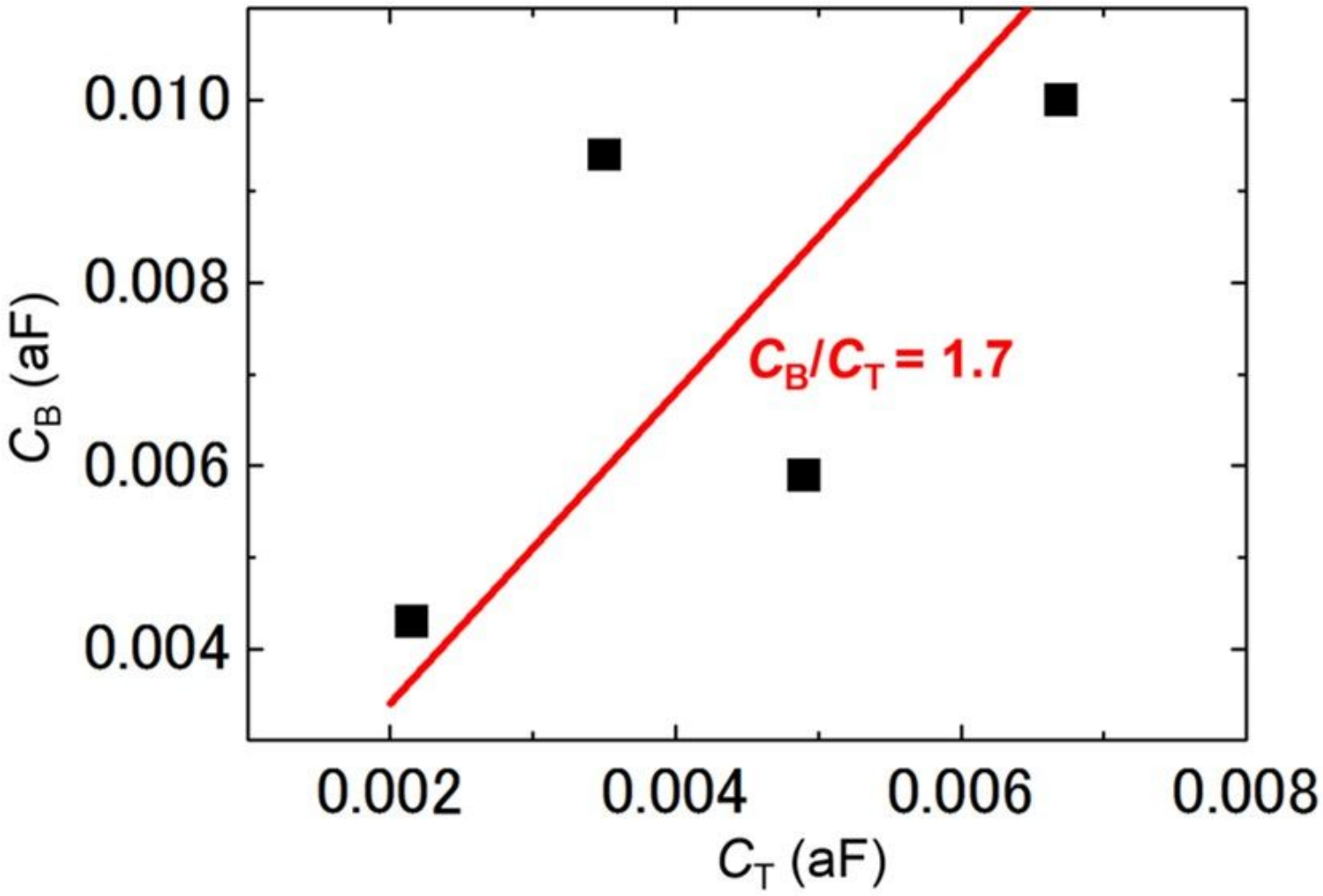

Figure 4

Plots of C_B vs. C_T of four devices showing simple current oscillation characteristics originating from a single dot. There is a positive correlation between C_B and C_T. The data roughly follow the relation without considering the shape effect of the nanodot system (red line).

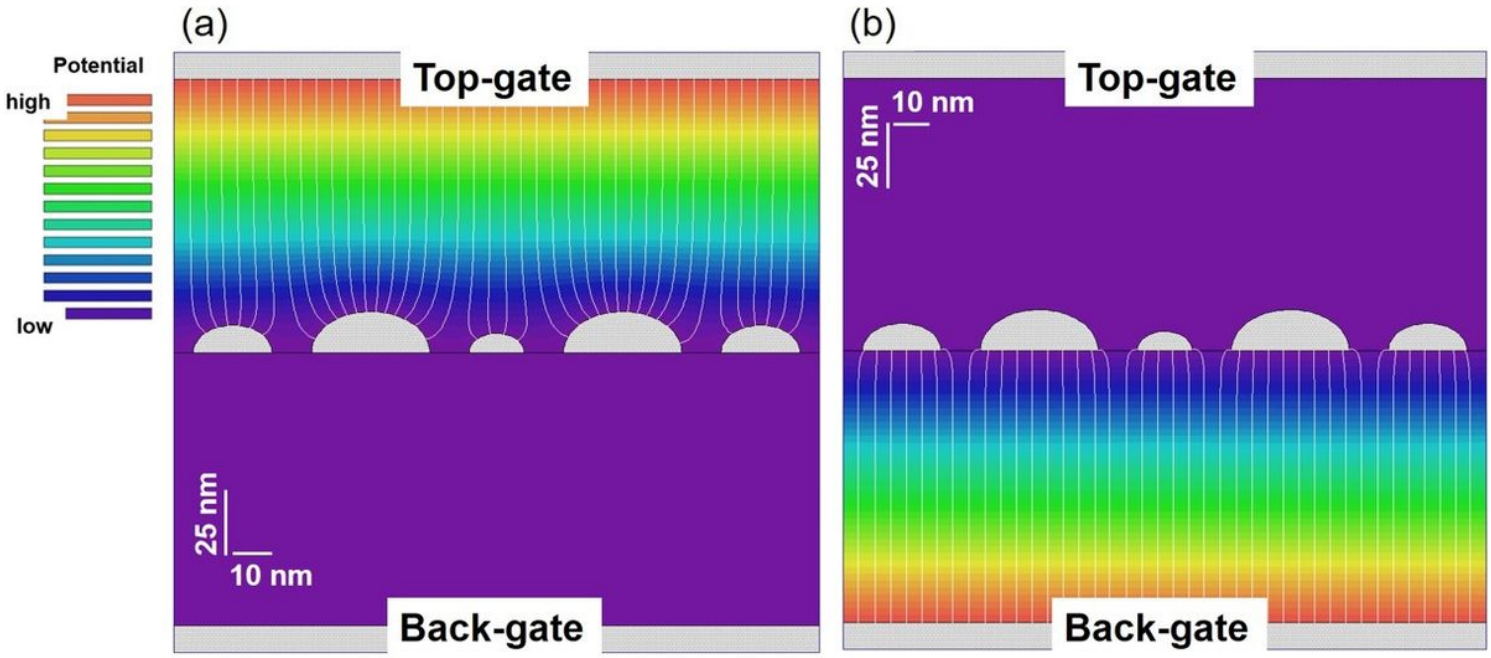

Figure 5

Simulation results of the electric potential (color) and the lines of the electric force (white lines) where the top or the back electrodes are biased by 1 V. Results for the *LSL*(*L* = large and *S* = small) dot configuration with biased (**a**) topand (**b**) backgate. For details of the model, see the text.

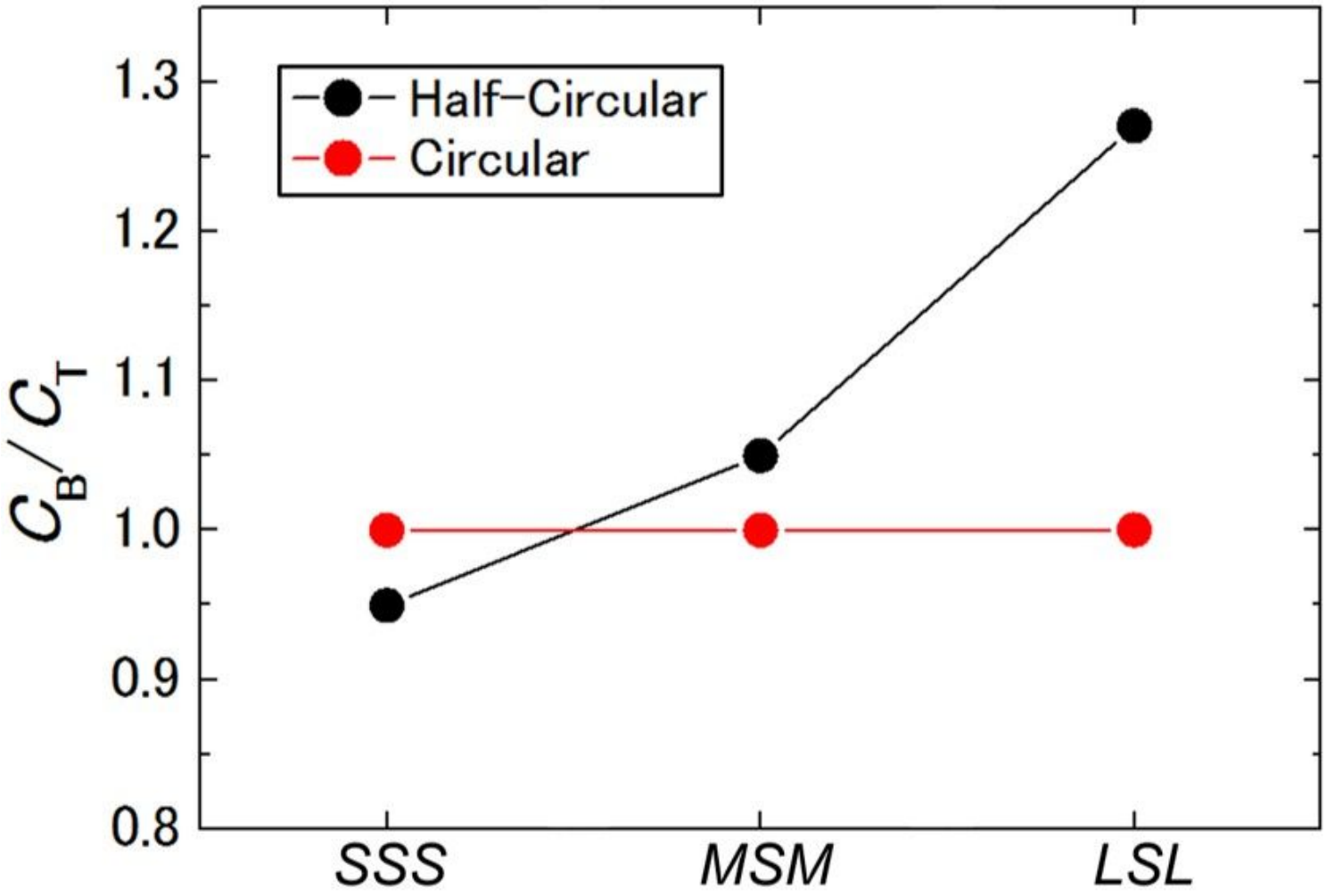

Figure 6

The gate capacitance ratio C_B/C_T of the central *S* dot for three dot configurations, *SSS*, *MSM*, and *LSL*(*L* = large, *M* = medium, and *S* = small). The C_B/C_T value for circular dots (red) and half-circular dots (black) are presented. The C_B/C_T value of the circular dots was almost constant at 1.0 regardless of the size of the adjacent dots. Conversely, it changed from 0.95 to 1.27 for the half-circular dots with increasing the adjacent dot size.