An Efficient Design of QCA Binary to Gray Code Converter for Telecommunication Systems

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Abstract Quantum Dot Cellular Automata (QCA) is a prominent technology in Quantum Electronics. This is implemented with the help of quantum cells which are also known as basic building blocks of Quantum Electronics. In QCA technology there are four different clock pulses, clock delay for each clock cycle is 0.25 ns. Using this technology now we are implementing the Binary to Gray code converter. In this paper, we are proposing a design to reduce the number of cells when compared to the previous designs and we are also extending the implementation of the converter up to 5-bits. The number of cells in the proposed design is improved by 2.5%, 36.44%, and 50.66% for 2-bit, 3-bit, and 4-bit respectively. Also, for 3-bit and 4-bit, the total occupied area is improved by 55.56% and 74.680% respectively. In our proposed design it helps us to decrease the area from the previous circuit, which may also lead to the decrease in the power consumption.

Keywords Quantum dot cellular automata · Quantum electronics · gray code · Power consumption

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1 Introduction

In the recent years, QCA is the best alternative for the Complementary Metal–Oxide–Semiconductor (CMOS) technology [1]. It is a transistor-less nanotechnology which allows to build logical circuits which has functioning frequency up to THz which is not possible in existing CMOS technology [2]. This Technology has a unique way of designing the circuits by arranging the quantum cells. In the past few years, as it is a transistor-less nanotechnology it depends on its electron configuration, it is well known for its ultra-high speed, low power consumption, small size and has higher switching frequency better than transistor based technologies [3]. Because of all these reasons it is replacing the CMOS technology. This has the ability to design digital circuits with small area, lower power dissipation, higher packaging density, high performance compared to CMOS technology. QCA works on a manometer scale which leads to the ultra-dense and high-performance circuits [4].

It consists of quantum cells containing quantum dots. Each Quantum cell is a square shaped structure containing four quantum dots in it which are internally connected through a tunnel, these quantum dots are situated at the edges of the quantum cell [5]. An individual cell represents a binary bit either '1' or '0' as shown in Fig.1. This representation is done when two electrons occupy the diagonal positions of the cell, depending upon those positions we calculate the polarities of the cell. The polarization range of the quantum cell is -1 to 1 [8,9]. We can calculate these polarization's w.r.to the following formula,

$$P_{cell} = \frac{(\delta_1 + \delta_3) - (\delta_2 + \delta_4)}{\delta_1 + \delta_2 + \delta_3 + \delta_4} \tag{1}$$

According to the above formula, if we calculate polarization of any cell we have three polarization's (P_{cell}). If P_{cell} = -1, then it is represented binary bit '0'; if P_{cell} = 1, then it is represented as binary bit '1'; if P_{cell} = 0, then it is known as a normal cell [6]. The orientation of the cell is named in clockwise direction. Each Orientation is named as δ_1, δ_2, δ_3 and δ_4. At a single instance, only two electrons can be occupied in a quantum cell that too in alternate positions (δ_1 and δ_3; δ_2 and δ_4).

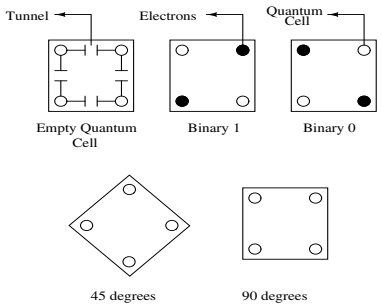

Fig. 1: Various structures and orientations of Quantum cell

In this paper, Binary to Gray code converters up to 5-bit are proposed. The paper is organized as follows. Section 2 gives an overview of how different clocks are used in QCA designer tool and simulation. The algorithm for binary to gray code conversion and proposed designs are discussed in section 3. The simulation results and performance parameters are deliberated in section 4. Section 5 gives conclusion on our proposed architectures.

2 QCA design & Clocking: An Overview

QCA is a technology whose basic element is a cell. We are using QCA Designer tool to design the circuits. In this designer tool, we have a different colour coding indicating its own speciality like input, output etc as shown in Fig.2. In this tool there are no wiring's [7]. We can select any particular block and replace or remove the block when and wherever we need to change. In this technology, the QCA wire means the way of arrangement of the cells and its angular position. Depending on these things the electrons move by passing the information to its neighbouring cell. The whole logic in any circuit lies between input and output of the circuit arrangement. Compared to other technologies like CMOS where the logic is very complicated if we have to change any wire, we have to look for every part of the circuit but in this tool we can replace wherever we need to replace the cell/ wiring [19-22]. In Fig.1, there are two angles of clock wiring's or flow of arranging the quantum cells i.e., 45 degrees and 90 degrees.

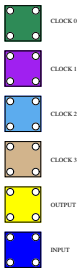

Fig. 2: Colour coding of Quantum cell

In any CMOS circuit we need clock to control it. Similarly, this technology also uses clock to control circuit. We have four different clock pulses [10]. Each clock pulse starts with a different phase. In QCA each and every cell is clocked. The four clock pulses are clock0, clock1, clock2 and clock3 [20-23]. Each clock has its own colour such as clock0 is indicated by green colour, clock1 is indicated by pink colour, clock2 is indicated by sky blue, clock3 is indicated by cream colour as shown. The input is always set to clock0 and the output clock can be any clock out of four. In any clock pulse each clock cycle in it consists of four phases that is switch, hold, release and relax [24-27].

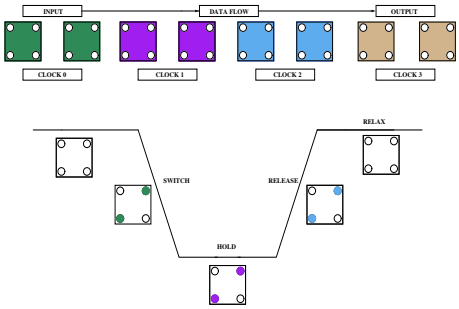

Fig. 3: Data flow representation in QCA

The clock phases change due to the tunnel present in QCA cell, which is like a potential barrier in the cell as shown in Fig.3. In order to control the potential barrier which exists when the electrons present in the quantum dots as they try to move along the tunnel junction and another barrier comes into play when switching occurs between the cells [18].

Switch phase: This phase gives rise to polarization. Here initial start of tunnelling of electrons are held strongly due to obstruction caused by the polarization effect between the dots.

Hold phase: As the name of this phase depicts the electrons will be strongly held in their previous position within the cell as polarization remains same as achieved in the last phase.

Release phase: In this phase QCA cells polarization is lost and it is converted back into its normal un-polarized state. As a result, the obstruction between dots is reduced and the electrons can move through dots.

Relax phase: The obstruction between the quantum dots remain same as obtained in the release phase and therefore the cell's state remains same.

The demonstration of all these phases of clock are shown in Fig.4

The basic difference between circuit designing in QCA and CMOS technology is that a circuit in QCA technology is not controlled through the clocks where as in CMOS it is contrary [19]. Hence in this technology the information is transmitted through each and every cell and not preserved. Every cell erases its state in every clock cycle as shown in Fig.5.

The Cell begins to polarize in the switch level and remains in the same state till the complete cell becomes polarized [14]. After reaching the elevated level that is hold stage, the cell stores its polarization. The cell polarization reduces once its clock reaches the release state. Finally, in the relax level of the clock, the cell completely

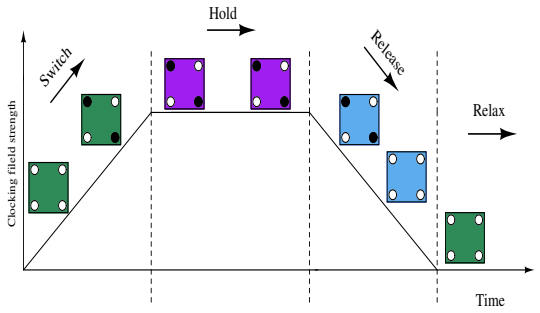

Fig. 4: A graph showing different phases in one QCA clock cycle

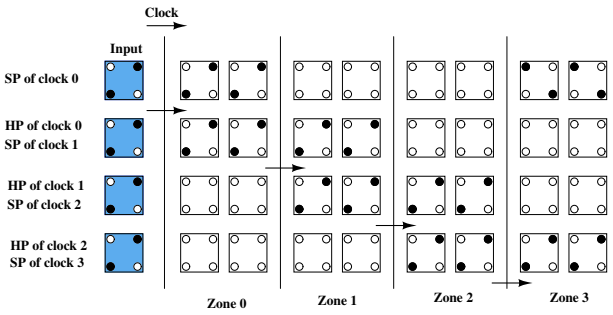

Fig. 5: Operation of wires in QCA

becomes unpolarized. The clock zones number in the critical channel of a QCA circuit design regulates its complete clock delay. In Fig.5, we can see the operation of a wire in different clock zones [15,16].

3 Proposed QCA Design

In the QCA technology the computation is done by the arrangement of cells and the polarization of neighbouring cells. We are using QCA Designer 2.0.3 version which is an open source software to design our proposed circuit. The Design's functionality is confirmed by this tool, but this tool has some default parameters such as size of the cell, relative permittivity, relaxation time, number of samples etc. We are going to implement one of the code converters using this tool by trying to reduce the number of cells.

A Binary to Gray code converter is a logical circuit which takes the input as binary number and gives the equivalent gray code to those particular binary bits. The conversion is done using simple two bits in terms of representation i.e., '1's and '0's. In these binary bits '1' means high or ON and '0' means low or OFF, these are the terms used in computer world or any manufacturing technologies [11-17]. The Binary

code is a weighted code, as it has positional weights whereas, Gray code is a non-weighted code, it does not have any positional weight. An example of Binary to Gray Code conversion is shown in Fig.6 for binary bits B = 10101.

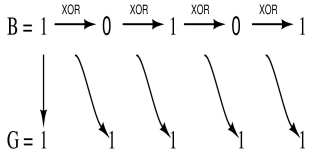

Fig. 6: Example to convert from Binary to Gray code

In the above example we have seen how a binary code is converted to gray code. We are going to implement this logical circuit (Fig.7) in QCA Design tool. We are focusing in reducing the number of cells used, decreasing the area and also implementation of code converter up to 5-bits.

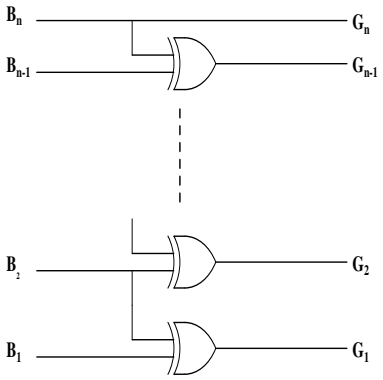

Fig. 7: Block diagram of Binary to Gray code converter

Generally, a code converter is a logical circuit used to convert one system of code to another system of code. In this paper, we are proposing the Binary to Gray code Converter from 2-bits to 5-bits. For 2-bit,3-bit,4-bit we are reducing the number of cells when compared to the existing architectures. And we have extended our design up to the 5-bit in this QCA Designer tool. The process of binary to gray code converter is simple i.e., the n^{th} bit of binary code is given as it is to the n^{th} bit of gray code as the MSB of binary code gray code are same and remaining bits of gray code are obtained by performing xor operation. The xor operation is performed between n^{th} bit and $(n-1)^{th}$ bit and this continues till the last bit or LSB. The process of conversion of binary code to gray code is explained in Algorithm.

Figures 8, 9, 10, 11 shows the schematic representation and wave forms of proposed 2-bit, 3-bit, 4-bit and 5-bit binary to gray code converters respectively.

Algorithm 1 Algorithm for Binary to Gray code conversion

Input: n-bit binary stream (B)
Output:n-bit binary stream (G)
Initialize: B=$b_1, b_2 \ldots\ldots b_n$ (b_i is i^{th} binary input where i=1,2,3,. . . .., n, b_1 is MSB)
Initialize: S[n]=elements of array, i.e. bits of B and P[n]=elements of array i.e. bits of G

```
/* Taking the Inputs */
For i=1 to n
        S[i] ← b_i
        Next i
End For
/* Conversion to Gray code and storing */
P[1] ← S[1]
For i=2 to n
        P[i] ← S[i] XOR S[i − 1]
        g_i ← P[i]
        Next i
End For
```

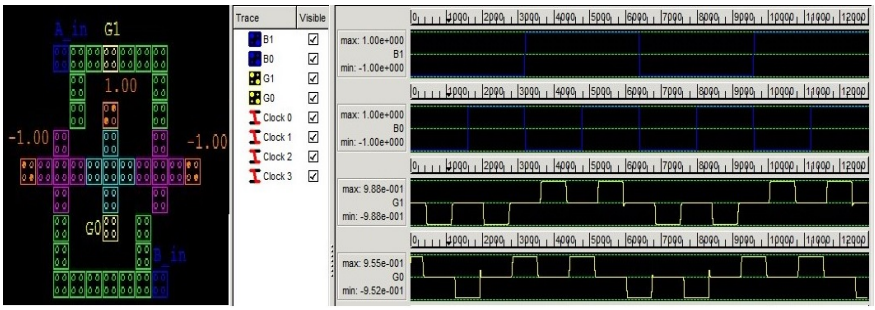

Fig. 8: The Schematic view and output wave forms of proposed 2-bit circuit

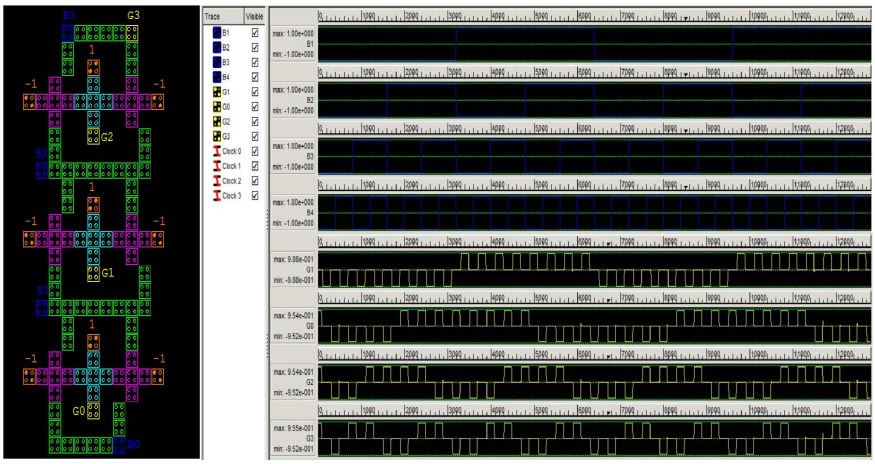

Fig. 10: The Schematic view and output wave forms of proposed 4-bit circuit

Fig. 9: The Schematic view and output wave forms of proposed 3-bit circuit

4 Results & Discussions

In this designer tool we are implementing the circuits by reducing number of cells and extending number of bits up to 5. We are using the Bi-stable approximation parameters mentioned in Table:

Area utilization factor (AUF) is an important parameter in QCA. It is the ratio of total occupied area by cells to that of total required cell area. It is a unit-less quantity. As AUF increases, the efficiency and reliability also increases.

$$AUF = \frac{Total\ area\ occupied\ by\ cells}{Total\ area\ required\ by\ cells} \tag{2}$$

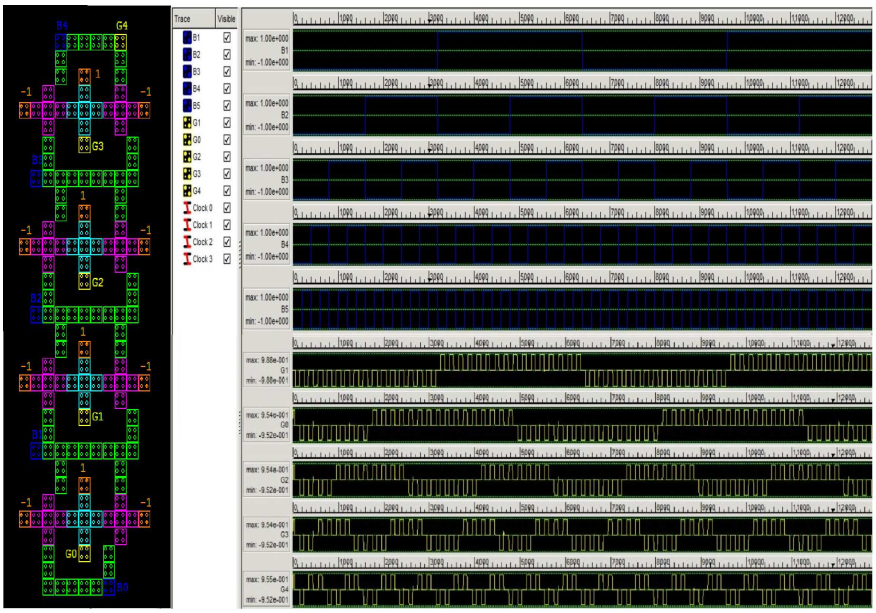

Fig. 11: The Schematic view and output wave forms of proposed 5-bit circuit

Table 1: Bi-stable approximation parameters

Parameters	Values
Cell width × Height	$18 \times 18\ nm^2$
Number of samples	12800
Convergence Tolerance	0.001000
Relative permittivity	12.900000
Radius of effect	65.000000 nm
Clock high	9.800000e–022 J
Clock low	3.800000e–023 J
Clock amplitude factor	2.000000
Layer partition	11.500000
Highest iterations per sample	100

Table 1 gives the performance comparison of proposed designs and existing designs in terms of number of cells used, total occupied area, total required area, area utilization factor and clock delay. The clock delay is same, as same number of clock phases are used. But there is a decrease in number of cells required from existing to proposed designs. Also the total occupied area and total required area is decreased which in turn increases the AUF.

Table 2: Comparison of performance parameters of proposed architectures with existing architectures

	Parameters	Number of cells	Total Occupied Area (nm^2)	Total Required Area (nm^2)	AUF	Clock delay (ns)
2-bit	[5]	40	39600	12960	3.05	0.75
	Proposed design	39	39600	12636	3.01	0.75
3-bit	[5]	82	79200	26568	2.98	0.75
	[28]	118	76000	-	2.80	0.75
	Proposed design	75	74800	24300	3.07	0.75
4-bit	[5]	126	114400	40824	2.80	0.75
	[29]	108	100000	-	-	0.75
	[30]	225	434451.36	-	-	1
	Proposed design	111	110000	35964	3.05	0.75
5-bit	Proposed design	147	145200	47628	3.05	0.75

5 Conclusion

QCA is a desired technology that helps in reducing area when compared to CMOS technology and it has low power dissipation, functional frequency is up to Tera Hertz (THz). In this we scale the designs through nanoscale. In this paper, we are designing the binary to gray code converter by optimizing the minimum number of cells for 2-bit, 3-bit and 4-bit; and we have extended the designing up to 5-bit converter.

We are making the design more efficient and reliable design compared to the previous existing designs. We have reduced the number of cells used, total occupied area is reduced, total required area is reduced, area utilization factor is increased and clock delay remains unchanged as we use same number of clock phases. With these set of calculations we can conclude that our design is efficient compared to existing designs.

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6 Declarations

Funding

Not Applicable

Conflicts of interest/Competing interests

Authors declare no conflict of Interest

7 Author Contributions

All authors contributed for the design and analysis of QCA converter.

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