

An Analytical Approach of Error Detection and Correction for On-board Nano Satellite

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Research Article

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RESEARCH

An Analytical Approach of Error Detection and Correction for On-board Nano Satellite

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Abstract

Nanosatellites are persistently progressing and creating global communication and data transmission worldwide. It builds up a colossal request for more progressed and dependable frameworks that can perform faster and more reliable information transmission. An approach has been distinguished as a good plot for anticipating single bit and multiple bit errors that are influencing On-board Nanosatellites. In this paper, we have proposed an Analytical Approach of Error Detection and Correction for On-board Nanosatellite. We have planned the framework separately with three distinctive parts: an encoding, error checking, and decoding portion. It has been created so that amid information exchange from satellite to the ground station, it analyzes six camera pictures simultaneously with the assistance of FPGA and EDAC strategies. We have presented the progressed turbo mechanics EDAC for unprecedented transfer speeds of satellite communication and execution examination with the AWGN and Rayleigh channels to extend the proficiency. EDAC strategies codes are tried in MATLAB and appear in graphical plots. This method is straightforward and accomplishes unwavering quality and exactness compared to comparable strategies.

Keywords: Error detection and correction; Low density parity check; Bose–Chaudhuri–Hocquenghem codes; Turbo codes; Convolutional codes; Shannon's theorem; Earth observation

1 Introduction

A nanosatellite is a device that moves in a bent way around a planet. Earth observation satellite is one of the fundamental devices for the investigation of the earth's environment [1]. Earth observation satellites apply high-resolution image sensors from the earth's surface to watch and get data on the earth's surface and utilize infrared for underneath observation. By watching earth from space, EO satellites give fundamental data on climate observing, urban checking, natural disaster, rural development checking, and natural checking etc [2]. Unfortunately, we missed our valuable data when interference occur in the data transmission.

Nanosatellite's error detection and correction devices aim to perform secured and error-less information transmission between satellite and ground station. They are subject to unsteady and unstable data corruption because of thermal noise, high energy particle impact, or other noise. Single bit and burst errors are two common types of satellite data communication errors. A single-bit error implies one bit changed from 0 to 1, and a burst mistake implies more than one conjugated bit

adulterated [3]. The mistake discovery handle is the primary step to error redress, which is subordinate to adding extra bits to the first information. Excess bits are accomplished through two basic coding plans convolution coding and block coding. Error correction can be classified as a Forward error correction and automatic repeat request. Sometimes ARQ and FEC can be combined [3]. This strategy is called a Hybrid automatic-repeat request program. There are numerous frameworks outlined to distinguish and redress mistakes. We introduced this core EDAC algorithm LDPC, Turbo code, BCH code, Convolutional code, and Shannon's theorem to our system to increment the proficiency of EDAC. Also, we analyzed their combined form of them. We presented a progressed turbo component with two interleaved, five encoding forms, and five interpreting forms. All the mechanism is tried in MATLAB with AWGN and Rayleigh channel.

The main contributions of this paper are as follows:

- We have proposed an architecture that consists of the EDAC method for the nanosatellites.
- We have studied, analyzed and compared the satellites' error detection and correction algorithms.
- We have identified the number of erroneous bits. Based on that, we have also proposed suitable error correction methods.
- We have implemented the scheme for the LDPC, BCH, Turbo, Convolutional and Shannon's theorem.
- We have analyzed the performance of five different EDAC algorithms with two different channels in MATLAB.
- Finally, we have identified the limitations of our proposed methods.

The rest of the paper has been depicted within the taking-after way. Segment I examine the EDAC strategies of nanosatellites. The objective behind the investigation has been displayed in segment II, and the proposed framework engineering method has been discussed in area III. Area IV appears the algorithmic investigation and performance analysis of EDAC Mechanism V-1.1. Area V and VI describe the EDAC Mechanism V-1.2 and EDAC Mechanism V-1.3. Area VII examines the execution of result advancement. Area VIII describes the limitation and future work of EDAC. In conclusion, area IX concludes our paper.

2 Related Works

Mamun et al.[1] proposed a Hamming Code to prevent parity and parity single bit error onboard satellites in LEO. The main focus is to work on EDAC via generating a Hamming Code matrix [16, 11, 4]. MATLAB is used for the implementation process of Both single-bit and double-bit errors. Pakartipangi et al.[4] proposed a technique for obtaining more comprehensive coverage area images for low dimensions satellites. The system handles all the errors bit using the XULA2 LX9 FPGA board and the camera array was designed so that overlapping areas can't be found. Ahmed Hanafi et al.[5] proposed an SRAM-based FPGA technology that implements an onboard computer system and uses low earth orbit Nanosatellites. The system was designed for developing a payload architecture and an inherent space environment. Ibrahim et al.[6] proposed a satellite system designed with acceptable

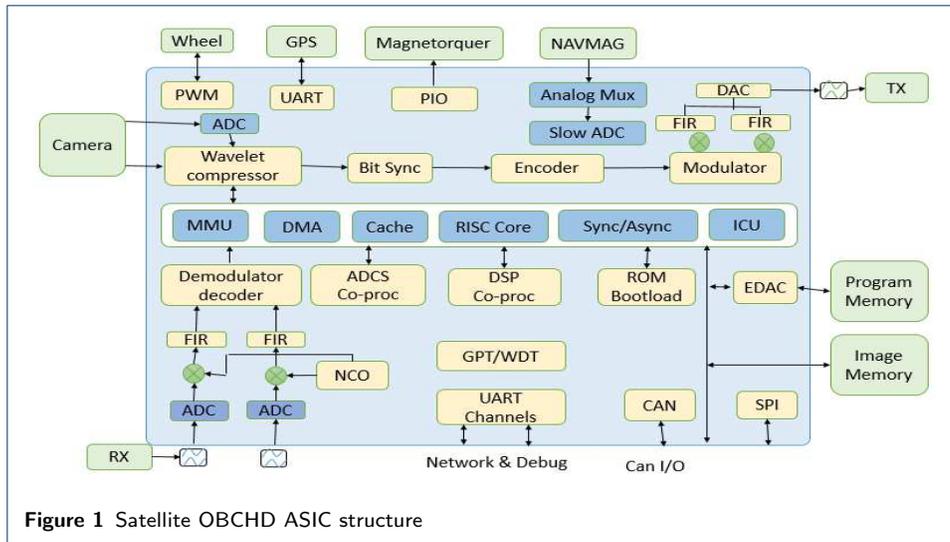
accuracy in a low power system. This paper presents a concept to establish avionics systems by utilizing crucial features with the available FPGAs. Scrubbing keeps the FPGA data configurations safe with frame calculation and back-tracking methods.

Daniel et al.[7] proposed a technique that describes a guideline for simulating the system accuracy providing the necessary statistics to support the decision system regarding the necessary methodology to be implemented[7]. The system is designed so that it can monitor air pollution in Mexican and Latin American cities. Wilson et al.[8] proposed two major supervise themes hybrid computing and re-configurable computing[8]. The system survey of the impose and convenience for small satellites also focuses on new technologies, methods and implementation for the next generation[8]. Banu et al.[9] proposed an encryption method to secure terrestrial communication via small satellite. Increased quantity of sending valuable and sensitive data, a satellite can bring risks of providing access to unauthorized data. An advanced encryption standard method is used to protect data from such threats. Banu et al.[10] proposed a commercial algorithm also known as Advanced Encryption Standard. To protect sensitive data and prevent unauthorized access in terrestrial communication 5 modes of AES in satellite imaging have been used. To prevent the fault from noisy channels and the effect of SEUs, that textit 5 modes were analyzed and observed using Hamming error correction code.

Hiler et al.[2] proposed a parity check matrix and a calculated syndrome of EDAC onboard nanosatellites. The scheme can self-detect and self-correct any single event effect errors during transmission. BENTOUTOU et al.[11] proposed an onboard EDAC method to protect data transmission among AISAT-1 CPU and its memory. The following paper presents the applications of double bit EDAC and its implementation with FPGA. Wang et al.[12] execution comparison of devotee goof correction codes for correcting colossal burst data ruins. Colossal burst goofs as regularly as conceivable happen in flunky communication driving to different chosen bit goofs. interior parts of the paper, we compare the CCSDS codes, such as RS codes convolution, turbo, and LDPC codes. Gao et al.[13] gives a thought of LDPC codes for the joint attendant and characteristic broadcasting framework. In this paper, we show an earthbound broadcasting framework called another Time Broadcasting-Wireless and Specialist and will be gotten a handle on inside the more conspicuous China run and some of the other parts of Asia. This framework gives excellent execution results, especially for combined deciphering.

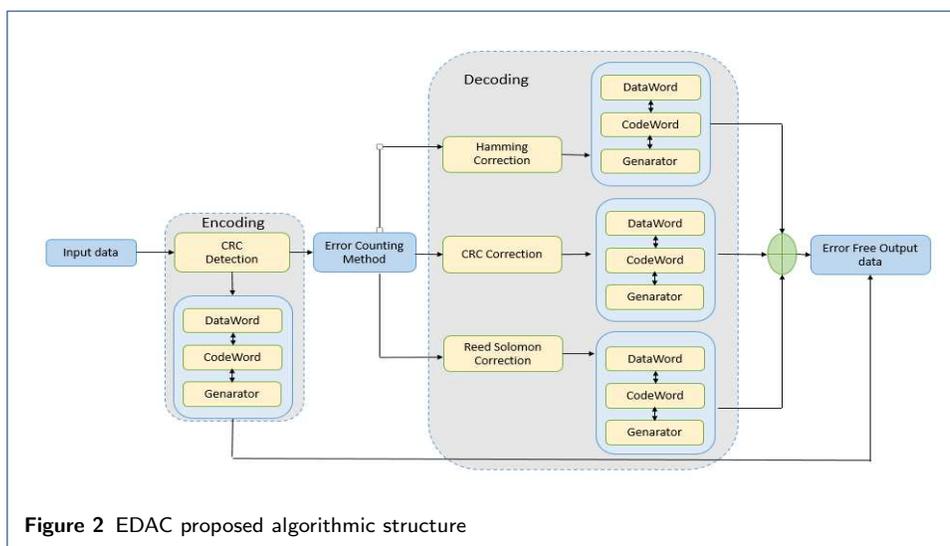
3 Methods

Satellite onboard command data handling structures are shown in figure 1. For a low-cost framework of the nanosatellite, a single chip executed On-board command information dealing with (OBCDH) was proposed for a mixed-mode application-specific coordinates circuit (ASIC) [5]. Future Nano Satellites, which have information handling and control capacities with information collecting and further detecting capabilities for Soil perception Missions, result from ASIC detail. Square graph 1 comprises of 4 Subsystems where a 32-bit RISC processor centre is adjusted for



space utilization, a Subsystem of picture dealing with the unit, a communication association for the satellite and a supporting fringe subsystem. OBC is the most component of to scaled-down OBCHD framework. To serve an introductory model of the advanced portion of the OBCHD ASIC, this onboard computer framework on a chip figure 1. Within the OBCHD, our fundamental need is to upgrade the EDAC framework to have error-free information on disciple communication. In EDAC, mechanisms V-1.1, V-1.2 and V-1.3 describe the different approaches to solve the satellite communication error and analyze the performance of different channels.

4 EDAC Mechanism V-1.1



Nanosatellites that transmitted information to the ground station from their blunders can be checked with the assistance of a few calculations. Within the ground station, CRC checks blunder information. After that step with a sort of blunder, able to get the information indicated by detection methods. Within the location

strategies, we figure out whether blunders are shown in our data in case of able to distinguish using three steps like information word codeword generator at that point able to recognize the erroneous bit within the input stream appeared in figure 2. Based on our mistakes, we ought to alter our calculations agreeing to the measure of mistakes. In this adjustment strategy like Hamming, CRC and Reed Solomon codes, with the assistance of these adjustment strategies, we would present at long last get our wanted errorless information.

4.1 Hamming code

Hamming code could be a direct piece code for blunder location and redress. Hamming codes can identify one-bit or two bits mistakes at the same time and it can rectify them as they were single-bit mistakes. The fundamental concept of the hamming code is to include an equality bit after the stream of information to confirm that the information was gotten by the ground station and matches the comparing input information stream. Partisan ground stations check the transmitted information so that they distinguish where the mistake has happened. The structure of the hamming code has square length, message length, and separate. square length characterizes as $n = 2r - 1$ where $r \geq 2$ message length and remove is $2r - r - 1$. Depending on the hamming code adaptation remove esteem got changed. Due to including more than one equality bit, this conspire can find the position of the blunder and self-correct it by altering the bit. Generally, three sorts of hamming codes are utilized in Nano-satellite communication such as Hamming[7,4,3], Hamming[8,4,4], and Hamming[16,11,4].

4.2 Cyclic Redundancy Check

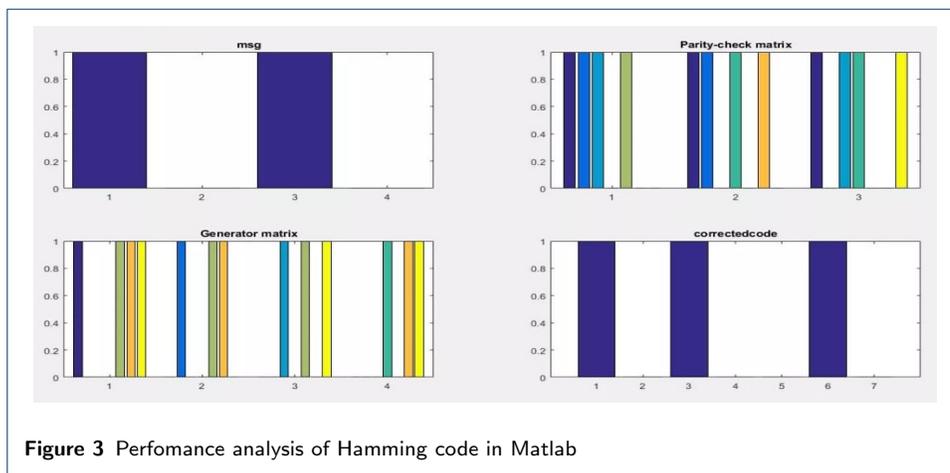
CRC is the method of accepting emerging alter blunders within the communication channel. Satellite information trade is based on CRC codes and the EDAC process broadly utilized in advanced CRC code is additionally commonly alluded to as polynomial codes -1 on a thin wire. Working on a thin wire is characterized as polynomial checks. The k-bit message is considered a polynomial condition list with the words k, from $x^{(k-1)}$ to x^0 . The most noteworthy arrange is the coefficient of $x^{(k-1)}$, the another thing is the proportionate of $x^{(k-2)}$, and so on. Test digits are created by rehashing the k-bit message x^n and part the produced by $rm(n + 1)$ bits polynomial code. The excite n -bit adjust is passed as test digits. The total collection grouping is separated by the same polynomial generator. If the remaining pieces are zero, no mistakes have occurred. If the remaining pieces are not zero, an exchange blunder happened.

4.3 Reed Solomon

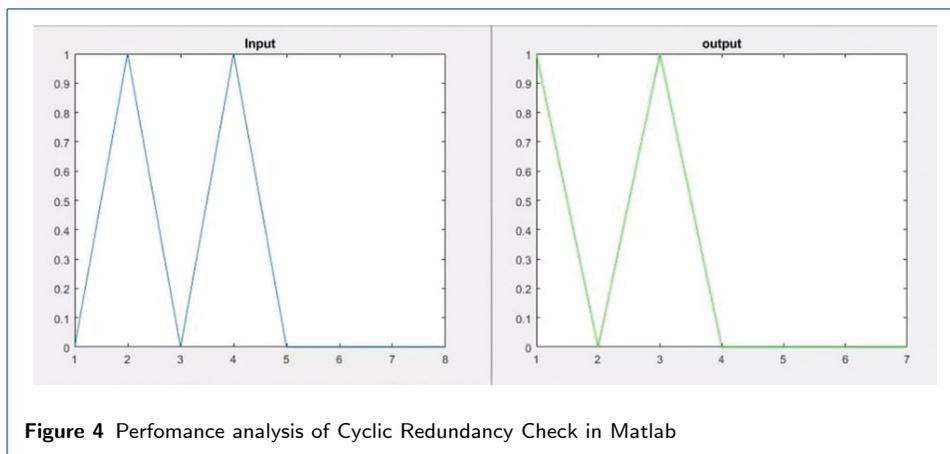
Reed Solomon codes work with a burst sort of information mistake. It is moreover utilized as a broadcast framework in adjustment code communication additionally in capacity framework etc [14]. It recognizes the burst blunder of information transmission and amends those blunder information. If the Reed Solomon codes are utilized at that point, the likelihood of an error remaining within the decoded information will be much lower [15]. Reed Solomon codes are too appropriate for different burst blunder adjustment codes as a grouping of $b + 1$ sequential mistakes

can influence up to 2 signals of measure excited [16]. The excited alternative goes to the coding architect and can be chosen over a wide range. Reed Solomon's mistake adjustment may be a forward-looking blunder code [17]. It works with polynomial tests of information. Polynomials have been tried in a few places and these numbers are either transmitted or recorded.

4.4 Performance analysis of EDAC Structure



In this figure 3, we have outlined as knead bits to equality check lattice at that point generator lattice and last adjusted code. To begin with, characterize codeword bits per piece, knead bits per piece, equality sub-matrix, generator lattice, and parity-check network. Encode message and discover the position of the blunder in code word (list). At that point, code alters and adjusted code. After all, evacuate blunder information at that point plot this figure 3.



In this figure 4, we have planned input and yield messages with the assistance of CRC. To begin with, we take the input and generate the network. At that point we discover checksum values. After discovering the checksum, we include a checksum to

message bits at that point we check yield is if the update is non-zero a transmission mistake has happened and update zero no blunders happened. At that point the plot yield figure 4.

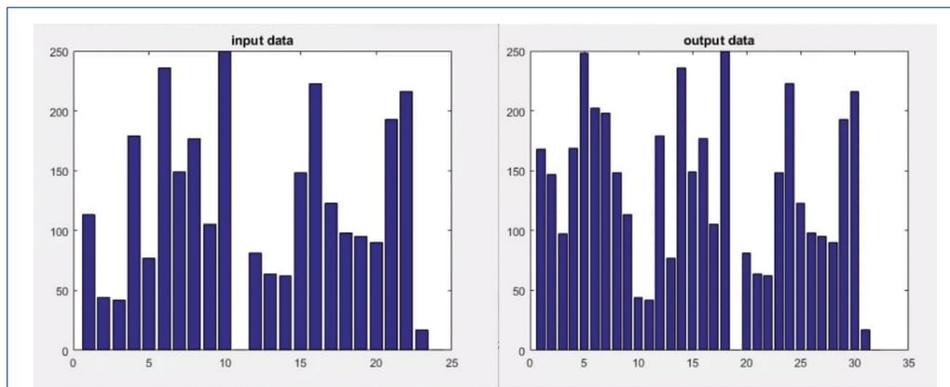


Figure 5 Performance analysis of Reed Solomon Code in Matlab

In this 5, we have outlined Reed Solomon code as input and yield messages. Reed Solomon code is utilized to adjust the burst blunders related. This code is characterized by three parameters an letter set estimate t , square length exciten, and message length k . Decoder characterizes this area utilize Reed Solomon code see of codeword as polynomial esteem is based on message encoded. The decoder recovers encoding polynomial from gotten message information in figure 5.

5 EDAC Mechanism V-1.2

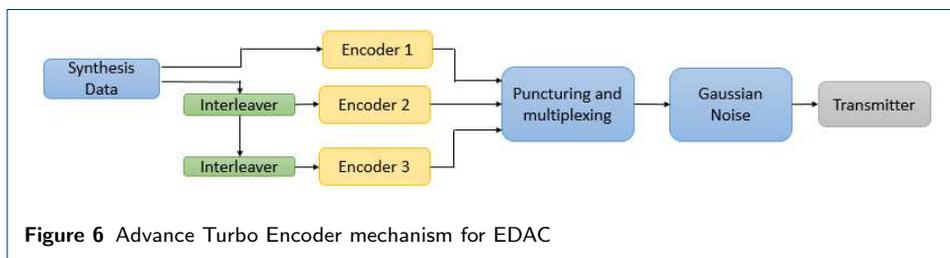


Figure 6 Advance Turbo Encoder mechanism for EDAC

5.1 Turbo Encoding Mechanism

The Turbo Encoder block uses a parallel concatenated coding scheme to encode a binary input signal[18]. Three identical convolution encoders and two internal interleavers are used in this coding scheme figure 6. An interleaver is used between systematic encoders of convolution as In Figure 6 seen. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing[19]. The process of puncturing also obtains other code rates.

5.2 Turbo Decoding Mechanism

Turbo decoder is applied when turbo encoded data is applied to transmission over the AWGN channel via Base-Band, The Log-Map decoding structure offers less

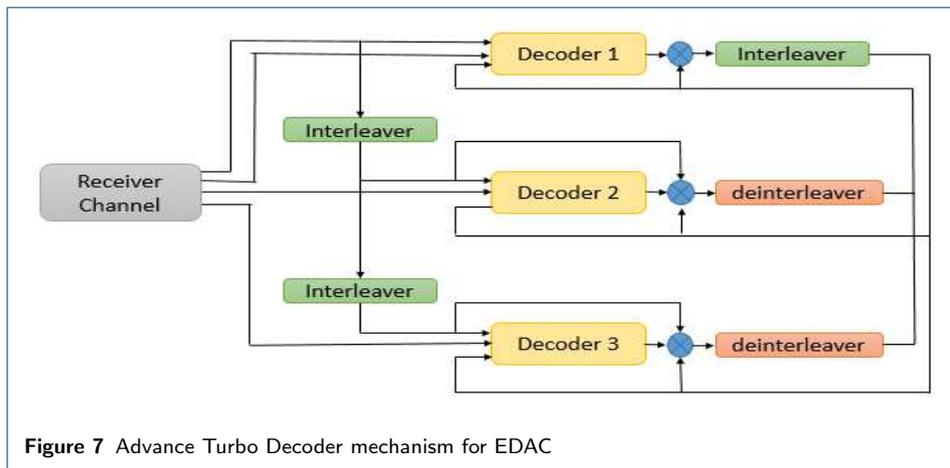


Figure 7 Advance Turbo Decoder mechanism for EDAC

complex output similar to the limit of Shannon with less complexity. Turbo decoder consists of interleaver and de-interleaver separated SISO decoders as shown in figure 7.

5.3 Additive White Gaussian Noise Channel

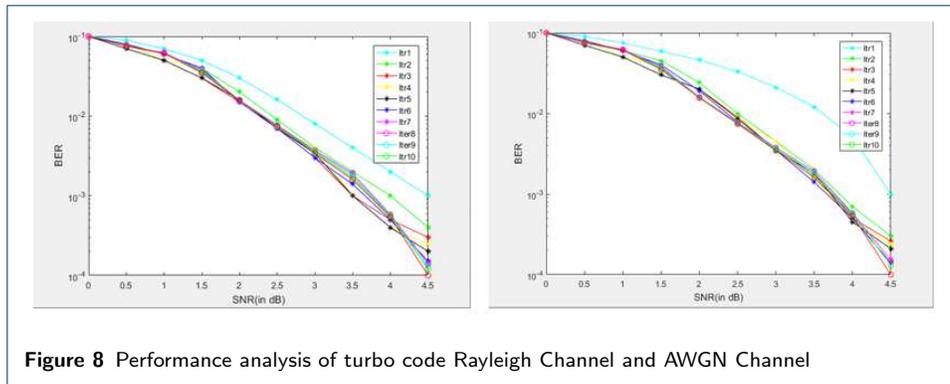
The Added substance White Gaussian Noise (AWGN) channel is one of the most commonly utilized channels that are demonstrated by large used to show an environment with an exceptionally vast number of added substance noise sources. Most added substance commotion sources in modern electronics are a coordinate result of zero-mean warm noise, which is caused by random electron movement inside the resistors, wires, and other components. The AWGN channel may be a well-known model to demonstrate the line of locate (LOS) conditions.

5.4 Rayleigh Channel

The Rayleigh blurring model is in a perfect world suited to circumstances where there are vast numbers of flag ways and reflections[20]. Common scenarios consolidate cellular broadcast communications where there’s a vast number of reflections from buildings and the like conjointly HF ionospheric communications where the uneven nature of the ionosphere suggests that the in general hail can arrive having taken various assorted ways. In this proposition, a moderate level independent Rayleigh blurring channel demonstrate is used for the blurring environment[21]. An autonomous Rayleigh blurring handle can be modeled as a steady irregular variable amid each image interim.

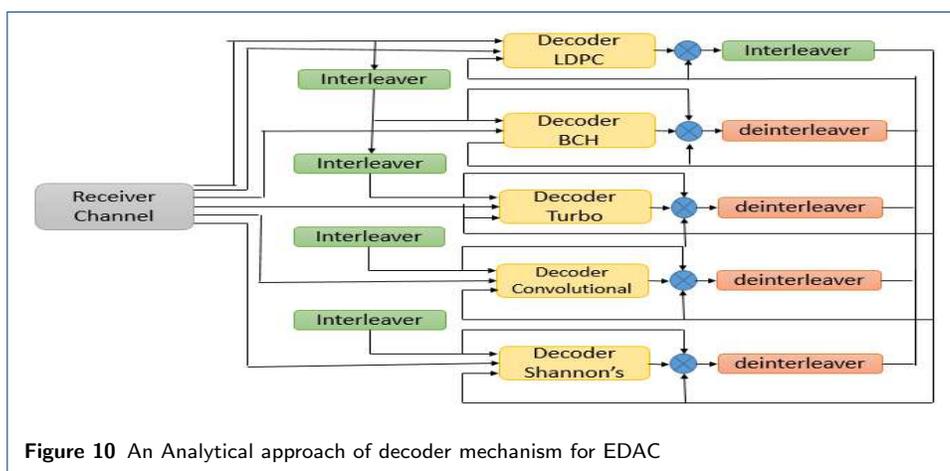
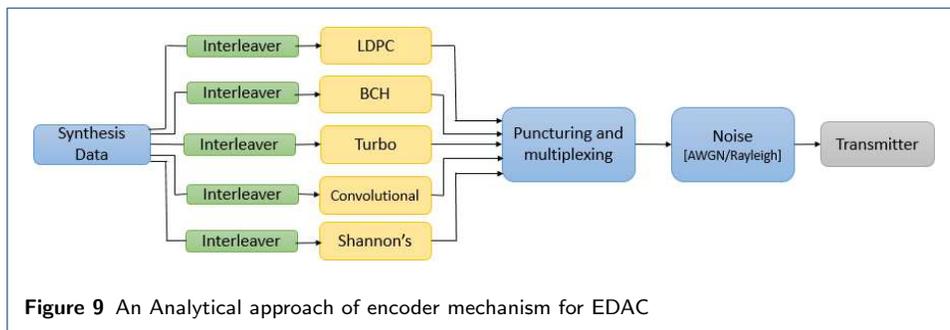
5.5 Perfomance analysis of Advance turbo mechanism

Turbo codes are better performance codes that result from the interaction of information between recursive codes and decoders of the constitution in figure 8. Turbo code simulated for Rayleigh faded channel for frame size $K = 40$. Frames number in each SNR taken as 500 to keep the simulation fast.



6 EDAC Mechanism V-1.3

Five Identical EDAC algorithms are used as encoders LDPC, BCH, Turbo, Convolutional, Shannon’s and for all the algorithms random interleaver are used in this coding scheme. Each constituent encoder is terminated by tail bits autonomously. An interleaver is used between five systematic encoders of convolution as in figure 9. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing. Other code rates are also obtained by the process of puncturing. The algorithm for decoding can be designed by either an A Probability posterior method or a method of maximum likelihood.



Decoder consists of Five interleavers and de-interleaver separated SISO decoders, shown in figure 10. Because of noise, encoded output data bit can get corrupted and entered the input of the decoder as r_0 for the device bit, r_1 for parity-1, and r_2 for parity-2, r_3 for parity-3, r_4 for parity-4, r_5 for parity-5. They are fed to the first SISO decoder with these inputs. SISO first the decoder takes the obtained data bits as input, sequence r_0 and parity sequence r_1 got, which is RSC generated encoder 1, Sequence of output results.

6.1 Low Density Parity Check(LDPC)

6.1.1 Low density parity check Encoder

LDPC code design reversible data transmitted is used to LDPC encoder and decoder. A few design methods will be considered lower the complexity of LDPC code encoding. The technique is to apply the stair code. Introducing the ladder structure can be encoded at linear times as compared to repetitive decoders in H. Only a single calculation is required to make the encoder effective by general multiplication. Design circuits perform the aspect of the Tanner graph. The same circuits use the encoding and decoding part. Such functions transfer a lot of promise in a function where the circuit area is limited.

6.1.2 Low density parity check Decoder

Best effective decoders for LDPC codes can realize by applying repeat message-passing decoders[22]. LDPC code represents by parity check matrix H . Tanner's graph is a graph presentation of LDPC, parity matrix. Tanner graph using defined sets of nodes. 1st variable nodes refer to a single bit of valid codeword x with the length of the bits. The second set represents the checking node. Constraint a flexible agreement trust extension decoder transmits the probability between checks nodes and variable nodes. This is data transfer local data using find solutions to a difficult overall complication with less complexity. However, for this type of application, it is necessary to save all the codewords that search for 2K codewords, which are increasing significantly [23]. Faith Promotion Decoder uses repeat messages to pass checks to search for codeword X and bit nodes.

6.2 performance analysis of LDPC

AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel[24]. The performance of LDPC on an AWGN channel in 11. Performance of LDPC codes 10^3 on AWGN channel at SNR = 0 dB and BRR 10^{-1} at the same SNR is not for any coding is higher than the original.

Rayleigh fading is considered the worst-case scenario as there is no effective way. Due to the functionality of the LDPC codes of the relay channel 12, multiple received signals are due to events such as reflection, scratching, and refractions[25]. For example, a comparison of curves in SNR = 5 dB implies that the code is BER 10^3 for coding and not BER 10^{-1} for no coding.

Figure 11 and 12 shows the effectiveness of LDPC codes on AWGN, Rayleigh channel. Here the curves are displayed at the same SNR = 2 dB BER, respectively 10^{-4} , 10^{-1} . The results show that the AWGN channel provides the best performance for the LDPC. It is almost impossible to encounter AWGN channels in real-life applications. In most cases, we have to consider the Rayleigh Fading system that should be built and keeping in mind the effects of the Rayleigh channel.

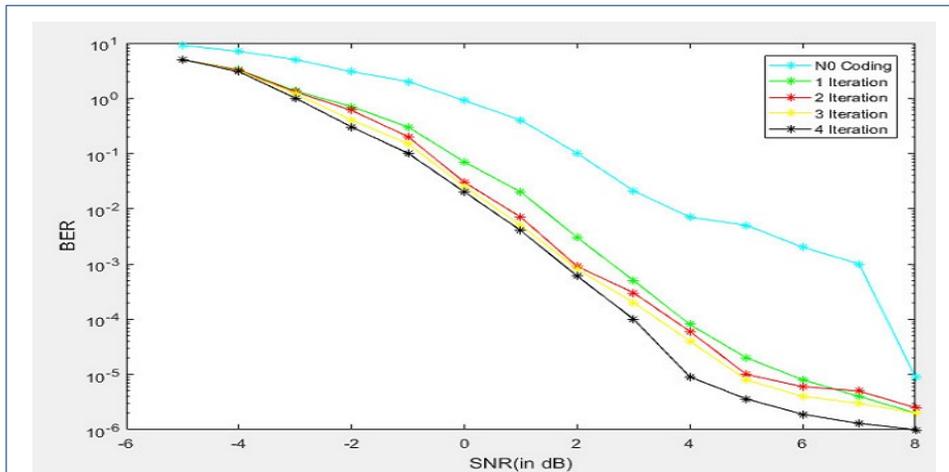


Figure 11 Performance analysis of LDPC code AWGN Channel

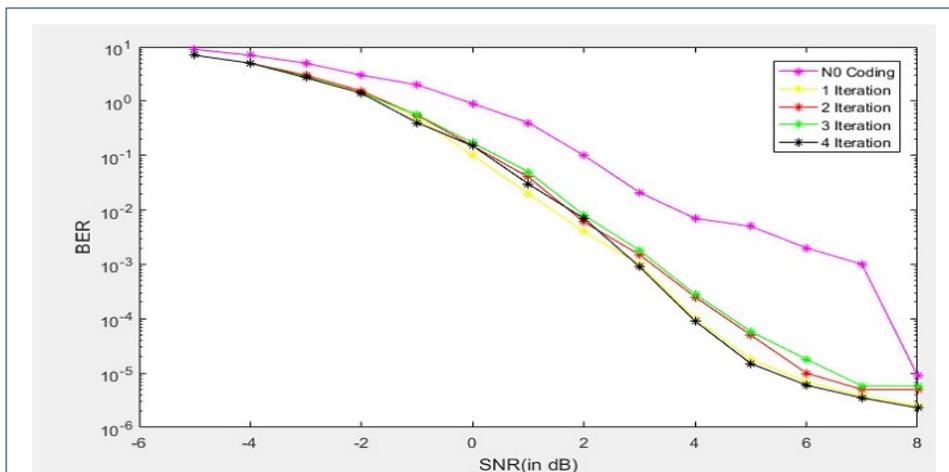


Figure 12 Performance analysis of LDPC code Rayleigh Channel

6.3 Bose Chaudhuri Hocquenghem(BCH) Codes

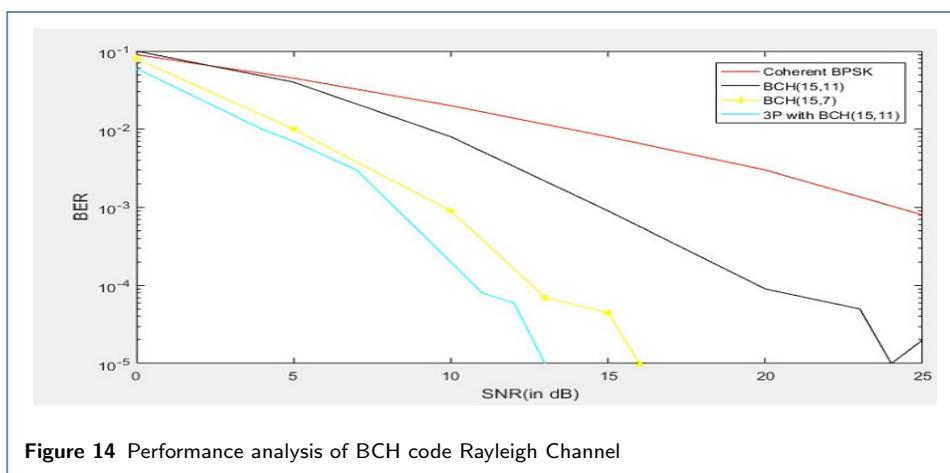
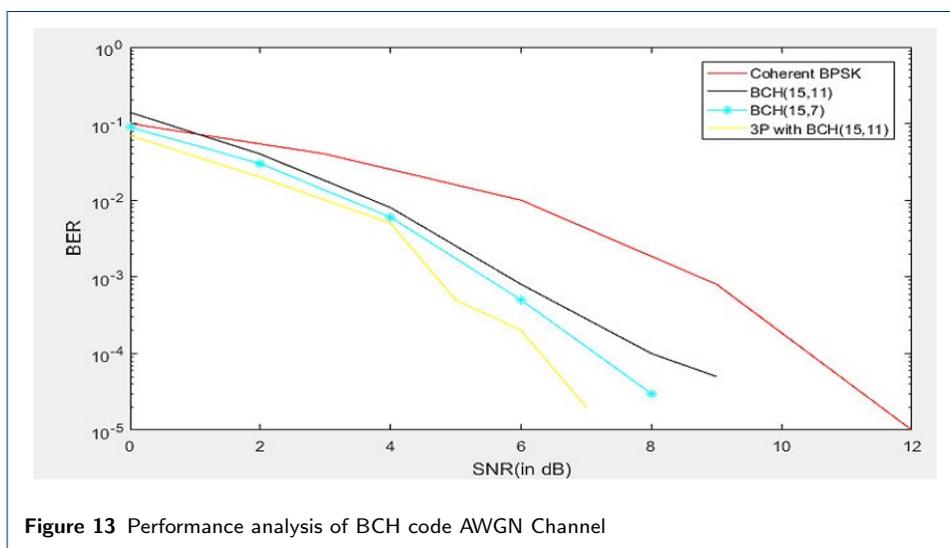
6.3.1 BCH Encoder

Codewords are shaped by including leftover portion after dividing the message polynomial with generator polynomial. They're products of the generator polynomial. On the encoding side, the generator polynomials are not ordinarily part because they will request more equipment and control circuitry. The polynomial is utilized as such for encoding[26]. The generator polynomial for BCH is given by $1 + x^3 + x^4 + x^5 + x^9 + x^{12}$ BCH codes are executed as efficient cyclic codes. Consequently, it can be effectively actualized and the rationale which actualizes encoder and decoder is controlled into move enrol circuits. The leftover portion can be calculated within the $(n-k)$ straight arrange move registers with the input association at the coefficient of the generator polynomial. LFSR is initialized with seed esteem 0.

6.3.2 BCH Decoder

The interpreting handle of the BCH codes comprises three steps. The disorder computation prepare creates $2t$ disorders from the gotten codeword which is the data information concatenated with the equality information. At that point, the blunder locator polynomial is computed from the disorders, of which the roots point out the blunder positions. Inevitably, by thoroughly finding out the roots of it utilizing the look calculation, the mistakes are adjusted. In the event it demonstrates to be no blunder within the square, we require not one or the other to assess the mistake locator polynomial nor conduct the Chien look handle. In this way, for decreasing the interpreting time, it is exceptionally important to recognize whether there's any blunder or not as early as conceivable. Here, we propose to check the mistake event with a disorder polynomial by reusing the encoder which as it were requires the GFD, whereas the routine blunder location strategy employments the disorder values which require a much longer time for conducting a few diverse CGFMs.

6.4 Performance analysis of BCH Code



13 and 14, shows the BER plots vs threshold SNR ft. for BCH code for two values of average SNR 0, 10dB and 20dB, with different Doppler frequencies. From the figures, it is clear that an increase in the performance of the BCH code occurs and for large values, the errors tend to be more random as the transition probabilities b and g increase leading to good performance since the BCH code is capable of correcting such random errors.

6.5 Convolutional Codes

6.5.1 Convolutional Encoder

Inside the encoder, data bits are input to a move enlist of length K , called the elemental length. As each bit enters at the cleared out of the select, the past bits are moved to the proper in show disdain toward of the truth that the primary orchestrated bit inside the select is evacuated. Two or more twofold summing operations, let's say r make code bits that leave inside the centre of one data stream period.

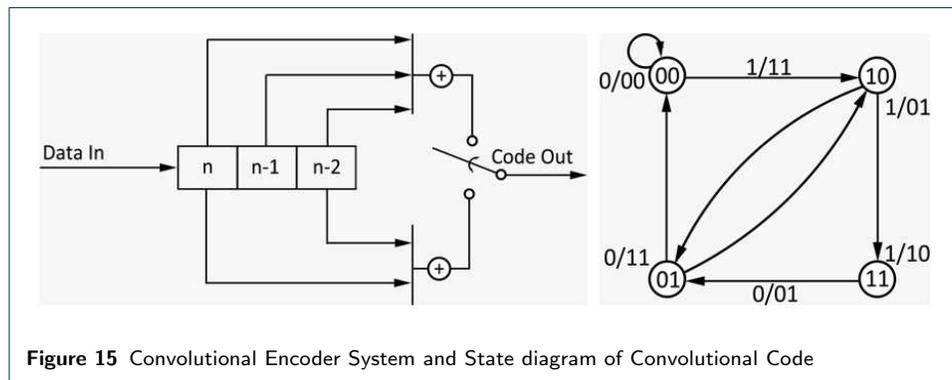


Figure 15 Convolutional Encoder System and State diagram of Convolutional Code

In this way figure 15, the code bit rate is $1/r$ times the data rate, and the encoder is called a rate $1/r$ convolutional encoder of confinement length K . Also required to completely characterize the encoder is the affiliations from stages inside the move select to the r summing squares. These are generator vectors each of which may be on a very basic level communicated as a push of K parallel digits.

6.5.2 State Diagram

Convolutional encoder shows up an outline with $K = 3, r = 2$, and the generator vectors are chosen as $[111]$ and $[11]$. Discrete looking at times are labelled n . The data stream enters on the cleared out and the show bit at time n , the first afterwards bit $n1$ and the taking after a most reliable bit at $n2$ have the move to enlist. Two balance bits are traded out inside the between times between n and $n1$ from the upper snake and after that the lower one. When the taking after data bit arrives, the move select moves its substance to the proper. The $K1$ earlier bit, in this case, two, choose the state of the encoder. They have appeared up in grey in 15.

Convolutional encoder There are 2^{K-1} states. For each encoder state, there are two conceivable comes about of yield code bits, depending on whether the input bit is zero or one. The advancement of states in time, at that point, can be a work of the information stream. The development of states in time, at that point, may well

be a work of the information stream Fig15. Each state is appeared up inside of a circle and the alter from one state to another is shown up by a jar, recognized by the input bit, cut, yield code bits.

6.5.3 Convolutional Decoder

Convolutional codes are frequently alluded to as trellis codes due to the reality that trellis charts can effortlessly portray them. The trellis chart of a code records the diverse states of the encoder and the ways they are connected to. The trellis structure for the state diagram of 16 state diagram. is appeared in 16. Trellis structure for a four-state encoder. There exist two straightforward approaches to translate a transmitted arrangement of bits.

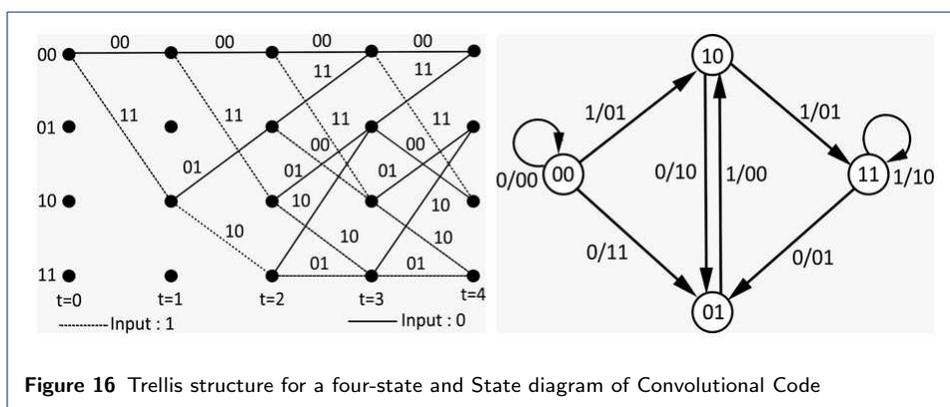


Figure 16 Trellis structure for a four-state and State diagram of Convolutional Code

The Viterbi calculation can be utilized by utilizing two primary procedures. The direct approach employments the difficult choice on the received noisy data bits by thresholding the information to parallel digits and after that applying the calculation. In contrast, the moment approach employments delicate choice to translate the lead by finding the way among all the ways of the trellis which has the most significant matrix.

6.6 performance analysis of Convolutional code

For the event, at an SNR regard of 5dB, a bit botch rate of 10^{-5} . was getting. That's, in this regard, 1 bit gotten in a blunder for 100000 bits sent. This was far off predominant to when the SNR was 2dB with a bit bumble rate of 10^{-1} . That's 1 bit gotten in botch when 10 bits were sent. For the theoretical BER, the SNR ranges of 2dB, 2.5dB, and 3dB had a bit botch rate of 10^{-1} whereas inside the mirrored BER the SNR was observed to be of the expand 2dB, 2.5dB and had the same regard of BER of 10^{-1} whereas the SNR of 3dB of the imitated BER had an advanced BER of 10^{-2} . This was as a result of the convolution coding displayed. Another characteristic was gotten by considering the incline of the hypothetical and imitated regard gotten as in 17 and 18.

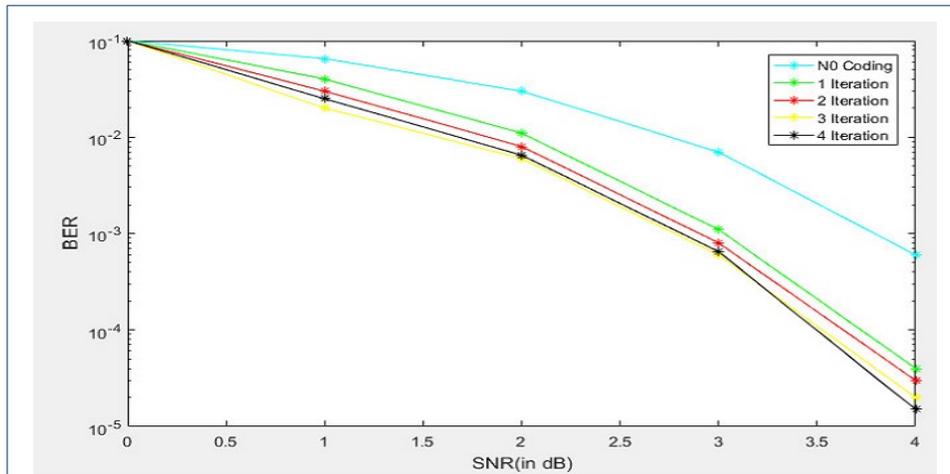


Figure 17 Performance analysis of Convolutional code AWGN Channel

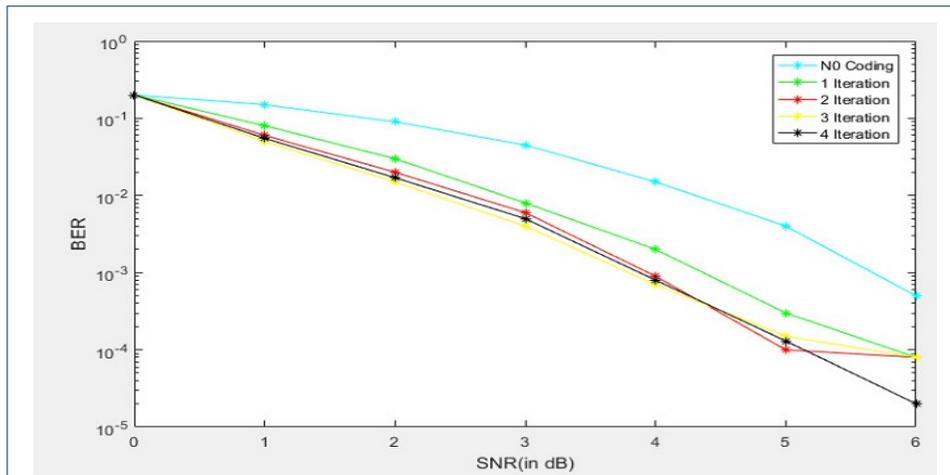


Figure 18 Performance analysis of Convolutional code Rayleigh Channel

6.7 Shannon's Theorem

6.7.1 Shannon's Encoding

The included repetition increments the length of the flag but permits for a more prominent location and adjustment of mistakes amid the translating preparation. Common causes of channel coding incorporate the utilization of equality check bits and redundancy codes. An equality check bit is essentially an additional bit that's included in a twofold sequence such that there's an indeed number of 1's. If an arrangement with an odd number of 1's is gotten, at that point, the decoder can identify that a blunder has happened amid transmission through the channel.

6.7.2 Shannon's Decoding

The yield of the channel is at that point gotten by a decoder, which attempts to change over the gotten flag back to the first message. At that point, at long last, the yield of the decoder is sent to the ultimate client or goal, which is alluded to as the data sink [27]. We speaks to a message. We'll regularly consider that it is the

yield of the compressor. The encoder gets W and encodes it to X_n . The encoder puts X_n into the channel and Y_n is the yield the decoder gets. At long last, the decoder tries to appraise W through Y_n . The decoders appraise is signified by W_c . Our objective is to get what kind of encodings are such that W_c is the same as W with tall likelihood and n is as little as conceivable.

6.8 Performance Evaluation of shannon's theorem

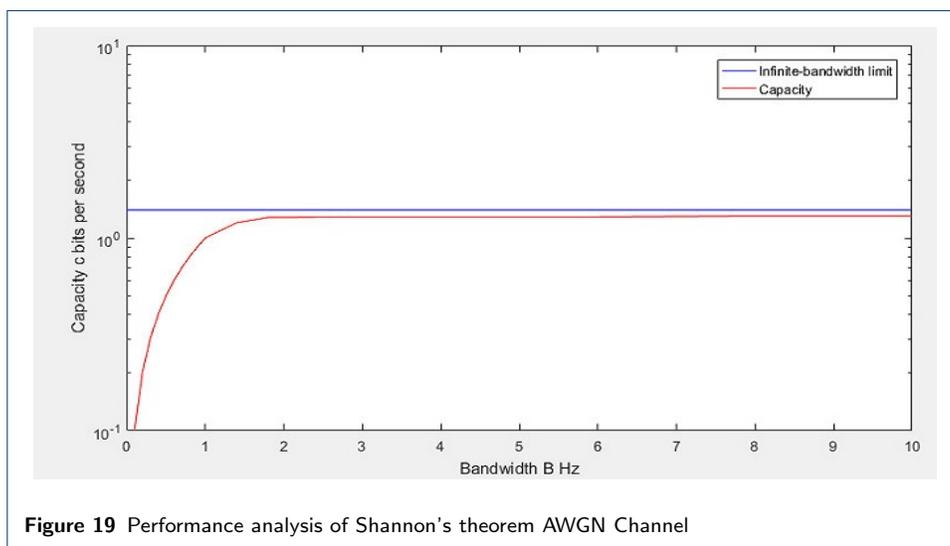


Figure 19 Performance analysis of Shannon's theorem AWGN Channel

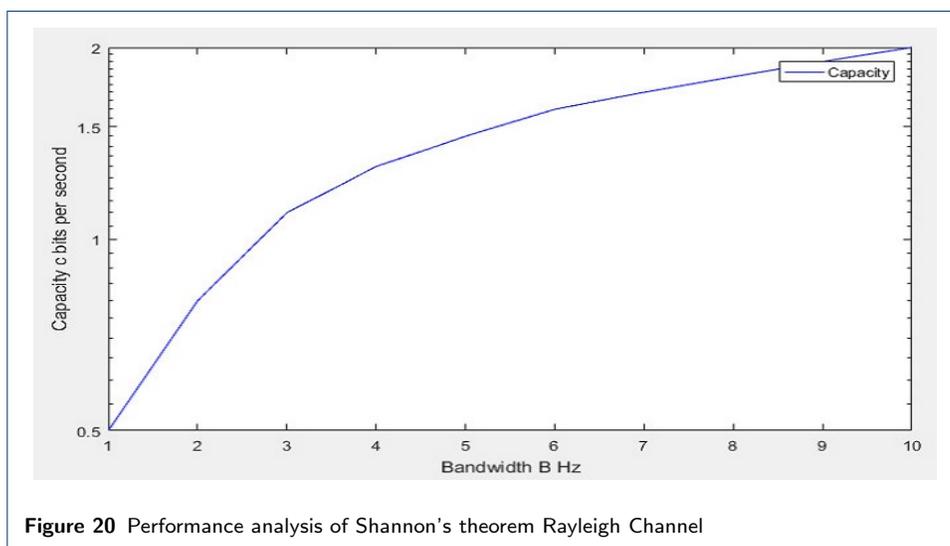
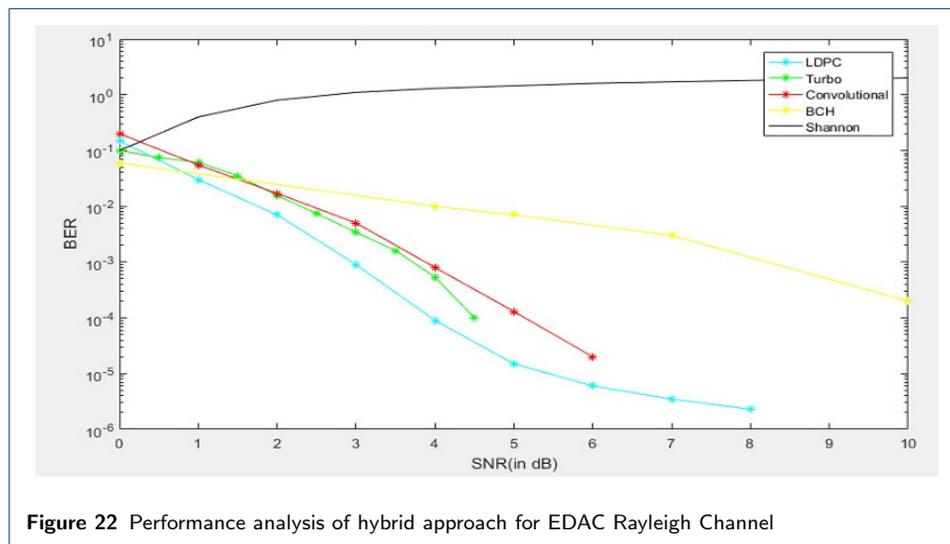
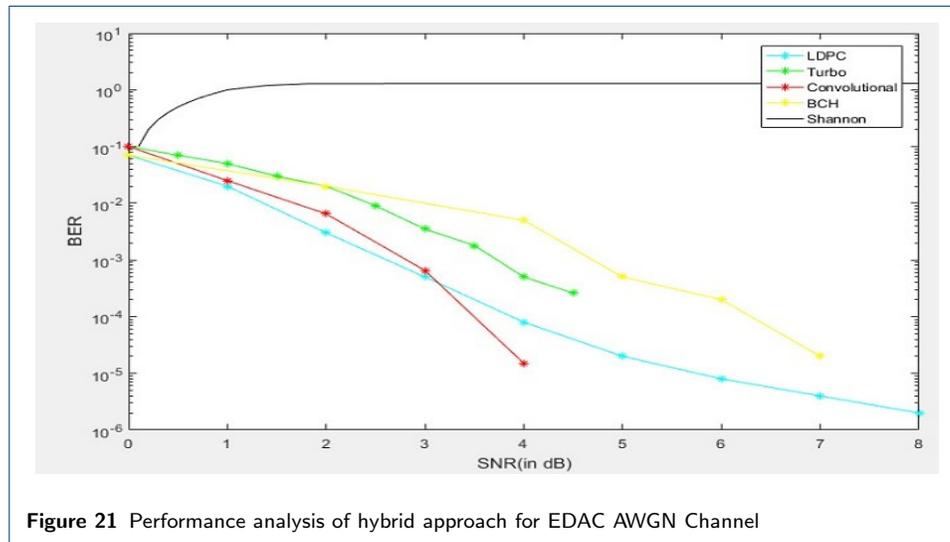


Figure 20 Performance analysis of Shannon's theorem Rayleigh Channel

In this figure 19 and figure 20, AWGN Channel and Rayleigh fading we have used Shannon Theorem. Higher theory a scale that can be loaded with a BER, with an enabled central signal, above the B Hz bandwidth affected by the channel. By the term “unfairly BER” means that it has provided conditions for the theorem is met, in any given BER, no matter how small, we can find the coding process that benefits this BER the smaller the BER given, the harder it will be processed. The least accessible bit rate is called channel capacity C . S / N is a square signal that

means the sound ratio, and the logarithm is in base 2.

7 Results and Discussion



In analytical figure 21 and figure 22, we apply two types of noise Rayleigh Channel and AWGN channel for all algorithms. AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel. Rayleigh fading is considered the worst-case scenario as there is no effective way. Here we can see that LDPC, Turbo, Convolutional, BCH, and Shannon's Theorem this algorithms are best performing for different types of data. Some algorithms are good for fewer data and some algorithms are better for more data. LDPC works better when signal noise is increasing. Convolutional code works best when signal noise is medium and bit error ratio 10^{-3} .

LDPC works better for the AGWN channel. We transmitted data continuously in

machine learning techniques and which type of data is best for which algorithms and identify more error data and remove error data in less time.

8 Limitation and Future Work

We used multiple algorithms to less data transmission error but there was some limitation of these algorithms, like An LDPC cannot detect all types of bits errors. LDPC adds to extra bits per conversation that have been transmitted through the satellite data transmission system. Turbo code affects single bit error correction and also detects multiple bit errors. If numerous bit error detection is in this code but turbo code can only solve single bits error correction. A BCH is not suitable for security purposes. BCH is more complex than a checksum and takes more processing. A strong BCH might run slowly in software. But Reed Solomon codes are not efficient as BCH codes. It cannot provide satisfying performance without BCH codes in BPSK modulation schemes.

In the future, we will introduce an advanced error detection method based on satellite transmitted data. Depending on data size, type, and importance detection algorithms will be changed. It will reduce the time of the EDAC process and get reliable safe data in a faster way. Predicted the less error mechanism in a different type of data. We will use the machine learning technique to find fewer error paths. We were implementing the ASCI architecture in Spartan 6 FPGA. After all, we collaborated on our system architecture with Bangabandhu Satellite-1 to have a more secure and faster data transmission.

9 Conclusion

In this paper, we focused on different EDAC techniques and code correlation to the study has been regulated. This application came up with the editor's good concern of all regular EDAC techniques. This paper represents an analytical approach to EDAC algorithms for nanosatellite data transmission systems. The prototype can be expanded or EDAC of multiple bits defects by using other more complicated error detecting and error-correcting codes. The ground station of nanosatellites is continuously maturing and growing in an impressive way. This is scheduled for the law that gives a plan of action from which the perimeters of space and technology are regularly being forced. The automation progresses memory chip cell architecture is becoming more and more solid, principally with the evolution of nanotechnology.

Abbreviations

EDAC: Error Detection and Correction; FPGA: Field Programmable Gate Array; AWGN: Additive White Gaussian Noise; EO: Earth Observation; LDPC: Low Density Parity Check; BCH: Bose Chaudhuri Hocquenghem; LEO: Low Earth Orbit;

Declarations

Availability of data and materials

The data set used and/or analysed during the current study are available from the corresponding author on reasonable request.

Competing interests

The authors declare that they have no competing interests.

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Authors' contributions

All authors contributed to the study conception and design. Data collection was done by MH. Methodology design were done by MH and MI. Original draft preparation including review and editing was done by MH. The study was supervised by MI. Both authors read and approved the final manuscript.

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Ethics approval and consent to participate

Not applicable.

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References

- Al Mamun, R., Islam, M.M., Tajrin, R., Noor, N., Qader, S.: Error detection and correction for onboard satellite computers using hamming code. *International Journal of Electronics and Communication Engineering* **14**(9), 251–257 (2020)
- Hillier, C., Balyan, V.: Error detection and correction on-board nanosatellites using hamming codes. *Journal of Electrical and Computer Engineering* **2019** (2019)
- Friedman, D.E.: Error control for satellite and hybrid communication networks. PhD thesis (1995)
- Pakartipangi, W., Darlis, D., Syihabuddin, B., Wijanto, H., Prasetyo, A.D.: Analysis of camera array on board data handling using fpga for nano-satellite application. In: 2015 9th International Conference on Telecommunication Systems Services and Applications (TSSA), pp. 1–6 (2015). IEEE
- Hanafi, A., Karim, M., Latachi, I., Rachidi, T., Dahbi, S., Zouggar, S.: Fpga-based secondary on-board computer system for low-earth-orbit nano-satellite. In: 2017 International Conference on Advanced Technologies for Signal and Image Processing (ATSIP), pp. 1–6 (2017). IEEE
- Ibrahim, M.M., Asami, K., Cho, M.: Reconfigurable fault tolerant avionics system. In: 2013 IEEE Aerospace Conference, pp. 1–12 (2013). IEEE
- Celis, J.A.P., de la Rosa Nieves, S., Fuentes, C.R., Gutierrez, S.D.S., Saenz-Otero, A.: Methodology for designing highly reliable fault tolerance space systems based on cots devices. In: 2013 IEEE International Systems Conference (SysCon), pp. 591–594 (2013). IEEE
- George, A.D., Wilson, C.M.: Onboard processing with hybrid and reconfigurable computing on small satellites. *Proceedings of the IEEE* **106**(3), 458–470 (2018)
- Banu, R., Vladimirova, T.: On-board encryption in earth observation small satellites. In: Proceedings 40th Annual 2006 International Carnahan Conference on Security Technology, pp. 203–208 (2006)
- Banu, R., Vladimirova, T.: Fault-tolerant encryption for space applications. *IEEE Transactions on Aerospace and Electronic Systems* **45**(1), 266–279 (2009)
- Bentoutou, Y.: A real time edac system for applications onboard earth observation small satellites. *IEEE Transactions on Aerospace and Electronic Systems* **48**(1), 648–657 (2012)
- Wang, B., Zhang, Q.: Study of performance comparison of satellite error correction codes for correcting big burst data errors. In: 2018 IEEE 3rd International Conference on Big Data Analysis (ICBDA), pp. 254–258 (2018). IEEE
- Gao, N., Xu, Y., He, D., Zhang, G., Zhang, W.: Design of ldpc codes for joint satellite and terrestrial broadcasting system. In: 2018 IEEE International Symposium on Broadband Multimedia Systems and Broadcasting (BMSB), pp. 1–6 (2018). IEEE
- Liu, Y., Guan, Y., Zhang, J., Wang, G., Zhang, Y.: Reed-solomon codes for satellite communications. In: 2009 IITA International Conference on Control, Automation and Systems Engineering (case 2009), pp. 246–249 (2009). IEEE

15. Chen, M., Xiao, X., Li, X., Yu, J., Huang, Z.R., Li, F., Chen, L.: Improved ber performance of real-time ddo-ofdm systems using interleaved reed-solomon codes. *IEEE Photonics Technology Letters* **28**(9), 1014–1017 (2016)
16. Yu, C., Su, Y.-S.: Two-mode reed-solomon decoder using a simplified step-by-step algorithm. *IEEE Transactions on Circuits and Systems II: Express Briefs* **62**(11), 1093–1097 (2015)
17. Lu, E.-H., Chen, T.-C., Lu, P.-Y.: A new method for evaluating error magnitudes of reed-solomon codes. *IEEE Communications Letters* **18**(2), 340–343 (2014)
18. Ali, S.A.: Performance analysis of turbo codes over awgn and rayleigh channels using different interleavers. PhD thesis, Eastern Mediterranean University (2001)
19. Wang, Z., Chini, A., Kilani, M.T., Zhou, J.: Multiple-symbol interleaved rs codes and two-pass decoding algorithm. *China Communications* **13**(4), 14–19 (2016)
20. Rhee, D.J., Rajpal, S., Lin, S.: Some block-and trellis-coded modulations for the rayleigh fading channel. *IEEE transactions on Communications* **44**(1), 34–42 (1996)
21. Li, J., Bose, A., Zhao, Y.Q.: Rayleigh flat fading channels' capacity. In: 3rd Annual Communication Networks and Services Research Conference (CNSR'05), pp. 214–217 (2005). IEEE
22. Wang, H.: The ldpc code and rateless code for wireless sensor network. In: 2019 2nd International Conference on Safety Produce Informatization (IICSPI), pp. 389–393 (2019). IEEE
23. Hou, J., Siegel, P.H., Milstein, L.B.: Performance analysis and code optimization of low density parity-check codes on rayleigh fading channels. *IEEE Journal on Selected areas in Communications* **19**(5), 924–934 (2001)
24. Pang, X., Yang, C., Zhang, Z., You, X., Zhang, C.: A channel-blind decoding for ldpc based on deep learning and dictionary learning. In: 2019 IEEE International Workshop on Signal Processing Systems (SiPS), pp. 284–289 (2019). IEEE
25. Chy, D.K., Khaliluzzaman, M.: Evaluation of snr for awgn rayleigh and rician fading channels under dpsk modulation scheme with constant ber. *International Journal of Wireless Communications and Mobile Computing* **3**(1), 7–12 (2015)
26. Hasan, M.Z., Akbar, M.A., Mahmood, I.: Performance analysis of (63, 56) bch code using multipath rayleigh fading channel on spartan-3 fpga. In: 2008 2nd International Conference on Advances in Space Technologies, pp. 69–73 (2008). IEEE
27. Somekh, O., Shamai, S.: Shannon-theoretic approach to a gaussian cellular multiple-access channel with fading. *IEEE Transactions on Information Theory* **46**(4), 1401–1425 (2000)