Analysis of optical and thermal properties of 940-nm vertical-cavity surface-emitting lasers

Congcong Wang (✉ wangcc@ihep.ac.cn)

Institute of High Energy Physics Chinese Academy of Sciences

Chong Li

Beijing University of Technology

Zhiyong Wang

Beijing University of Technology <https://orcid.org/0000-0002-8751-9432>

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Abstract

We achieve 13.5mW optical output power, 48% power conversion efficiency, 1.17 W/A slope efficiency and 17kW/cm² laser power density with top-surface-emitting 940 nm oxide-confined vertical-cavity surface-emitting laser (VCSEL). The physical mechanism of minimum threshold current generation in oxide-confined VCSEL has been thoroughly studied theoretically and experimentally. Further, we also succeeded in 90.8mW optical output power, 40% power conversion efficiency with 2×4 VCSEL arrays. We find an increase in output power and PCE of 2×2 VCSEL arrays as we increase the array spacing which we attribute primarily to increased heat dissipation and reduced thermal crosstalk between the emitters. Thermal properties in oxide-confined 2×2 VCSEL arrays were analyzed numerically and experimentally. The simulated results are in good agreement with the measurement. It is proved that theoretical simulation is very useful for the future device optimization.

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) have advantages of symmetrical laser beam, low threshold, high-speed modulation, single longitudinal mode, lack of catastrophic optical mirror damage (COMD), and simple arrangement in two dimensional arrays(Chuyu et al. 2017; Lu et al. 2015; Seurin et al. 2010; Larisch et al. 2016; Seurin et al. 2016; Tatsuo Hariyama et al. 2018). They have been used in optical interconnect, high-speed local-area networks parallel links, Gigabit Ethernet, atomic clock system, free-space data transmission, laser pumping and illumination field. Moreover, 940-nm VCSELs have been innovatively applied in the fields of three-dimensional (3D) face recognition, laser radar, automobile auxiliary driving, artificial intelligence robot and virtual reality/augmented reality (VR/AR) (Tatsuo Hariyama et al. 2018; Yong-Qin et al. 2011; Shichijo,Miyamoto 2019; Nazaruk et al. 2014). In laser pumping, laser radar, 3D sensing, illumination and other highly integrated fields need VCSEL with high output power and photoelectric conversion efficiency (PCE). In some extreme temperature conditions, temperature changes will seriously affect the performance of VCSELs. Extensive application in optical fiber sensing and core chip atomic clock system, require VCSELs with low threshold, wavelength stability and low temperature sensitivity(Derebezov et al. 2010; Nishikata et al. 2005; HuiQing et al. 2004; Tong 2005).

Some scholars have studied the output power, PCE, beam quality and working stability of VCSEL. Moench H et al. reported the 808-nm VCSEL array combination with the photoelectric conversion efficiency (PCE) of up to 40% and output power of 9.6kW(Moench et al. 2014a; Moench et al. 2014b). Zhou D. L. et al investigated the 980-nm VCSEL array combination with photoelectric conversion efficiency of up to 40% and output power of 14kW(Zhou et al. 2015b; Zhou et al. 2014). Osram

power of 1W(Iga,Kenichi 2018). Meng Xun et al. studied the 940-nm VCSEL array with output

developed the 940-nm VCSEL array with electro-optic conversion efficiency of up to 35% and output power of 210mW(Meng Xun et al. 2021). Compared with the 808-nm and 980-nm VCSEL array, the

performance of 940-nm VCSEL array is relatively poor. The internal thermal and thermal crosstalk effect of the VCSEL array is one of the most significant factors, which affect the output power and PCE. A high temperature will reduce the output characteristics and lifetime of VCSEL array. Heat sources of VCSEL consist of two parts: joule heating of DBR (especially P-DBRs) and heating of the active region. Compared with 808-nm VCSEL array, 940-nm VCSEL array produces more heat due to more P-distributed Bragg reflectors (DBRs). What is more serious is that top-emitted 940-nm VCSEL array has poor cooling effect compared with the bottom-emitted 980-nm VCSEL array.

In this paper, our main attention will be focused on the photoelectric properties of 940-nm VCSEL and its arrays. Firstly, temperature dependence of threshold current, the output power and electro-optic conversion efficiency (PCE) of VCSEL were studied, and the mechanism of the minimum threshold current was analyzed in detail. Then, the output power and PCE of 2×2 VCSEL arrays with different arrays spacing ($d=160\mu\text{m}$, $180\mu\text{m}$ and $200\mu\text{m}$) were systematically analyzed. In addition, 3D thermoelectric coupling models were established based on finite element analysis to investigate the thermal distribution of 2×2 VCSEL arrays.

2. Fabrication

The GaAs-based 940nm VCSEL epitaxial structure consists of 23 pairs $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}/\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ layers for the P-DBRs and 32 pairs $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}/\text{AlAs}$ layers for the N-DBRs. The active region includes three strained 4.4-nm-thick $\text{In}_{0.16}\text{Ga}_{0.84}\text{As}$ quantum wells (QWs) and four 6.2-nm-thick strain-compensating $\text{GaAs}_{0.92}\text{P}_{0.08}$ barriers. The QWs with high In-content for wavelength extension and strain compensating $\text{GaAs}_{0.92}\text{P}_{0.08}$ barriers for compressive strain in the QWs for high differential gain (Simpanen et al. 2019). Carriers and photons are well-confined along the transverse direction by a 30nm thick $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ oxide aperture on the P-DBRs. The top-emitted 940-nm VCSEL array chip fabrication is as follows. First, etched circular top mesas just through the optical cavity with $\text{Cl}_2 + \text{BCl}_3$ in an inductively coupled plasma (ICP) reactive ion etching to expose high Al content layer. Then oxide aperture ($\Phi = 10\mu\text{m}$) was formed by the selective wet oxidation of $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ to Al_2O_3 at temperature of 430°C . Ti/Au metal contact was deposited on the top of wafer by using electron beam evaporation system. SiN layer was deposited to form an insulating layer. After the GaAs substrate was thinned to $150\mu\text{m}$, the Ni/Au/Ge/Ni/Au metal contact was deposited on the bottom of wafer by using measurement and control sputtering system. Finally, the contacts were rapidly annealed at 435°C . Figure. 1 shows the sectional diagram of VCSEL array.

3. Results And Discussion

The VCSEL arrays were tested on a probe station using a semiconductor parameter analyzer (Keithley 4200), a high precision current source (Keithley 2430), a laser beam profiler (Spiricon SP928), a power meter (Thorlabs S120C) and a spectrograph (Yokogawa AQ6370D). A thermo electric cooler (TEC) can control the temperature vary from -30°C to 40°C . Figure. 2 shows schematics of experiment setup in our

experiment. All the performance parameters of VCSELs are obtained by on-chip test under continuous wave condition without extra heat dissipation solution.

Figure 3(a) showed the temperature-dependent threshold currents (I_{th}) and slope efficiency for top-emitting VCSEL. And the relationship of threshold currents and temperature meets the parabolic equation (1). Under the same condition of injection current, operating temperature affects the threshold current and slope efficiency. As the operating temperature rises, the internal temperature of the device increases, which results in a reduction in output power and power conversion efficiency (PCE). As is shown in the figure. 3(a), the threshold current decreases at first and then increases as the temperature increases in the case-temperature range from -30 °C to 40°C. The minimum threshold currents ($I_{th, min}$) of 10-μm oxide aperture VCSEL was 0.995mA, when the environment temperature was 20°C.

$$I_{th}(T) = I_{th, min} \times \left[1 + C_T (T - T_{min})^2 \right] \quad (1)$$

where C_T is a constant, $C_T=9.16 \times 10^{-5}$; T_{min} is the temperature of the minimum threshold current, $T_{min}=19.3^\circ\text{C}$; $I_{th, min}$ is the minimum threshold current, $I_{th, min}=1\text{mA}$; $I_{th}(T)$ is the threshold current in different temperature (T).

The mode wavelength (MW) and gain peak wavelength (GPW) of VCSEL are two main factors that affect the threshold current of VCSEL. In order to study the physical mechanism of VCSEL threshold current generation, the reflection spectrum of DBR (contains P-DBR and N-DBR) and gain spectrum of active region were simulated using TFCalc and Crosslight software under the operating temperature of -30°C ~ 40°C. The reflectivity spectrums were calculated by transfer matrix method. Among them, the minimum point in the reflection spectrum corresponds to the resonance condition, so the mode wavelength can be obtained from the reflection spectrum of VCSEL(Wang et al. 1995).

Figure. 3(b) showed the mode wavelength (MW) and gain peak wavelength (GPW) of the 10μm VCSEL (10mA) under the operating temperature of -30°C ~ 40°C. With the increase of temperature, the mode wavelength and gain peak wavelength of VCSEL were redshift. The redshift rate of mode wavelength is 0.0557 nm/°C. As is known, the mode wavelength of a VCSEL is determined by the cavity resonance due to the short optical resonator. The wavelength shift mainly depends on changes of the average refractive index in the resonator(Michalzik 2013). The redshift rate of gain peak wavelength is 0.33 nm/°C. As the temperature increases, the crystal lattice constant increases. This leads to a weakening of the binding effect of the valence electron period potential. The energy required for the valence electron transition decreases and the band gap shrinks. Bandgap shrinkage causes gain peak wavelength redshift. The peak gain decreases as the temperature increases, due to electron occupancy probability near the Fermi level is smoothness. A minimum threshold current of a VCSEL value exists, when the gain wavelength is the same as the mode wavelength at a temperature of 20°C, due to temperature-dependent gain and mode wavelength shifts. The physical mechanism of VCSEL threshold current generation was verified by combining theory and experiment.

Figure. 4 showed the measured (a) temperature-dependent power, current, voltage (P-I-V) and (b) PCE characteristics of 10 μ m VCSEL. As is shown in figure. 4(a), the maximum output power is 13.5mW at -30°C and decreases to 9.6mW at 40°C. The slope efficiency is 1.17 W/A at -30°C and decreases to 0.98 W/A at 40°C. With the temperature increases, electron hole non-radiative recombination especially auger recombination is strengthened. More electric energy is released in the form of phonons, internal losses increasing with the temperature, which leads to a decrease of the differential efficiency and output power. Lower carrier concentration and higher carrier mobility can reduce the differential resistance. With the increase of temperature, the carrier concentration in the active region increases, and the probability of collision between carriers and ionized impurities increases, which leads to the decrease of carrier mobility. Temperature-dependent I-V curve means that the differential resistance of VCSEL was decreased with temperature increasing. This result indicates that the main factor determining differential resistance of VCSEL is the carrier concentration in the active region, and the secondary factor is the carrier mobility.

As is shown in figure. 4(b), when the injection current is about 5mA, the PCE reaches the maximum value. Among them, the highest efficiency can reach 48% at 20°C. When the injection current is about 13.5mA, laser power density is up to 17kW/cm² at -30°C. To examine the beam property, the far-field patterns of the VCSEL at 20°C were measured at a distance of 50 mm from the VCSEL surface by a laser beam profiler. The far-field beam profile is symmetric and the intensity is near uniform, the far-field divergence angle is 23° at 13.5 mA.

Through the above experiments, we found that 10- μ m oxide aperture VCSEL has higher electro-optical conversion efficiency and power density, but overall output power was low. In order to improve the output power of VCSELs, the photoelectric performances of 2×2 and 2×4 VCSEL arrays with oxidation aperture of 10 μ m were studied systematically.

Figure. 5 shows the output power and PCE of 2×2 VCSEL arrays. As the VCSEL array spacing (d) is 200 μ m, the maximum PCE was 47.2% at -30 °C and decreased to 40.06% at 40 °C; the maximum power was 48.72mW at -30 °C and decreased to 32.93% at 40 °C. Full width half maximum (FWHM) was 1.05nm at -30 °C and decreased to 1.42nm at 40 °C, respectively. The spectral broadening rate is only 0.0053nm/°C. The beam distribution is relatively uniform, and the divergence angle is about 20°. With increasing temperature and the decrease of the array spacing, the output power and PCE show a downward trend. The main cause of this phenomenon is heat accumulation caused by thermal resistance effect. In addition, in order to increase the power of the VCSEL array, the 2×4 VCSEL array (d=200 μ m) was prepared, and the maximum power and PCE were 90.8mW and 40% at -30 °C, respectively. The spectral broadening rate is 0.007nm/K. The above measured data conform that device exhibited superior adaptability to high and low temperatures operation characteristics.

In order to analyze the thermal effect of VCSEL, its thermal resistance of can be obtained from the emission spectra and dissipated power. The thermal resistance equation (2) is(Zhou et al. 2015a)

$$R_{th} = \frac{\Delta T}{\Delta P_{diss}} = \frac{\Delta \lambda / \Delta P_{diss}}{\Delta \lambda / \Delta T_a} \quad (2)$$

ΔP_{diss} is the dissipated power. The dissipated power is equal to injected electrical power subtracting output optical power. $\Delta \lambda / \Delta P_{diss}$ is calculated by variation of the wavelength shift with the variation of the dissipated power (Zhou et al. 2015a). $\Delta \lambda$ is the wavelength shift rate, ΔT_a is the varied ambient temperature.

The thermal resistance was obtained by analyzing the experimental photoelectric performance parameters of 2×2 VCSEL array (d=200μm). Fig. 6(a) shows the measured temperature-dependent emission wavelength, the wavelength shifts with ambient temperature linearly by a rate of 0.054 nm/°C. The relationship between peak wavelength and dissipated power is shown in Fig. 6(b), which obtained by measuring the emission spectra under different injection currents at ambient temperature of 20 °C. When the injection current was 40mA, $\Delta \lambda / \Delta P_{diss}$ is 0.028 nm/mW. The dissipated power (P_{diss}) is 70mW. According to (2), the thermal resistance is 0.515 °C/mW. The equation of actual temperature in active region (T_{ac}) is as follows: $T_{ac} = T_a + R_{th} P_{diss}$. In this case, the actual temperature in active region is 56.04 °C.

In order to analyze the thermal distribution of 2×2 VCSEL arrays (d=160μm, 180μm and 200μm), a 3D thermoelectric coupling model based on finite element analysis was established by COMSOL Multiphysics. In this model, the equivalent structure method is adopted to simulate the VCSEL structure, whose structure mainly includes: P-DBR, active region, N-DBR and GaAs substrate. Joule heat and heat generation in active region are two main sources of VCSEL heat generation. The resistance is generated by the VCSEL heterojunction barrier structure and the parasitic resistance of the VCSEL array, interact with the current to produce a large amount of joule heat. The carrier injection, carrier leakage, carrier recombination and absorption loss occurring in the active region will generate a large amount of heat, which becomes the main heat source of the active region. In this model, the ambient temperature is set to 20°C and the injection current of each light source is set to 10mA.

Figure. 7 shows the simulated temperature distributions and temperature curve along A-A' cut-line in active region. As is shown in Fig. 7, the maximum temperatures in active region were 63.1 °C @160μm, 59.1°C@180μm and 55.9°C@200μm, respectively. When the array spacing is 200μm, the simulation results are consistent with the actual results, which proves the correctness of the simulation results. According to the above experimental results, optimizing the thermal accumulation of devices can improve the output power and PCE. Therefore, in order to obtain high-power VCSEL, it is necessary to optimize the epitaxial structure, such as reasonably increasing doping concentration, designing gradual DBR structure and reduce the pairs of DBRs. The DBRs have gradient composition interfaces and are modulation doped for efficient transport of carriers across the interfaces and low internal optical loss(Simpanen et al. 2019). In order to improve the heat dissipation performance of the device, the device can use the 3D micro-channel heat sink of tungsten copper alloy with Pin Fin structure to conduct water cooling heat dissipation.

4. Conclusion And Perspectives

In summary, the physical mechanism of minimum threshold current generation in oxide-confined VCSEL has been thoroughly studied theoretically and experimentally. That is, the threshold current reaches the minimum value when the mode wavelength matches the gain wavelength. VCSEL with an oxide aperture diameter $\varphi \sim 10 \mu\text{m}$ exhibit 13.5 mW operating optical output power and 1.17 W/A slope efficiency at -30°C . And its highest PCE and laser power density are up to 48% at and $17\text{kW}/\text{cm}^2$. The 2×2 VCSEL array ($d=200\mu\text{m}$) exhibit the maximum PCE was 47.2% at -30°C and decreased to 40.06% at 40°C ; the maximum power was 48.72mW at -30°C and decreased to 32.93% at 40°C . Full width half maximum (FWHM) was 1.05nm at -30°C and increased to 1.42nm at 40°C , respectively. The spectral broadening rate is only $0.0053\text{nm}/^\circ\text{C}$. The 2×4 VCSEL array ($d=200\mu\text{m}$) exhibit the maximum power was 90.8 mW at -30°C . We find an increase in output power and PCE of 2×2 VCSEL array as we increase the array spacing which we attribute primarily to increased heat dissipation and reduced thermal crosstalk between the emitters. Thermal properties in oxide-confined 2×2 VCSEL arrays were analyzed numerically and experimentally. The simulated results agree well with the measurement. It is proved that theoretical simulation is very useful for the future device optimization.

Declarations

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Figures

Figure 1

Sectional diagram of the VCSEL array

Figure 2

Schematic of experiment setup for (a) P-I-V and (b) far-field spot and spectrum

Figure 3

VCSEL: (a) Temperature-dependent threshold currents and slope efficiency. (b) Mode wavelength (MW) and gain peak wavelength (GPW).

Figure 4

VCSEL: (a) Temperature-dependent power and current (P-I-V) characteristics. (b) Power conversion efficiency (PCE) characteristics.

Figure 5

2x2 VCSEL arrays (array spacing $d=160\text{ }\mu\text{m}$, $180\text{ }\mu\text{m}$, $200\text{ }\mu\text{m}$): (a) Temperature-dependent power and current (P-I) characteristics. (b) Power conversion efficiency (PCE) characteristics.

Figure 6

2×2 VCSEL array ($d=200\ \mu\text{m}$) (a) Measured temperature-dependent emission wavelength ($I=40\text{mA}$). (b) Peak wavelength versus dissipated power at 20°C

Figure 7

2×2 VCSEL arrays: Simulated temperature distribution and temperature curve along A-A' cut-line in active region: (a) $d = 160 \mu\text{m}$. (b) $d = 180 \mu\text{m}$. (c) $d = 200 \mu\text{m}$