Effects of Fitting Parameter on Device Performance and Reliability of Double-Gate n-FinFET by Using Bohm Quantum Potential (BQP) Model

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Research Article

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Posted Date: February 23rd, 2022

DOI: https://doi.org/10.21203/rs.3.rs-1301648/v1

Effects of Fitting Parameter on Device Performance and Reliability of Double-Gate n-FinFET by using Bohm Quantum Potential (BQP) Model

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Abstract:

Scaling of devices has been reached a brick wall due to short channel effects (SCEs) and quantum behavior of carriers. At this level, the quantum mechanics became more powerful than classical mechanics. In this paper,3-D Bohm Quantum Potential (BQP) model has been used to evaluate the electrical characteristic of n-FinFET at 300Kfor different high-k materials as gate dielectric. In this work, the numerical tool Silvaco's Devedit has been used to simulate the device in 3-D.The sub-threshold swing (SS) is evaluated utilizing physics based modeling and numerical simulation, indicating strong dependency of SSon the fitting parameter (α), gate dielectric materials, and physical gate length of n-FinFET. The SS value down to 46.46 mV/decade is achieved using high gate dielectric constant (TiO2, k= 80). Here, drain induced barrier lowering (DIBL), transconductance, unity gain cut-off frequency (f_T), intrinsic gate delay, and off-state power dissipation etc. electrical parameters have been investigated.

Index Terms: Bohm Quantum Potential method, Devedit Silvaco simulator, fitting parameter, SCEs

1. Introduction

- **Need of FinFET over MOSFET :**

Aggressive gate pitch scaling forced designs for 22nm Intel technology to use self-aligned contacts [1]. At the side of the contact, the width and length of the spacers of the gate fill up leftover gate pitch distance (Fig. 1). If decreasing the width among two gate spacers, then contact resistance increases exponentially. Therefore gate length required scaling down. Due to this region, the planar devices limit gate length scalability. So we need an alternative device structure with enhanced channel controllability.

Multigate FETs (like FinFET) provide better short channel control operation and very low doping requirements in the channel; that's why the transverse field is more down in the channel, improving the sub-threshold swing (SS) and lowering the threshold voltage thus, device performances improve. Another importance of a low doping channel is lowered dopant ion scattering. It provides better driving current and lower fluctuations for random dopants [2].

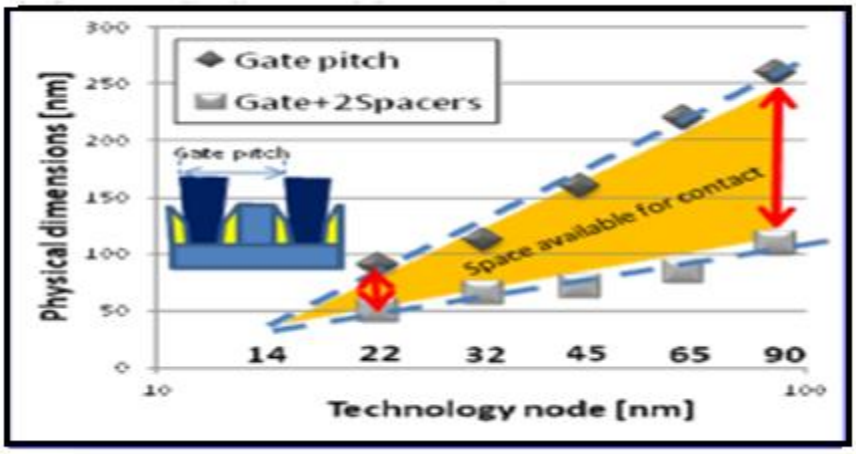

Fig.1 Gate pitch scalability challenge: Disappearing space for source/drain contact leads to increasing demand on gate length scaling [1].

In a FinFET, the gate wraps around a thin slice of (preferably undoped) silicon, also known as a "fin", and the drain currents flow with the side and top surfaces of the fin [3]-[5]. The wrapped gate around the channel increases the electrostatic control on the channel. Thus SCEs and leakage currents are reducing.A general structure of FinFET is shown in Fig.2.It offers structure parameters like fin width, fin height, and gate length. Today scaling is required for improving the digital performance of devices following Moore's law, but due to scaling, analog and RF performances are also affected in many ways [6],[7].

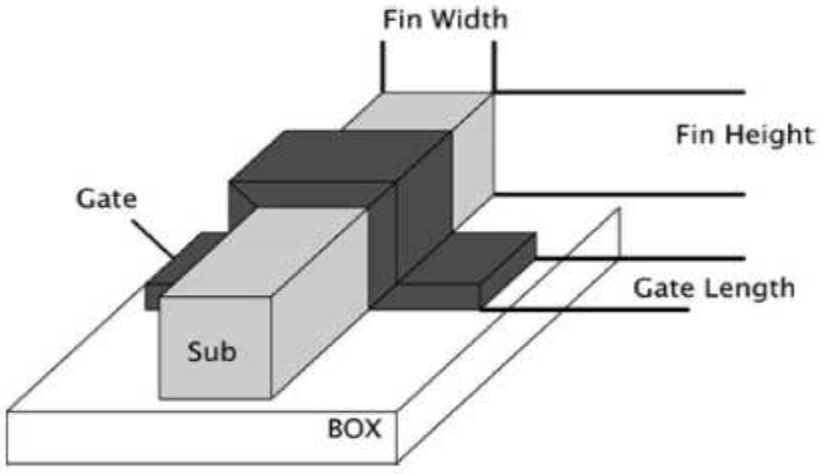

Fig.2 Standard Tri-gate FinFET device indicating the main geometrical parameters, namely, gate length, fin width, and fin height.

The effects of the BQP model on device performance at the various value of a fitting parameter (α) have been studied. A 3D devedit Silvaco simulator is used for result simulation. The main

goal of our paper is to investigate and compare thesub-threshold swing (SS)value for different high-k gate dielectric material as function of fitting parameter (α) and also, the performance of the proposed device is analyzed as function of the physical gate length of TiO2 based DG n-FinFET.

2. Physics of Proposed Device

- **Requirement of quantum mechanism :**

Today's semiconductor technology has gate lengths scaled down below 20 nm. Therefore, quantum effects become important. Due to scaling, tunneling occurs through the gate insulator, so alteration is required for gate controlling that is a function of V_{gs}. Here quantum confinements lead to a shift in the V_{th} and hence a clear increase of t_{ox} of devices.

For these quantum effects, we can use various models like drift-diffusion, density gradient, or BQP [8]. In this paper, the alternative method of the Density Gradient method called Bohm Quantum Potential (BQP) method has been used.The BQP method has two advantages over Density Gradient method.

1) Better convergence properties in many situations.
2) Better calibration to the Schrodinger-Poisson model.

2.1 Bohm Quantum Potential Model :

The University of Pisa has developed the BQP model for the silvaco simulator. Thismodel is an alternative method of the Density Gradient method, and it can be applied to asimilar range of problems. Behalf of Bohm's interpretation, the wave function (ψ) equation can be written as

$$\psi = R \exp\left(i\frac{S}{\hbar}\right) \quad \ldots\ldots (1) \text{ (in polar form)}$$

Where R, a probability density per unit volume, is the modulus of ψ and S has the dimension of an "action" (energy × time) and represents the phase of ψ multiplied by ħ.In these models, the wave function of particle is written in terms of its amplitude and phase. These are then substituted into the Schrodinger's equation to derive the following coupled equations of motion for density (2) and phase (3).

$$\frac{\partial \rho(r,t)}{\partial t} + \nabla.\left(\rho(r,t)\frac{1}{m}\nabla S(r,t)\right) = 0 \ldots\ldots\ldots (2)$$

$$-\frac{\partial S(r,t)}{\partial t} = \frac{1}{m}[\nabla S(r,t)]^2 + V(r,t) + Q(\rho,r,t) \ldots\ldots (3)$$

Where$\rho(r,t) = R^2(r,t)$ is the probability density, Q is the Bohm Quantum Potential, V is potential term from Schrodinger equation [9]. Equation 2 has the form of continuity equation. With the help of Madelung's transformation of the Schrodinger equation, the equations 2 and 3 have been derived. These two equations have the form of classical hydrodynamic equations with additional potential. This potential is derived from Bohm's interpretation of Quantum mechanics;

therefore, this potential is called Bohm Quantum Potential (BQP).The BQP equation is written by [10],

$$Q = -\frac{\hbar^2}{2}\gamma\frac{\tilde{\nabla}[M^{-1}\tilde{\nabla}(n^{\alpha})]}{n^{\alpha}} \quad \ldots\ldots\ldots (4)$$

From equation 4, it is observed that Q is the function of position, carriers density and fitting parameters. Where $\gamma$and α are two fitting parameters, $M^{-1}$is the inverse effective mass tensor and *n* is the electron (or hole) density for a quantum system of electrons, the electron density can be written as

$$n = \sum_i (f_i\ R^2{}_i) \quad \ldots\ldots\ldots\ldots (5)$$

The fitting parameter (α) is defined by, $\alpha = 1 - \frac{\eta}{2}$ ……...(6)

$$\eta \equiv \frac{\sum_i (f_i R^2{}_i)}{\sum_i f_i \nabla R^2{}_i . \sum_i (f_i \nabla [M^{-1}(R^2{}_i)]} \sum_i \frac{f_i \nabla (R^2{}_i) M^{-1} \nabla (R_i^2)}{R_i^2} \quad \ldots\ldots\ldots (7)$$

now,putting the value ofη in equation 6 then we get

$$\alpha \equiv 1 - \frac{1}{2}\frac{\sum_i (f_i R^2{}_i)}{\sum_i f_i \nabla R^2{}_i . \sum_i (f_i \nabla [M^{-1}(R^2{}_i)]} \sum_i \frac{f_i \nabla (R^2{}_i) M^{-1} \nabla (R_i^2)}{R_i^2} \quad \ldots\ldots\ldots (8)$$

α depends on the device structure and on the applied bias. Here, the effects of fitting parameter (α) on the device performance has been studied where α vary from 0.2 to 0.3.

- **Current equations for BQP model :**

For the Silvaco' ATLAS TCAD tool, the current equations in drift-diffusion model are given as

$$\overrightarrow{J_n} = qD_n \nabla n - qn\mu_n \nabla \psi - \mu_n n(kT_L \nabla(\ln n_{ie})) \quad \text{(for electrons)} \ldots\ldots (9)$$

$$\overrightarrow{J_p} = -qD_p \nabla p - qp\mu_p \nabla \psi + \mu_p p(kT_L \nabla(\ln n_{ie})) \quad \text{(for holes)} \ldots\ldots\ldots (10)$$

Where ψ is wave function, k is the Boltzmann's constant, T_L is lattice temperature and n_{ie} is effective intrinsic carrier concentration. The quantum effects are included in Silvaco's ATLAS TCAD tool by changing the transport model equations with the position dependent Bohm quantum potential (BQP). In Bohm quantum potential model, the current equations (9) and (10) take the form as given [11]

$$\overrightarrow{J_n} = qD_n \nabla n - qn\mu_n \nabla(\psi - Q) - \mu_n n(kT_L \nabla(\ln n_{ie})) \quad \text{(for electrons)} \ldots\ldots (11)$$

$$\overrightarrow{J_p} = -qD_p \nabla p - qp\mu_p \nabla(\psi - Q) + \mu_p p(kT_L \nabla(\ln n_{ie})) \quad \text{(for holes)} \ldots\ldots\ldots (12)$$

3. Device Structure And Simulation Framework

The 3D structures of proposed device are presented in Fig. 3(a) and (b), respectively. The value of device dimensions (i.e. L_g,H_{fin}, W_{fin} and t_{ox}) are listed in table.1. The high-k dielectric material (TiO2, k = 80) layer has been proposed to replace the conventional SiO2 gate dielectric material for good gate control of SCEs. In this paper we used titanium nitride (TiN) as gate material to avoid polysilicon depletion effect. The work-function of titanium nitride (TiN) is 4.65 eV. For drain and source contacts, here we used aluminum electrodes.The drain and source regions have the same n-type of doping concentration (10^{19} cm^{-3}) while the channel has a p-type lightly doped concentration (10^{16} cm^{-3}).

In 3D devedit silvaco simulator for device simulation have two main parts: (1) Structure formation and (2) Numerical resolution. Under Structure formation, it includes the mesh definition, deferent regions of the device, doping of devices, and electrodes. Under Numerical resolution, all gate-work functions, the physics of the models, and methods used by the simulator are defined[12]. The choice of physical models is important to improve the accuracy of the numerical simulation results. Here, the proposed device structure is based on the BQP model. The BQP model correctly predicts the quantum confinement.

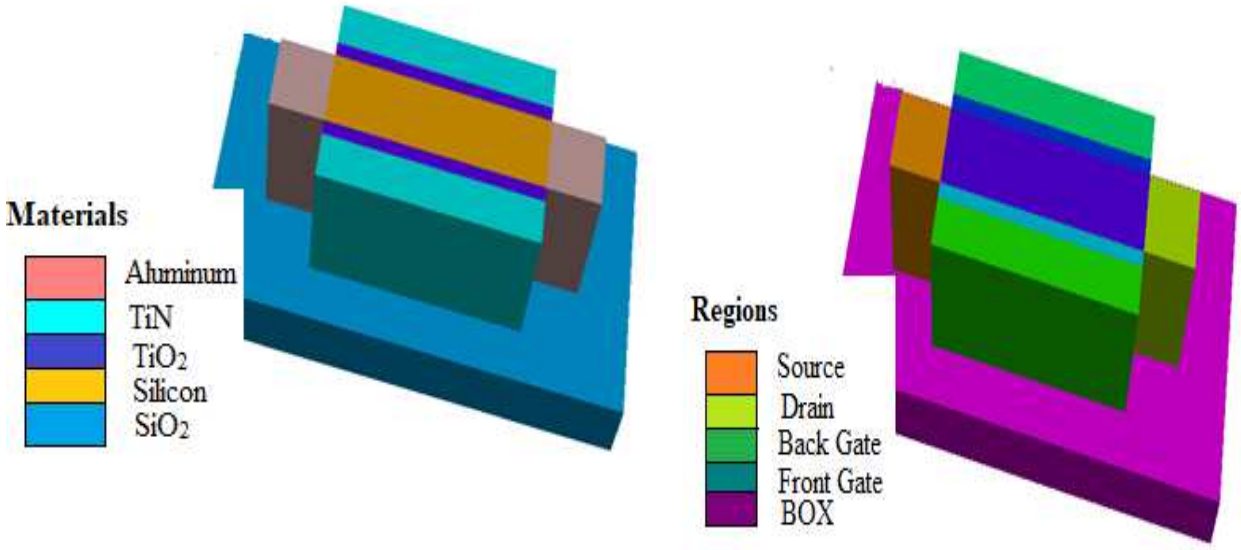

Fig.3 3D schematic view of TiO2 DG n-FinFET (a) on behalf of materials and (b) on behalf of regions.

Table 1 Parametersof TiO2 DG n-FinFET

Parameters	Values
Gate Length (L_g)	20 nm
BOX thickness (t_{box})	5 nm
Height of Fin (H_{fin})	10 nm
Width of Fin (W_{fin})	5 nm
Device Layer Doping (N_d)	10^{19} cm^{-3}
Gate work function	4.65 ev
Gate Oxide Thickness (t_{ox})	1 nm

4. Results and Discussion

BQP model is derived from pure physics and allows the model to approximate the quantum behavior of different classes of devices as well as a range of materials. The effects of quantum confinement on the device performance, including I-V characteristics, will then be calculated to a good approximation.

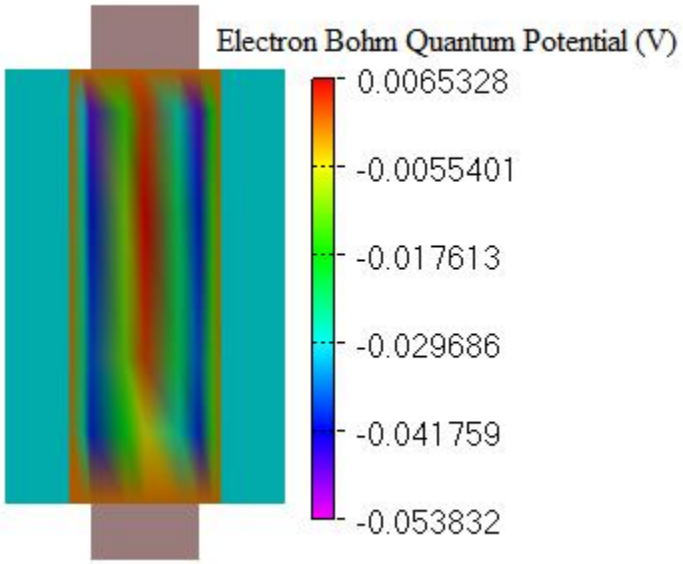

Fig.4 Top Cut plane view of proposed n-FinFET.the channel showing the electron BQP variation.

Fig.4 shows the electron Bohm Quantum Potential (BQP) variation. Here positive values of EBQP indicate the higher electron density at mid of channel and negative value of EBQP showing lower electron density around the edge of the channel. The electron and hole concentration for the BQP model is given by the equation [13]

$$n = N_c \exp\left(-\frac{E_c + qQ}{kT}\right) \quad \text{and} \quad p = N_v \exp\left(-\frac{qQ - E_v}{kT}\right) \quad \ldots\ldots\ldots\ldots \quad (13)$$

where Q is Bohm quantum potential,n and p are electron and hole concentration respectively.

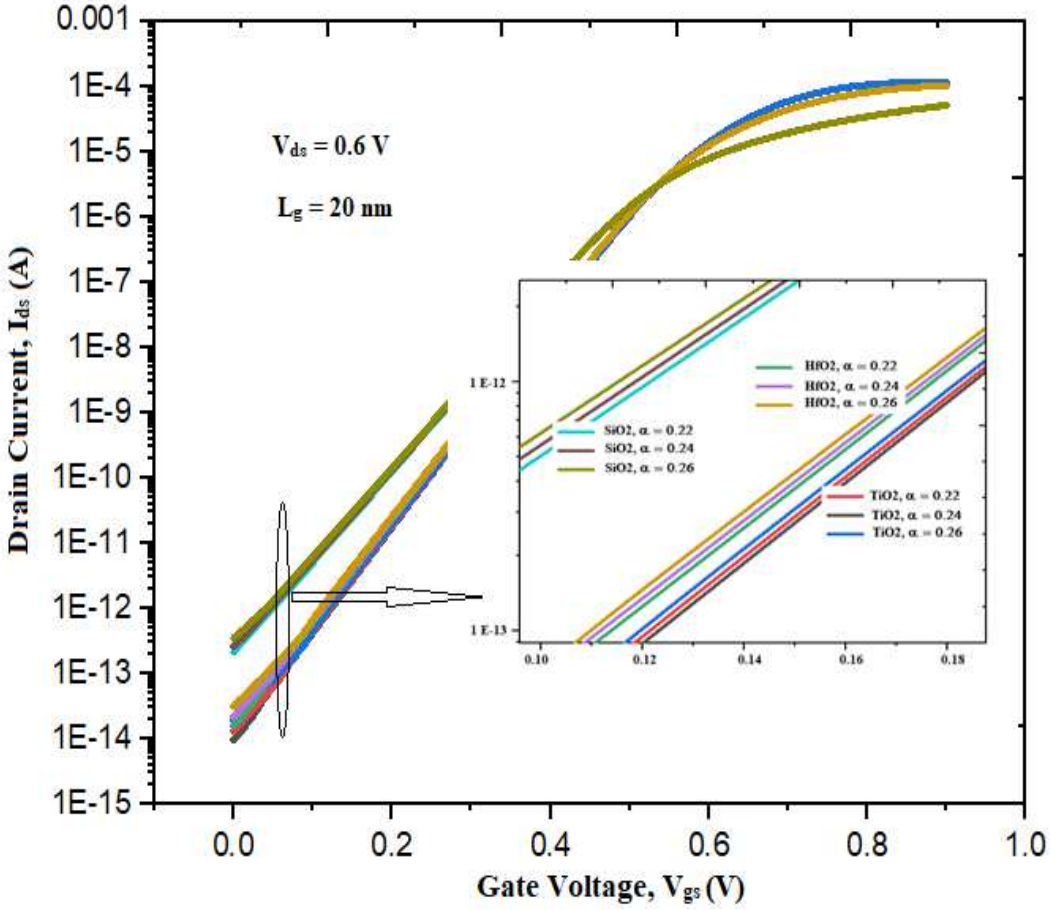

Fig.5 Transfer characteristics curve of DG n-FinFET with α= 0.22, α= 0.24 and α = 0.26 for high-k gate dielectric materials (i.e., SiO2, HfO2, TiO2) at V_{ds} = 600mV.

Fig.5 shows the I-V characteristics of DG n-FinFET for different high-k materials under α = 0.22, 0.24 and α = 0.26 on the logarithmic scale.The high-k gate dielectric materials having good controllability over the channel that's why drain current increases upto overdrive voltage (V_{gs}-V_{th}) then after the drain current gets saturate.Drain voltage was kept at 600 mV for measurement of I_{ON}/I_{OFF} current ratio. $I_{ON}$was studied at gate voltage (V_{gs}) = 0.9 V and I_{OFF} was measured at V_{gs} = 0 V. The device driving capability is approximately 0.2 mA at a gate overdrive voltage (V_{OV} =V_{gs}−V_{th}) of 0.53 V for TiO2 DG n-FinFET at α = 0.24. The device TiO2 DG n-FinFET has better SS, DIBL and higher I_{ON}/I_{OFF} ratio as compared to SiO2 DG n-FinFET and HfO2 DG n-FinFET. The all comparison parameters shown in table 2 at the different values of α.

4.1 Effect of gate dielectric materials on SS, DIBL and V_{th} :

The sub-threshold swing for various gate dielectric materials with the gate oxide thickness as a fixed parameter. As the dielectric constant increases, the sub-threshold swing decreases as shown

in Fig. 5. The changing rate of the sub-threshold swing decreases with the changing rate of the gate oxide film thickness as the dielectric constant increases. The reason for this is that the off current decreases as the dielectric constant increases. Therefore, the on-off current ratio will increase with the increase of the dielectric constant and the transistor performance will be improved [14]. Fig.5.shows the sub-threshold swing variation for different gate dielectric materials which are silicon oxide (SiO2, k = 3.9), hafnium oxide (HfO2, k=21) and titanium dioxide (TiO2, k = 80).In this model, the SS and DIBL decreases when gate dielectric material value increases. The SS and DIBL value shown in comparison table 2.

Table 2. Comparison of SS, DIBL and I_{ON}/I_{OFF} current ratio for DG n-FinFET at different gate dielectric materials.

Gate Dielectric Materials	Fitting Parameter (α)	Sub-Threshold Swing (mV/decade)	DIBL (mV/V)	Threshold Voltage (V_{th}) in volt	I_{ON}/I_{OFF} ratio
SiO2 (k=3.9)	α = 0.22	70.48	32	0.334	2.4×10^{8}
	α = 0.24	70.97	32	0.333	1.92×10^{8}
	α = 0.26	71.46	30.4	0.332	1.45×10^{8}
HfO2 (k=21)	α = 0.22	58.04	12	0.365	0.64×10^{10}
	α = 0.24	55.03	11.2	0.363	0.45×10^{10}
	α = 0.26	51.84	10.8	0.364	0.32×10^{10}
TiO2 (k=80)	α = 0.22	51.49	10	0.370	0.11×10^{11}
	α = 0.24	46.46	10	0.369	0.85×10^{10}
	α = 0.26	46.5	8	0.369	0.32×10^{10}

4.2 Effect of physical gate lengths and fitting parameter on Sub-threshold Swing of DG n-FinFET :

The change of the sub-threshold swing along with the physical gate length is shown in Fig.5. As seen in Fig.6, in the case of HfO2 with a dielectric constant of 21, it can be seen that the sub-threshold swing greatly changes along with the channel length. That is, the short channel effect becomes large and the sub-threshold swing increases greatly as the channel length decreases. However, the short channel effect decreases as the dielectric constant increases. In particular, it is observed that the TiO2 with a dielectric constant of 80 does show the small short channel effect even if the channel length decreases.

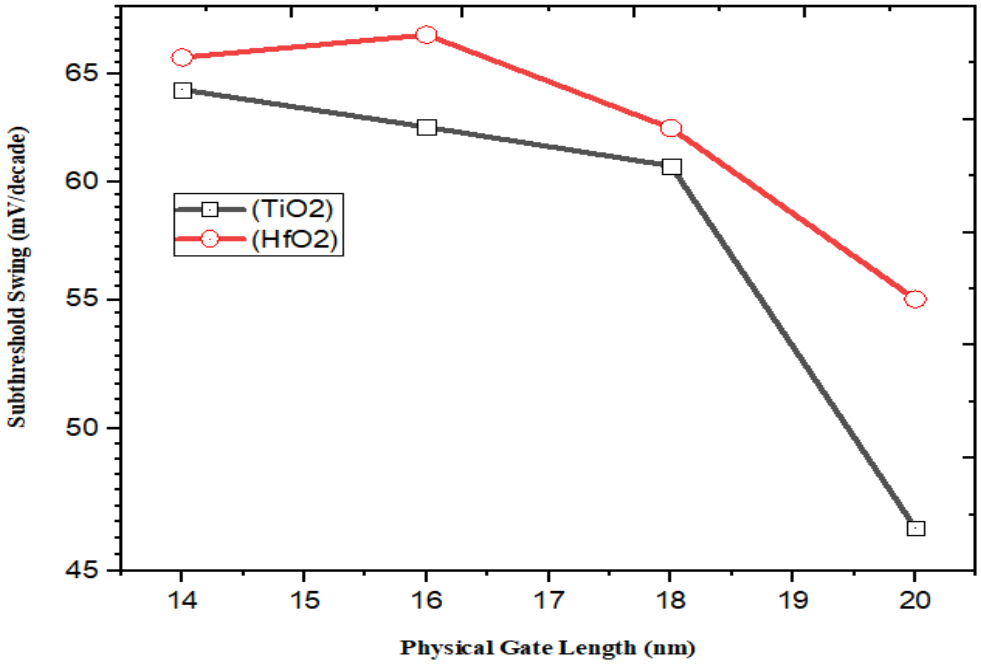

Fig.6 Sub-threshold Swing curve of DG n-FinFET as function of gate length at V_{ds} = 0.6 V

Fig.7 shows the change of the sub-threshold swing with respect to fitting parameter vary from α = 0.2 to 0.3.In BQP model equation, the fitting parameter (α) basically depends on dimension of device as well as supply voltage and SS is also dependent on Vgs. From the Fig.7, it has been observed that the sub-threshold swing decreases from 58.36 mV/dec to 33.6 mV/dec when α vary from 0.2 to 0.3 for TiO2 gate dielectric material. But the best value of α is 0.24 for sub-threshold current. At α equal to 0.24, the SS is 46.46 mV/decade for TiO2 gate dielectric materials better as compared to SS value 55.03 mV/decade for HfO2 gate dielectric material.

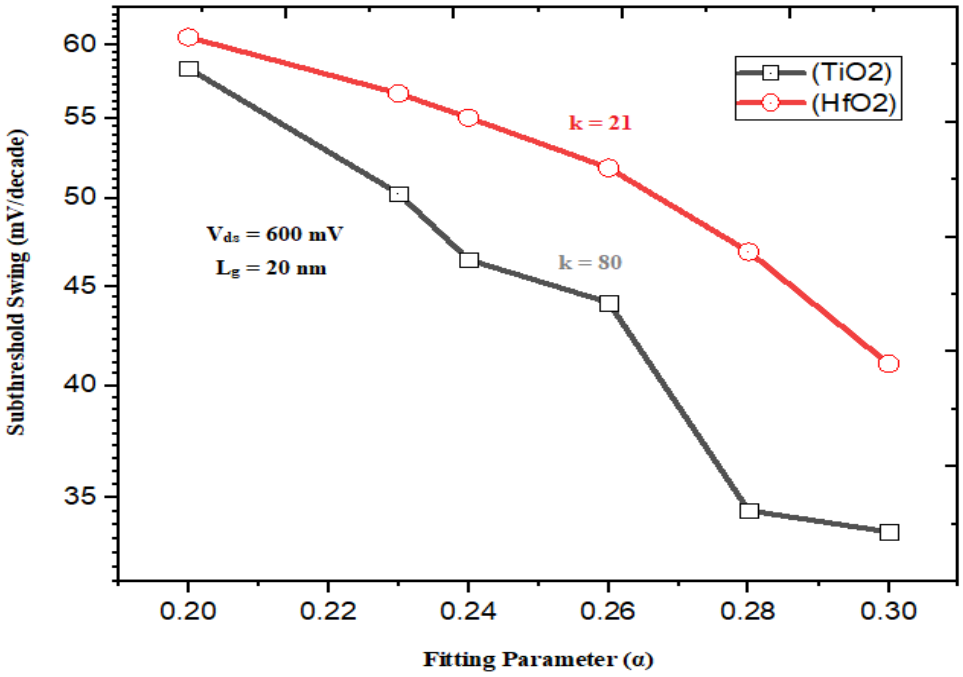

Fig.7 Sub-threshold Swing versus fitting parameter curve.TiO2 n-FinFET have lower (i.e., better) ss values than HfO2 n-FinFET

4.3 DC and Analog/RF performance of TiO2 DG n-FinFET (proposed n-FinFET) :

Fig.8.presentsthe I-V characteristics of a proposed FinFET with different gate lengths at α = 0.2. The curves present the relationship between the drain current and gate voltage for different values of physical gate length. First, it can be easily observed from Fig.8, that the current flattens with increasing the gate length. The current level depends on the gate length as well as gate voltage, The smaller gate length has low channel resistance, and lower transit times means the carriers move very faster from source to drain end; therefore, transistor operation will increase.Table.4 shows the comparison of device characteristics between the proposed FinFET in our work and other FinFETs reported in the previous works [15], [16]. The proposed FinFET shows higher I_{ON}/I_{OFF} ratio, reduced DIBL value, and lower sub-threshold swing (SS = 46.46 mV/dec) as compared to reported FinFETs.

Table 3 Comparison of device characteristics betweenTiO2DG n-FinFET (proposed) in this work and other reported FinFETs

	Proposed work	**Ref.[13]**	**Ref.[14]**
Wafer type	SOI	SOI	Bulk
Gate electrode	TiN	N^+-poly-si	Poly-si
Dielectric	TiO_2	SiON	SiO_2
Gate Length, L_g (nm)	20	40	100
Oxide Thickness, t_{ox} (nm)	1	1.4	5
Drain Voltage, V_{dd} (V)	0.6	1.2	1.5
ON-Current, I_{ON} (mA)	0.12	0.54	0.26
SS (mV/dec)	46.46	79	80
DIBL (mV/V)	10	155	7
I_{ON}/I_{OFF} ratio	> 10^9	> 10^6	> 10^7

The DC-performance of proposed n-FinFET shown in table.4 at different physical gate length. From the comparison table.4, we can say that the 20 nm gate length provides better sub-threshold swing (46.46 mV/decade at α = 0.24) and higher I_{ON}/I_{OFF} current ratio as compared to other reported FinFETs gate lengths (i.e., L_g = 40 nm and 100 nm)

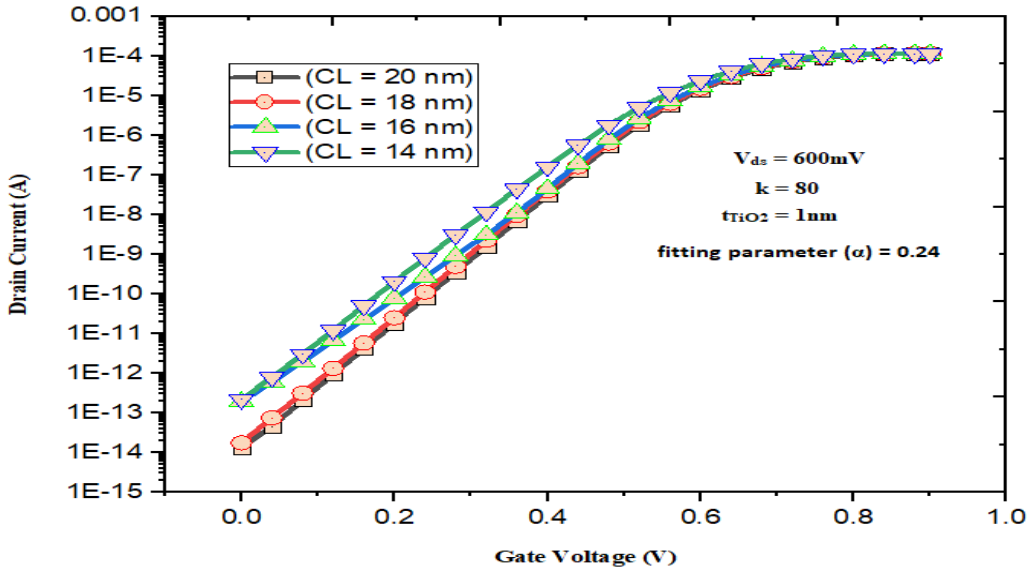

Fig.8 Transfer characteristics of proposed n-FinFET for different gate length at V_{ds} = 600mV

Table 4 Comparison of DC parameters of proposed FinFET at different gate lengths

Physical Gate Lengths (nm)	Sub-threshold Swing (mV/decade)	Threshold Voltage (V_{th}) in volt	I_{ON}/I_{OFF} ratio
CL = 14	64.25	0.315	0.5×10^9
CL = 16	62.50	0.356	0.6×10^9
CL = 18	60.73	0.360	0.65×10^{10}
CL = 20	46.46	0.369	0.85×10^{10}

The transconductance (g_m) behavior of the DG n-FinFET is simulated by the silvaco tools using the BQP model atVds = 0.6 V, as shown in Fig. 9. Initially, the g_m is increasing up to V_{gs} = 0.66 volts. Because of the inversion current (I_{inv}) starts contributing to I_{ds}. After V_{gs} = 0.66 volts, it decreases because overdrive (V_{gs} - V_{th}) voltage increases at constant I_{ds}, which means gm is inversely proportional to overdrive (V_{gs} – V_{th}) voltage. The transconductance of TiO2 is higher than the transconductance of HfO2 and SiO2 based DG n-FinFET shown in Fig.9.

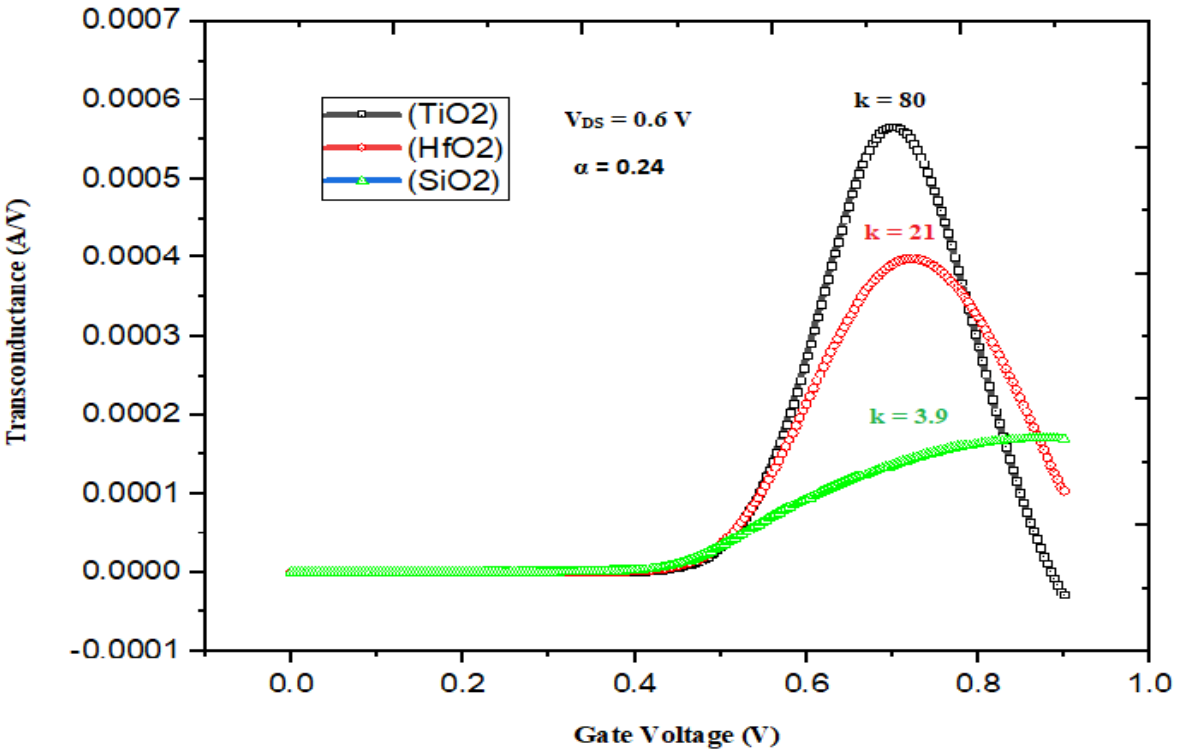

Fig.9 Transconductance curve of DG n-FinFET with different high-k at V_{ds} = 0.6 V

Fig. 10 shows the high frequency capacitances likes gate-to-source capacitance (C_{gs})and gate-to-drain capacitance (C_{gd})for n-FinFETas a function of the gate-to-source voltage for drain voltage

of V_{ds}= 600mV. The simulated results of gate-to-source capacitance (C_{gs}) and gate-to-drain (C_{gd}) are 78.5 aF and 83.4 aF, respectively, for the proposed device. For the analog/RF performance (likes, f_T, and intrinsic delay) of devices, the capacitance (C_{gg}) value should be lower. From equation (14), we can say smaller capacitance (C_{gg}) provides a better intrinsic cutoff frequency (f_T).

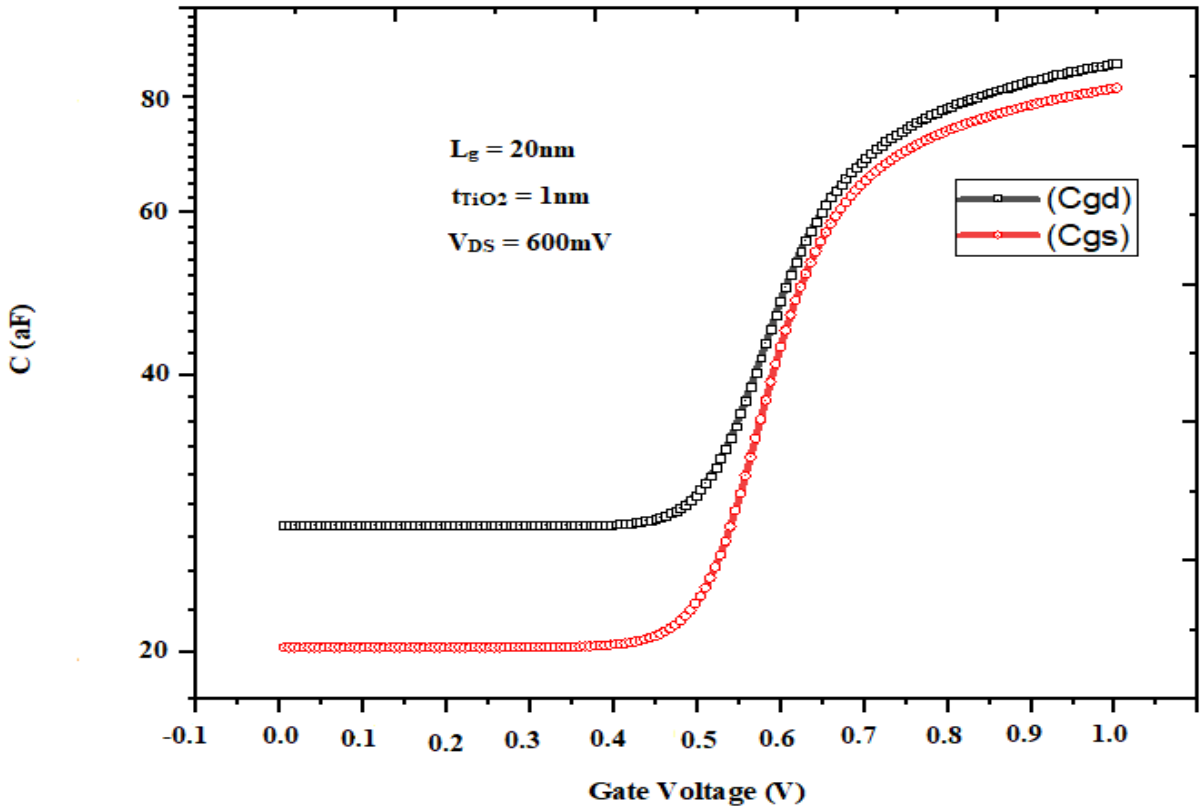

Fig.10 Cgs and Cgd versus Vgs plot for TiO2 DG n-FinFET

For RF application, the unity gain cut-off frequency (f_T) is very important parameter to study. The f_T equation is given

$$f_T = \frac{g_m}{2\pi c_{gg}} \quad \text{..... (14)}$$

- **Relation between cutoff frequency and transit time of device :**

We know that, $g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_n C_{ox} \frac{W_{eff}}{L}(V_{gs} - V_{th})$, put the value of g_m in equation (14) then we get

$$f_T = \frac{\mu_n Cox \frac{W_{eff}}{L}(Vgs - Vth)}{2\pi c_{gg}} \quad \text{..... (15)}$$

$$f_T = \frac{\mu_n(Vgs - Vth)}{2\pi L^2}, \text{ (where } C_{gg} = C_{ox}WL) \quad \ldots\ldots\ldots\ldots (16)$$

$$f_T = \frac{\mu_n E_{ch}}{2\pi L} = \frac{v_d}{2\pi L} = \frac{1}{2\pi\tau_t} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (17)$$

Where g_m is transconductance and c_{gg} is gate to gate capacitance. The value of c_{gg} is sum of the c_{gs} and c_{ds}, W_{eff} is effective fin width ($W_{eff} = 2H_{fin}$) and τ_t is transit time. Fig.11 represents f_T for TiO2 DG n-FinFET as a function of the V_{gs} with different value of α. f_T of proposed n-FinFET is 1392 GHz at $\alpha = 0.24$.It is higher than the other value of α. The higher f_T makes it suitable for the device's high speed because a small gate length provides a low transit time. From equation (17), we can say shorter transit time provides a higher intrinsic cutoff frequency [17].

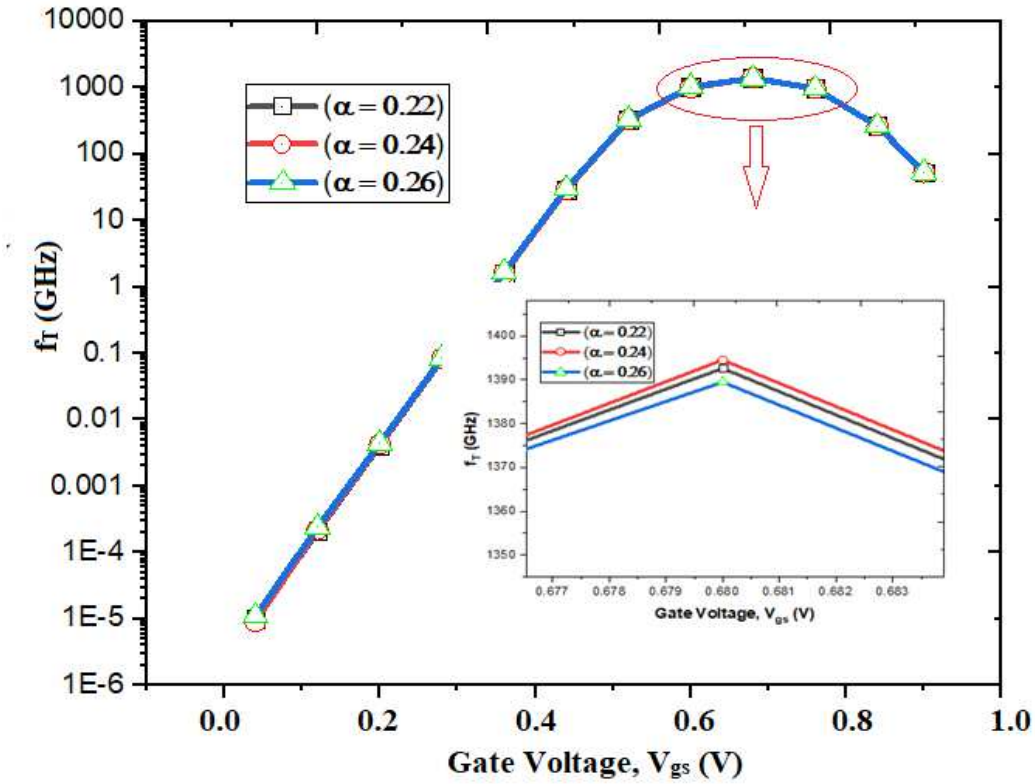

Fig.11 Cut-off frequency versus gate voltage graph for TiO2 DG n-FinFET at different values of α

Another important parameter is intrinsic gate delay (τ_{int}). It represents the frequency limit of the transistor operation. The equation of τ_{int} is written as for the n-FinFET in terms of parasitic gate capacitance (C_{gg}) [18]

$$\tau_{int} = \frac{C_{gg} \times V_{dd}}{I_{ds}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (18)$$

Where τ_{int} represents the intrinsic gate delay, Fig. 12 shows the τ_{int} versus drain-to-source voltage (V_{ds}) curve for the proposed n-FinFET at different values of α. it shows that delay for high-k (k= 80) n-FinFET at α = 0.24 is lower than α = 0.22 and 0.26 at low V_{ds} values. At this V_{ds} value, I_{ON} becomes higher. After this V_{ds} value, if V_{ds} again increasing the drain current becomes constant, and C_{gg} also acquires its maximum value of accumulation mode at flat band voltage (V_{FB}). Hence the intrinsic delay increases a bit. Hence, for low power applications, this model is good at α = 0.24 because it has a lower intrinsic gate delay than other values of α.

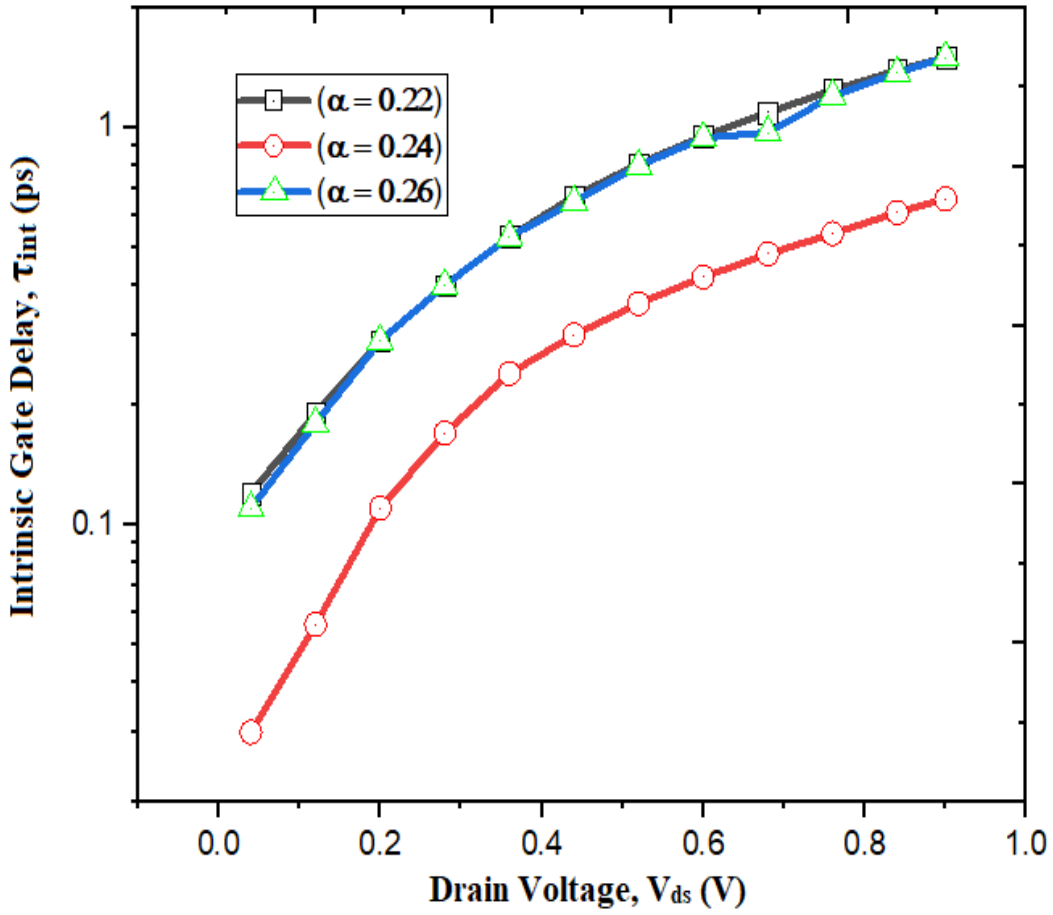

Fig.12 Intrinsic gate delay curve as function of drain voltage for TiO2 DG n-FinFET at different values of α

Another important parameter is off-state power dissipation shown in Fig.13.it has been plotted as a function of drain-to-source voltage. The off-state power dissipation is calculated by PD = I_{OFF}× V_{dd}. This parameter indicate the high V_{dd} based device have higher off-state power dissipation.Table.4 show the comparisons of analog/RF parameters (i.e. f_T, τ_{int} and PD) with different values of α.

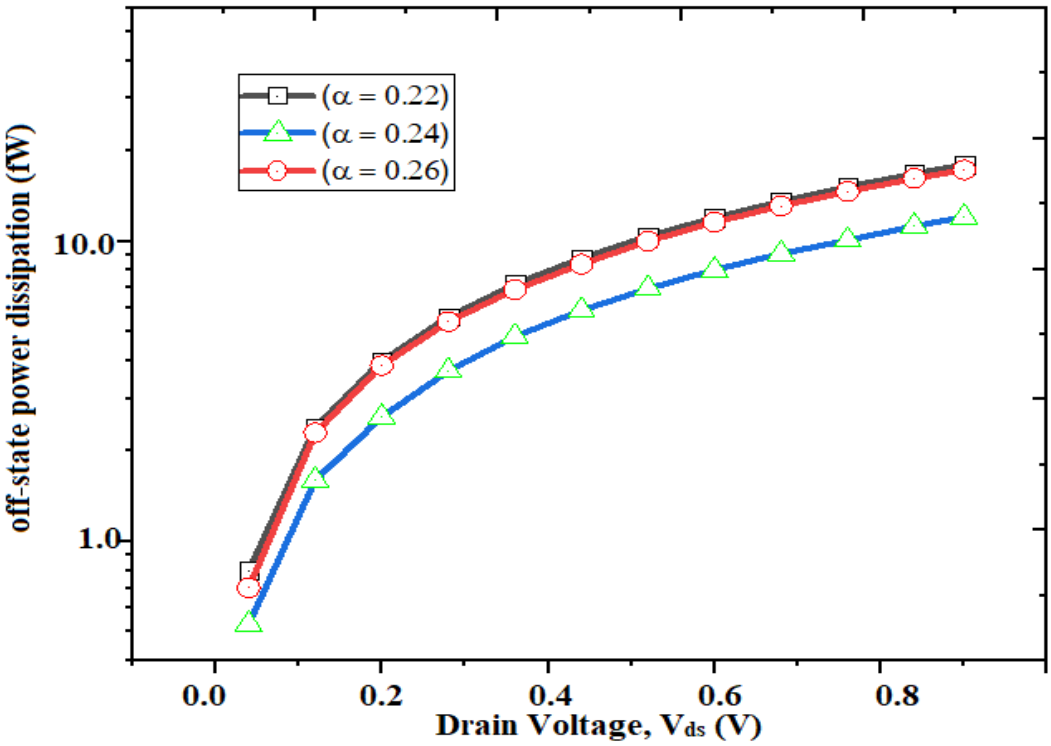

Fig.13 off-state power dissipation curve as function of drain voltage for TiO2 DG n-FinFET at different values of α

Table.5. Comparison of f_T, PD and τ_{int} for TiO2 n-FinFET at different values of α

Fitting Parameter (α)	Cut-off Frequency,f_T (GHz)	off-state power dissipation,PD (fW)	Intrinsic Gate Delay,τ_{int} (ps)
α = 0.22	1392.60	12	0.95
α = 0.24	1394.5	8.04	0.42
α = 0.26	1390	11	0.94

5. Conclusions

In this paper, the BQP model is used in the physics section of the 3D devedit Silvaco simulator to evaluate the I-V characteristics, Sub-threshold Swing, DIBL, gm, intrinsic gate delay, and off-state power dissipation at the different value of a fitting parameter (α = 0.22, 0.24 and 0.26).In the proposed device, the channel is lightly doped because the doped channel reduced the effect of impact ionization; therefore, sub-threshold swing decreases. At 1 nm gate-oxide thickness, a low DIBL value of 10 mV/V, sub-threshold swing is 46.46 mV/dec, driving current of 0.2 mA and leakage current of 13fA have been achieved for the TiO2 DG n-FinFET at α = 0.24.In comparison to density gradient methods the chief benefits of this method BQP model is that both Maxwell-Boltzmann and Fermi-Dirac statistics have been included, adopted independent transport model, and delivers better fit and calibration.

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Statements and Declarations

Funding statement: Young Faculty Research Fellowship scheme under Digital India Corporation.

Conflict of Interest: There is no conflict of interest.

Author contributions: The first author has written and documented the paper and the second author collected the research material, checked, and modified the technical content.

Availability of data and material: All sources of data are from reference cited in the paper.

Compliance with ethical standards: The work has maintained ethical standard.

Consent to participate: The authors agree to participate.

Consent for Publication: The authors agree with the copyright policy of the journal.