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Effect of Uniaxial Strain on Characteristic Frequency of Scaled SiGe HBT with Embedded Stress Raiser

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Abstract

In order to further improve the performance of scaled silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) and consider the compatibility with mature CMOS process, a novel SiGe HBT is designed by introducing the embedded Si_{1-y}Ge_y stress raiser into the collector. In the proposed HBT structure, the collector region is subjected to additional uniaxial stress, to enhance the characteristic frequency. The effect of embedded Si_{1-y}Ge_y stress raiser on the frequency performance with different Ge mole fractions is simulated and analyzed by employing SILVACO[®]TCAD tools. The simulation results show that the high frequency performance of the device can be significantly improved by applying additional uniaxial stress in the collector. At $y = 0.3$, the current gain of the device is increased by approximately 6% compared to the case where no stress is applied to the collector region ($y = 0$). Taking the uniform SiGe base case with the Ge fraction of 0.25 as an example, by adjusting the Ge fraction of the stress raiser, the peak values of f_T and f_{max} reach about 507.7 GHz and 730.7 GHz, respectively. Compared with the traditional SiGe HBT without any additional stress in the collector region, f_T and f_{max} are respectively increased by 29.1% and 71.5%. When $y = 0.1$, the proposed device has the best frequency characteristics due to the peak value of the $f_T \times f_{max}$ product.

Keywords: SiGe HBT, uniaxial stress, stress raiser, cut-off frequency

1 Introduction

As integrated circuits (ICs) continue to move towards smaller process nodes, the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of silicon-based devices gradually enter the terahertz (THz) band. Compared with traditional III-V semiconductor devices, silicon-based

high-frequency devices have the advantages of low cost, easy mass production, and compatibility with developed CMOS process, then gradually attract the attention of countries around the world [1]. As the core device in RF ICs, SiGe HBT takes advantage of energy band engineering and is fully compatible with mature silicon processes. The “DOTFIVE” and “DOTSEVEN” initiatives

were proposed by STMicroelectronics, Infineon, and other research institutes [2, 3]. Its goal is to develop SiGe HBT devices that can be used in communication and remote sensing with (f_T) up to $0.5 \sim 0.7$ THz, and give full play to the great potential and technical advantages of SiGe HBT in reference circuits and system applications. The International Semiconductor Technology Roadmap (ITRS) predicts that the f_T/f_{\max} of HBT will reach 570/610 GHz by 2020 [4]. Currently, the frequency performance of SiGe HBTs is mostly improved at the expense of high process costs, and the frequency performance of SiGe HBTs is improved by continuously optimizing the process flow and reducing the process node to reduce the lateral size of the device [5–7].

On the other hand, as the feature size of ICs becomes smaller and smaller, the isometric scaling technique faces more and more severe challenges. Silicon-based strain technology can effectively improve the mobility of carriers, thus improving the performance of devices, and has become an important mature technology and development direction of high-frequency/high-performance semiconductor devices and ICs [8]. Strain effect now has been introduced into SiGe HBT to improve device performance [9–12]. STMicroelectronics uses stacked metal interconnect wire structure near HBT based on BiCMOS-9W process [9]. The uniaxial stress is introduced into the device by the different thermal expansion coefficients of each metal layer. f_T and f_{\max} increased by 21% and 12%, respectively. Ref. [10] proposed a new strain Si HBT device structure that uses a relaxed SiGe virtual substrate as the collector region and grows biaxial strain Si (SSi) on it as the emitter region. Compared with the traditional SiGe HBT, the current gain is increased by 11%. It should be noticed that the self-heating effect of virtual SiGe substrate is very significant, which cannot meet the requirement of ultra-high frequency [11]. In Ref. [12], external SiGe stress film is used to apply uniaxial stress to the base region of conventional bulk Si BJT, and TCAD simulation is carried out based on the fluid dynamics (HD) model. The simulation results showed that the f_T and f_{\max} are only increased by about 5% and 3% respectively, and the improvement effect of a characteristic frequency is very limited. Ref. [13] investigated the effect of global stress on the

high-frequency characteristics by full-band Monte-Carlo simulation, but the way of applying the additional uniaxial stress is not discussed in detail.

In view of the above, the device structure proposed in this work employs the “Embedded SiGe source/drain Technology” which commonly used in the uniaxial strain Si PMOS transistors. In this work, the $\text{Si}_{1-y}\text{Ge}_y$ stress raiser is implanted in the collector region of the device, and the uniaxial stress is introduced into the collector region, which is convenient for BiCMOS integration with the strained-Si CMOS process. The influence of Ge mole fraction y in the embedded $\text{Si}_{1-y}\text{Ge}_y$ stress raiser on f_T and f_{\max} was further investigated and simulated analysis was conducted to reveal the physical causes for the influence of additional uniaxial stress in the collector region on characteristic frequency, to provide some potential possibilities for the design of silicon-based terahertz ICs in the future.

2 Device Structure

The structure of the NPN SiGe HBT device with additional uniaxial stress in the collector region designed in this work is shown in Fig. 1. In this structure, the base region and emitter region have the same width. The parasitic effect between Si cap layer and SiGe base layer can be reduced and the frequency characteristics of the device can be improved. The emitter region width is reduced to 100 nm to effectively reduce the intrinsic resistance of the base region. Embedded $\text{Si}_{1-y}\text{Ge}_y$ stress raiser at both sides of the collector region introduces uniaxial strain, which improves the mobility of carriers, effectively reduces the square resistance of the collector region and the transmission time of carriers in the collector region, reduces the effective collector region width and BC junction capacitance, and improves the frequency characteristics of the device. The Si cap layer is subjected to uniaxial tensile stress and the resulting interfacial barrier in the emitter region effectively reduces the reverse current injected into the emitter region from the base region, thus improving the current gain of the device. In addition, for SiGe HBT fabricated by traditional bipolar process, the BE junction area is usually smaller than the BC junction area, and the current gain is limited by the larger BC junction area.

For the structure proposed here, two P⁺ diffusion regions are implanted below the SiGe base region as the contact part of the external base region, therefore, the current gain can be further improved.

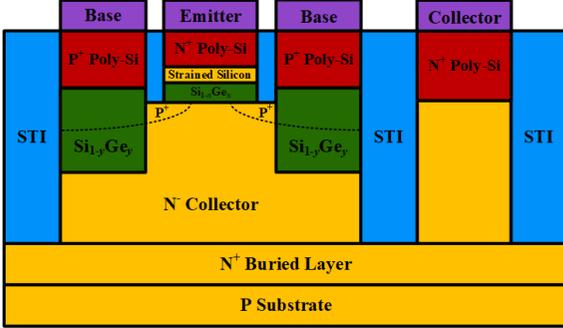


Fig. 1 Device structure with embedded Si_{1-y}Ge_y stress raiser

3 Estimation of Strain Mechanism

Since the lattice constant of SiGe is greater than that of Si, the embedded Si_{1-y}Ge_y stress raiser generates a longitudinal uniaxial compressive stress σ_{xx} in the collector region. The Si lattice in the collector region is further compressed and the lattice constant decreases. The Si_{1-x}Ge_x base region is superimposed with uniaxial compressive stress on top of the conventional biaxial compressive stress to form the composite strain base region. The Si cap in the emitter region is also affected by the uniaxial tensile stress σ_{xx} . Considering the requirement of integration with uniaxial strain Si PMOS transistors, uniaxial compressive stress is usually applied along the [110] direction of (001) substrate, and the Si cap and the substrate collector region should have the same strain tensor ε_{Si} [13].

$$\varepsilon_{\text{Si}} = \begin{bmatrix} s_{12}\sigma_{xx} & 0 & 0 \\ 0 & \frac{1}{2}(s_{11} + s_{12})\sigma_{xx} & \frac{1}{4}s_{44}\sigma_{xx} \\ 0 & \frac{1}{4}s_{44}\sigma_{xx} & \frac{1}{2}(s_{11} + s_{12})\sigma_{xx} \end{bmatrix}, \quad (1)$$

s_{11} , s_{12} and s_{44} are elastic compliance coefficients, the longitudinal strain tensor is:

$$\varepsilon_{\parallel, \text{Si}} = \frac{1}{2}(s_{11} + s_{12})\sigma_{xx}. \quad (2)$$

For the SiGe base layer with composite strain, the lattice constant of the collector region is further reduced by uniaxial stress compared with that of the conventional biaxial strain. To be consistent with the longitudinal strain tensor $\varepsilon_{\parallel, \text{Si}}$ in Eq. (2), the base region of the composite strain level and strain tensor $\varepsilon_{\parallel, \text{SiGe}}$ is equivalent to:

$$\varepsilon_{\parallel, \text{SiGe}} = (1 + \varepsilon_{\parallel, \text{Si}}) \frac{a_0}{a(x)} - 1, \quad (3)$$

Where a_0 and $a(x)$ are the lattice constants of relaxed Si and relaxed Si_{1-x}Ge_x, respectively. If the longitudinal strain tensor of the biaxial strain SiGe base region is consistent with that in Eq. (3), the equivalent lattice constant $a^*(x)$ of the composite strain base region can be expressed as:

$$a^*(x) = \frac{a(x)}{1 + \frac{1}{2}(s_{11} + s_{12})\sigma_{xx}}. \quad (4)$$

For uniaxial compressive stress, $\sigma_{xx} < 0$. For uniaxial tensile stress, $\sigma_{xx} > 0$. It can be seen that $a^*(x) > a(x)$ from the above, due to the uniaxial compressive stress introduced in the collector region. This corresponds to the fact that the additional uniaxial stress in the collector region has the effect of increasing the value of the Ge fraction x in the base region caused by the composite strain while maintaining the same level of strain as in the conventional biaxially strained Si_{1-x}Ge_x base region, the bandgap of the base region is spontaneously reduced and the intrinsic carrier concentration is increased, resulting the bandgap of the Si cap-layer is also reduced and its intrinsic carrier concentration is increased.

The characteristic frequency of SiGe HBT mainly refers to the cut-off frequency f_T . This work only considers the frequency characteristics under the condition of a small signal and ignores the large injection effect. According to the small-signal model, the expressions of f_T and f_{max} are [14]:

$$f_T = \frac{1}{2\pi[\tau_F + \frac{kT}{qI_C}(C_{\text{BE}} + C_{\text{BC}}) + (R_E + R_C)C_{\text{BC}}]}. \quad (5)$$

$$f_{\text{max}} = \sqrt{\frac{f_T}{8\pi R_B C_{\text{BC}}}}. \quad (6)$$

kT/qI_C is the BE junction dynamic resistance, I_C is the BC junction electron current, C_{BC} is the capacitance of the BC junction, C_{BE} the BE junction capacitance, R_E and R_C represent the emitter resistance and collector resistance, respectively. τ_{BC} is the forward transit time. Under the condition of small signal, the transit time can be approximately expressed as [15]:

$$\tau_F \approx \frac{1}{\beta} \left(\frac{W_E}{S_{pE}} + \frac{W_E^2}{2D_{pE}} \right) + \frac{W_B^2}{2D_{nB}}. \quad (7)$$

In order to reflect the effect of stress on the characteristic frequency, this work only considers the Ge fractions of the base layer as a constant, and uniform doping in the base region. In Eq. (7), W_E and W_B are the longitudinal width of the emitter region, and the longitudinal width of the base region, respectively. β the current gain, D_{pE} , and D_{nE} are minority carrier diffusion coefficients in the emitter region and the base region respectively, S_{pE} represents the holes recombination velocity at the contact interface of the emitter region.

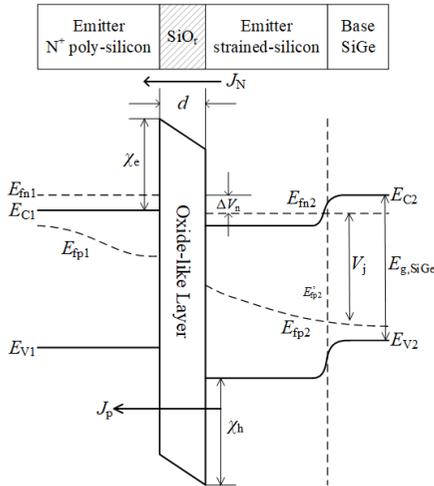


Fig. 2 Energy-band of poly-Si/oxide-like layer/strained Si system

As shown in Fig. 2, the thickness of the polysilicon emitter is W_1 , and an extremely thin “oxide-like” layer SiO_x is formed at the interface with the strained Si layer, the barrier heights of electrons and holes are χ_e , and χ_h . The barrier height of electron χ_e is generally very small. For

electrons injected from the emitter region to the base region, the transport process is not affected by the oxide-like layer, and it is “transparent” for electrons [16]. χ_h acts as a barrier to the holes injected from the base region, and the holes pass through the oxide-like layer in the form of quantum tunneling. V_j is the bias voltage falling on the Si/SiGe BE junction and meets $V_{BE} = V_j + \Delta V_n$. If the holes in the emitter region comply with the Boltzmann distribution, the holes tunneling current can be written as:

$$J_P = J_{PT} = \frac{4q\pi m_h^*(kT)^2 P_{T,Si}}{h^3} \exp\left(-\frac{q\Delta V_p - E_{fp1}}{kT}\right). \quad (8)$$

h is Planck constant, $P_{T,Si} \approx \exp(-d\sqrt{\chi_h})$ is the holes tunneling probability [17]. m_h^* is the effective mass of holes. The thickness of the silicon cap layer is very thin and is uniformly doped with the concentration is N_D . χ_h increases $\Delta E_{V,SSi}$ due to the upward shift of the valence band under the action of stress, and the tunneling probability becomes:

$$P_{T,SSi} \approx \exp(-d\sqrt{\chi_h + \Delta E_{V,SSi}}). \quad (9)$$

Neglecting the recombination in the strained Si cap layer, the hole tunneling current can be rewritten as:

$$J_P = \frac{qn_{i,SSi}^2 P_{T,SSi}}{N_D} \sqrt{\frac{kT}{2\pi m_h^*}} \exp\left(\frac{qV_j}{kT}\right) = \frac{qn_{i,Si}^2}{G_{E,SSi}} \exp\left(\frac{qV_{BE}}{kT}\right), \quad (10)$$

$n_{i,Si}$ and $n_{i,SSi}$ are the intrinsic carrier concentrations of relaxed and strain Si cap layers, respectively. Due to the uniaxial stress applied on the Si cap layer, the bottom of the conduction band E_C decreases. Under the same V_{BE} conditions, ΔV_n increases $\Delta E_{C,SSi}/q$, the actual BE junction voltage drop decreases accordingly $\Delta V_j = \Delta E_{C,SSi}/q$. For the base region of uniform doping and uniform Ge fraction, the Gummel Number of the emitter region, ie. $G_{E,SSi}$ and the collector current density J_C are as follows:

$$G_{E,SSi} = \frac{N_D}{S_{pE}} \frac{n_{i,Si}^2}{n_{i,SSi}^2} \exp\left(\frac{q\Delta V_n + \Delta E_{C,SSi}}{kT}\right), \quad (11)$$

$$J_C \approx \frac{q \exp\left(\frac{qV_{BE}}{kT}\right)}{\left[\int_0^{W_B} \frac{N_B}{D_B^*(n_{i,SiGe}^*)^2} dx\right]} \quad (12)$$

$$= \frac{q(n_{i,SiGe})^2}{G_{B,SSi}} \exp\left(\frac{qV_{BE}}{kT}\right),$$

$S_{pE} = P_{T,SSi} \sqrt{kT/2\pi m_h^*}$ is the recombination velocity at the interface of the emitter region. The additional uniaxial stress on the substrate leads to the increase of the intrinsic carrier concentration $n_{i,SiGe}^*$ in the base region, and the minority carrier diffusion coefficient $D_B^* \propto \mu_{nB} = (1 + 3x)\mu_{n0}$ [18] in the base layer also increases, μ_{n0} is electron mobility of relaxed Si. It can be seen that the uniaxial stress increases the base Ge fraction x equivalently, thus increases, but $\Delta E_{C,SSi}$ will also reduce J_C , so the value of J_C is mainly determined by Ge fraction y in $Si_{1-y}Ge_y$ stress raiser. The $G_{B,SSi}$ of the base region can be derived directly from Eq. (12):

$$G_{B,SSi} = \frac{(n_{i,SiGe})^2 W_B N_B}{(n_{i,SiGe}^*)^2 D_B^*} \exp\left(\frac{q\Delta V_n + \Delta E_{C,SSi}}{kT}\right). \quad (13)$$

DC current gain is defined as $\beta = G_{E,SSi}/G_{B,SSi}$ [19], from Eqs. (12) and (13), we have the following relationship:

$$\beta = \left(\frac{1}{S_{pE}}\right) \left(\frac{n_{i,Si}^2}{n_{i,SSi}^2}\right) \left(\frac{n_{i,SiGe}^*}{n_{i,SiGe}}\right)^2 \left(\frac{D_B^* N_D}{W_B N_B}\right). \quad (14)$$

The product of R_C and C_{BC} in Eq. (5) represents the charge and discharge time of the BC depletion capacitor, which has a significant effect on the frequency of the SiGe HBT. There is a large amount of mobile charge in this region. The width of that depletion region is related to J_C . Under the condition of small injection or signal, if only the effect of V_{BE} on J_C is considered, C_{BC} can be approximated as:

$$C_{BC} = \frac{d}{dV_{CB}} \left[\left(qN_C - \frac{J_C}{v_s} \right) W_{BC} \right] \quad (15)$$

$$\approx \left(qN_C - \frac{J_C}{v_s} \right) \frac{dW_{BC}}{dV_{CB}}.$$

v_s is the electron saturation velocity in the collector region, W_{BC} is the width of the depletion region of the BC junction, and it is also related to J_C :

$$W_{BC} = \sqrt{2\varepsilon_{Si}(V_{bi} + V_{CB}) / (qN_C - J_C/v_s)}. \quad (16)$$

The uniaxial compressive stress in the collector region will narrow the forbidden bandgap of the collector region. Therefore, the built-in potential V_{bi} in the depletion region of the BC junction decreases and C_{BC} increases, but J_C is also affected by the stress. If the fraction y of the stress raiser is very small, the effect of stress on C_{BC} is also very small, then the effect of stress on C_{BC} is negligible [13]. In addition, considering that the stress of the embedded $Si_{1-y}Ge_y$ stress raiser in this work increases with increasing values of y , dislocations can be introduced within the collector region. The dislocations in Si and Ge are mainly prismatic ones that can form suspension chains, act as donor or acceptor, and have a compensating effect on the mobile carriers in the collector region. Also dislocations can be considered as scattering centers and can affect the mobility and resistivity of carriers, which will also affect the frequency characteristics of the device under greater stress.

4 Simulation Results and Analysis

According to the device structure shown in Fig. 1, the parameters of each active region are given in Table 1.

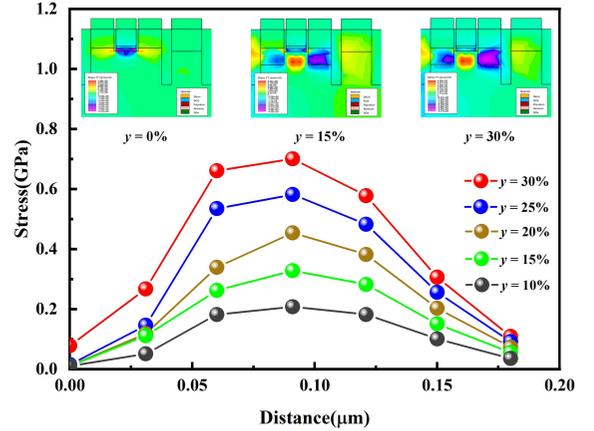


Fig. 3 Simulated result of longitudinal stress distribution in the collector

Fig. 3 shows the trend of uniaxial additional stress in the collector region along the electron transport direction for different values of the Ge fraction y in the stress raiser. It is obvious that

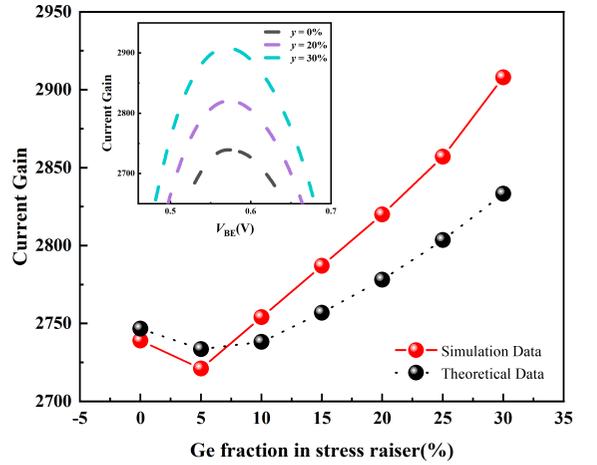
Table 1 Structure and technology parameters for simulations

| Region | Material | Thickness(nm) | Width(nm) | Doping(cm ⁻³) | Ge fraction(%) |
|----------------------------|--|---------------|-----------|---------------------------|----------------|
| N ⁺ Emitter | Polysilicon | 100 | 80 | 3×10 ¹⁹ | 0 |
| N ⁺ Emitter cap | Strain Si | 20 | 80 | 2.5×10 ¹⁸ | 0 |
| P ⁺ Base | Strain Si _{1-x} Ge _x | 30 | 80 | 2.5×10 ¹⁸ | 25 |
| Stress raiser | Strain Si _{1-y} Ge _y | 150 | 92 | 0 | 0-30 |
| N ⁻ Collector | Strain Si/Relaxed Si | 300 | 280 | 1×10 ¹⁷ | 0 |
| N ⁺ Collector | Relaxed Si | 200 | 340 | 1×10 ²⁰ | 0 |
| P ⁺ Substrate | Relaxed Si | 100 | 340 | 1×10 ¹⁵ | 0 |

the stress raiser can effectively introduce uniaxial stress into the collector region. With the increase of y , the additional uniaxial stress generated by the stress raisers increases significantly.

Fig. 4 shows the calculated variation of the current gain for different Ge fractions of stress raiser. When y is between 0 and 5%, the current gain decreases with the increasing stress. After that, it increases with the increase of the y , but the increase is very small. The reasons for this can be analyzed according to Eq. (14): y between 0 and 5% corresponds to very small stress (< 0.1 GPa). With such a small uniaxial compressive stress, the equivalent Ge fraction increase in the Si_{1-x}Ge_x base region is negligible. Along the [110] orientation of (100) substrate, the change of bandgap in the Si cap layer $\Delta E_{g,SSi}$, and the change of valence band edge $\Delta E_{V,SSi}$ is also very small. And the barrier height of the oxide-like layer to hole χ_h is usually about 1 eV [16]. So the tunneling probability P_T in Eq. (14) has little effect, which is approximately $\beta \propto \sqrt{m_h^*}$. The calculation results of the variation of the average holes effective mass of valence band show that, when the stress is in the range of 0 ~ 0.2 GPa, decreases greatly, resulting in β being slightly reduced. When the stress is greater than 0.2 GPa, the magnitude of bandgap shift increases with increasing stress. As a result, the accumulation of holes at the interface layer decreases significantly under higher stresses and the height of the holes barrier χ_h becomes a major factor in the continued increase in β . In general, the first and second terms to the right of the equal sign in Eq. (14) decrease as the stress increases, while the remaining terms increase as the stress increases. When the Ge fraction y is small, term 1 leads to a reduction in β . When y is increased, the magnitude of uniaxial stress is also increased,

then terms 3 and 4 mentioned above become the main factors that make β increase.

**Fig. 4** Variation of DC current gain with Ge fraction y in the stress raiser

It should be noted that various factors are affecting the characteristic frequency, and the theoretical analysis in the previous section is intended to provide a relevant physical basis for analyzing the effect of uniaxial stresses applied in the collector region on the frequency performance of the device. Combining the simulation results allows for an in-depth analysis of the physical mechanism affecting the frequency characteristics, rather than establishing a detailed physical model. The distribution of the applied uniaxial stress σ_{xx} along the x -direction of the collector is not uniform. By fitting the stress σ_{xx} distribution curve of Fig. 3, the average stress magnitude over the length of the transverse collector in the range 0 ~ L can be calculated as:

$$\langle \sigma_{xx} \rangle = \frac{1}{L} \int_0^L \sigma_{xx}(x) dx. \quad (17)$$

By substituting the calculation results of Eq. (17) into Eq. (4), the Ge fraction of the composite strained base region under additional uniaxial stress conditions can be obtained according to the relationship between the $\text{Si}_{1-x}\text{Ge}_x$ lattice constant and the equivalent Ge fraction x^* . The intrinsic carrier concentration of the base region and the diffusion coefficient can be then calculated, and the intrinsic carrier concentration of the strained Si cap layer can be obtained, as detailed in Ref. [20]. A comparison of the theoretical results calculated according to Eq. (14) with the simulation results in Fig. 4 reveals that the DC current gain is consistent with the variation pattern of the Ge fraction y , which can illustrate the correctness of the previous theoretical analysis. The reasons for the difference between the two are: (1) The thickness of the strained silicon capping layer is extremely thin, therefore, for the convenience of the analysis, it is approximated that the recombination of minority carriers in this layer and the effect of the thickness of the layer is ignored. (2) The interfacial state and the recombination velocity S_{pE} in the interface between strained Si cap layer and oxide-like layer depends on different process conditions, and more detailed physical modeling is dependent on the specific fabrication process. (3) Building a more accurate physical model of current gain also requires solving complex differential equations to calculate the distribution functions of the minority carriers and the magnitudes of various microscopic currents in the emitter region [16], which are beyond the scope of this paper.

Fig. 5 shows the variation curve of collector current J_C with BE junction voltage V_{BE} and stress. It can be seen that the uniaxial additional stress applied to the collector region does increase J_C . From Eq. (12), this is mainly due to the increase of the minority carriers' diffusion coefficient and the equivalent x in the base region, but there is no change in the order of magnitude. This is due to the fact that the effective bias voltage V_j falling on the Si/SiGe emitter junction decreases as the variation $\Delta E_{C,SS}$ in the conduction band of the strained Si cap layer increases. In general, J_C still increases with increasing y . As y

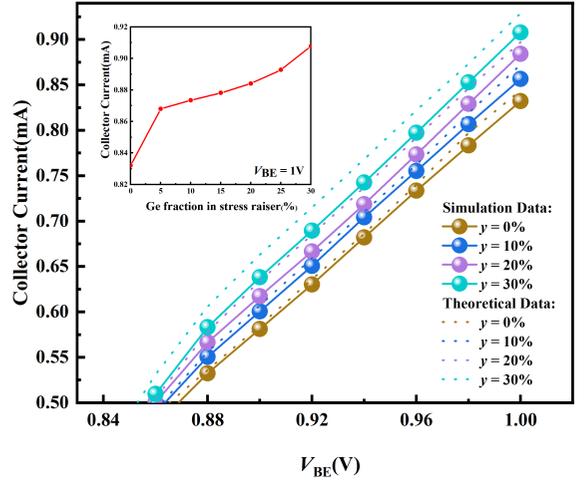


Fig. 5 Variation of collector current with Ge fraction in the stress raiser

increases, the recombination between stress raiser and collector region is enhanced by the increased prismatic dislocations, so the variation of J_C with y is not obvious. In addition, the theoretical calculation of the collector current according to Eqs. (12) and (13) are also given in Fig. 5, which exhibit a good agreement with the simulation results. This is because the electron current J_C is dependent on the energy band variation rather than the height of the oxide-like layer barrier and interface state [16].

According to the definitions of f_T and f_{max} , the value of characteristic frequency at a certain collector current I_C can be obtained for the variation curves of the common-emitter current gain H_{21} and the unidirectional transmission power gain U under small-signal conditions when both parameters are reduced to 0 dB. For example, the curves of H_{21} and U with frequency f were analyzed by AC simulation at different V_{BE} conditions for $y = 0.1$, as shown in Fig. 6 and Fig. 7.

By extracting the data from the curves, the frequency characteristic for different Ge fractions y can be obtained, as shown in Fig. 8 and Fig. 9. The cut-off frequency f_T and maximum oscillation frequency f_{max} are significantly increased compared to the case without stress raiser ($y = 0$), by about 29.1% and 71.5% respectively. The peak values of f_T and f_{max} reached 507.7 GHz and 730.7 GHz for $y = 0.15$ and $y = 0.1$, respectively, entering the “half-THz” band. According to the analysis presented above, the favorable factors

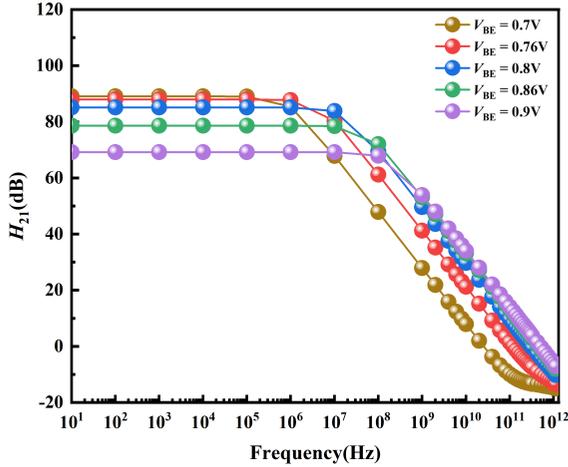


Fig. 6 Variation of small-signal current gain H_{21} with frequency f

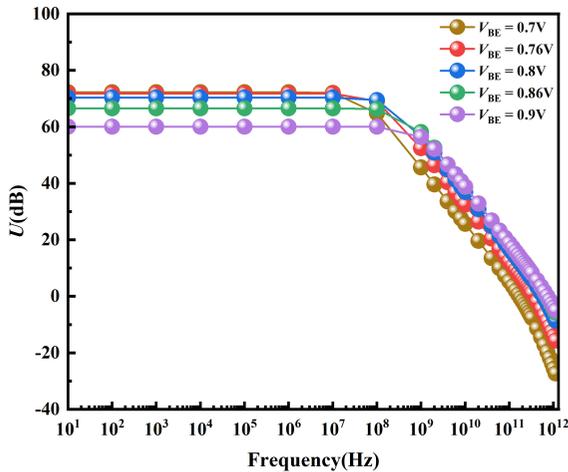


Fig. 7 Variation of unilateral power gain U with frequency f

leading to an increase in the characteristic frequency as the additional uniaxial stress increases are the increase of current gain, collector current, and interfacial recombination velocity. The additional uniaxial stress equivalently increases the Ge fraction of the base region, as illustrated in section 3, leading to an increased minority carrier diffusion coefficients and a simultaneous decrease in the resistance of in the working base region. The additional stress increases the carrier mobility and reduces the series resistance of the emitter and collector regions.

It can also be seen from Fig. 8 that f_T increases as y increases from 0 to 0.15 but decreases when y exceeds 0.15. Similarly, f_{max} increases as y

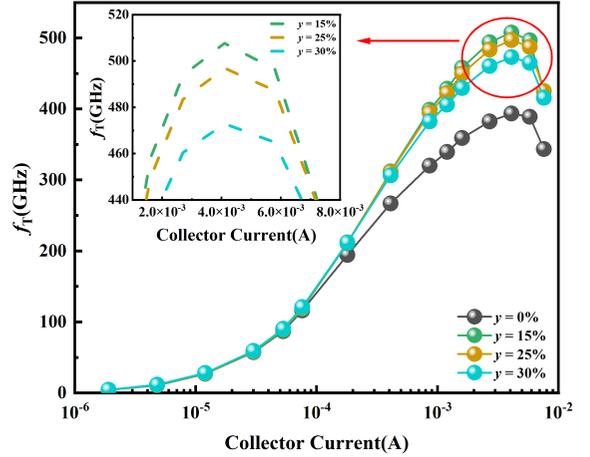


Fig. 8 Variation of the cut-off frequency f_T with Ge fraction y

increases from 0 to 0.1 but decreases when y beyonds 0.1. Referring to Eqs. (5), (14) and (15), it can be concluded that the reason for this situation is mainly the effect of prismatic dislocations in the collector region on the product $R_C \times C_{BC}$. For one thing, the dislocation compensates for the reduction of the free charge (J_C/qv_S) in the collector region, leading to an increase in barrier capacitance C_{BC} . Secondly, the lattice distortion caused by the dislocation becomes the scattering center of the carrier, and in the low-doped collector region, its ionization as the dominant center has an anisotropic scattering effect on the carrier, reducing the electron mobility, thus increasing the product $R_C \times C_{BC}$ in Eq. (5), resulting in a drop in f_T .

Fig. 9 depicts the variation trend of f_{max} with collector current and Ge fraction y . From Eq. (6), the trend is similar to that of f_T . At higher-level stresses, C_{BC} increases, so both f_T and f_{max} increase and then decrease as y increases. It should be noted that, however, the increase and decrease in f_{max} are greater than the change in f_T . In addition to the influence of C_{BC} , the base resistance R_B is also another dominant role. Qualitatively, this is most likely due to the thin base region, where the dislocations at the Si/SiGe interface act as a deep energy level, enhancing the recombination of the base region and reducing the concentration of holes in the base region. At the same time the dislocation scattering also hurts the mobility of the base region majority carriers. The concentration compensation and scattering effect

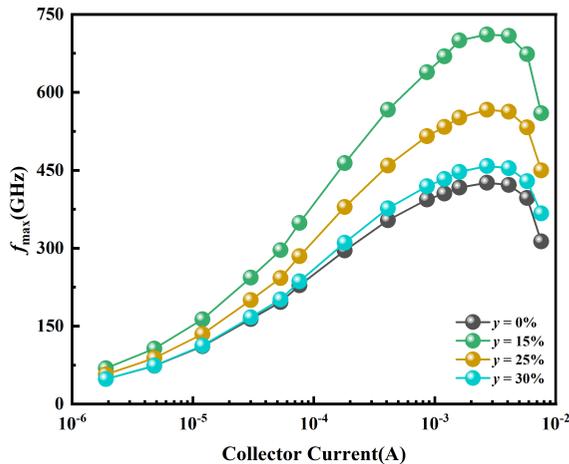


Fig. 9 Variation of the maximum oscillation frequency f_{\max} with Ge fraction y

of dislocation on the base region majority carriers leads to the increase of R_B more than the increase of f_T , thus worsening the f_{\max} .

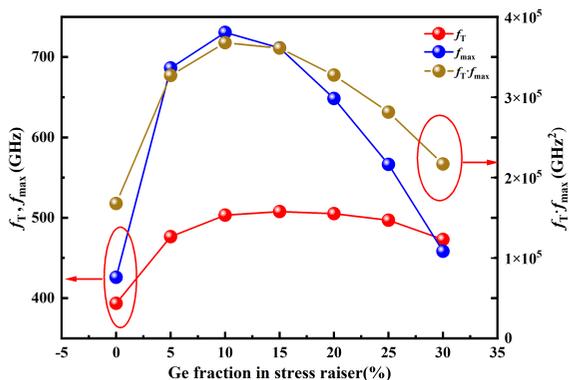


Fig. 10 Variation of $f_T \times f_{\max}$ with Ge fraction y

For more visual analysis of the frequency characteristics, Fig. 10 shows the variation of f_T and f_{\max} peaks for different Ge fractions y . It is clear from this that the Ge fractions corresponding to the two peaks are different, and it is not straightforward to obtain the optimal value of the Ge fraction for the design of device to achieve the best frequency performance. For this purpose, the Ge fraction can be determined by determining the peak of the product $f_T \times f_{\max}$. It is clear from the graph that $f_T \times f_{\max}$ peaks at $y = 0.1$ and that the overall performance is optimal for the frequency characteristics.

5 Conclusion

In this work, a device structure for a scaled SiGe HBT with an embedded $\text{Si}_{1-y}\text{Ge}_y$ stress raiser in the collector region is designed. Under additional stress, the theoretical analysis shows that the improvement of the frequency characteristics is mainly due to the change of the strained Si/SiGe band structure, as well as the improvement of the physical parameters such as the DC current gain, the interface recombination rate in the emitter region and the $R_C \times C_{BC}$ product, while the effect of the dislocation scattering caused by the stress on the relevant physical parameters is also taken into account. The simulation results show that the introduction of additional uniaxial compressive stresses in the collector region can indeed significantly improve the frequency performance of the device, and the Ge fraction y can be flexibly adjusted to achieve different degrees of enhancement of the characteristic frequency. In particular, the cut-off frequency f_T reaches a maximum at $y = 0.15$, which is close to the Ge fraction of the SiGe source-drain in a strained Si PMOS in a 90 nm process. Moreover, the device structure designed in this work is similar to that of PMOS and is therefore easily integrated with strained Si CMOS processes, resulting in a BiCMOS device structure with a smaller size or layout region and better performance. The research in this work can provide a theoretical basis for the design of future silicon-based Terahertz Devices and ICs, and has some potential application value. In addition, this work only investigates the physical parameters of the device that affect the characteristic frequency, and it is believed that on this basis, by further optimizing the process structure and parameters of the device, even better frequency characteristics can be obtained.

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