Comparative Analysis of Quality Factor and Digital Inverter Performance in Gate Underlap and Overlap DMG FinFETs

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Research Article

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Abstract

This paper presents a comparative 3D simulation study of Quality factor among Gate Underlap and Overlap techniques in both Si and Ge Dual Material Gate (DMG) FinFETs using the Sentaurus TCAD tool. The results of both the techniques are carefully examined and compared with Conventional DMG FinFET to analyze the performances of these devices. The effect of gate overlap/underlap techniques on threshold voltage (V_{th}), I_{ON}/I_{OFF} ratio, drain induced barrier lowering (DIBL), transconductance (g_m), subthreshold swing (SS), and Quality factor (Q) are investigated. It is found that DMG Ge FinFETs have higher g_m and quality factor values as compared to DMG Si FinFETs. The prospects of these techniques in low-power digital applications have been performed by implementing complementary DMG FinFET based inverter circuit. We have extracted the average delay and noise margin where it renders better performance such as high current gain and no overshoot and undershoot peaks in the transient characteristics.

I. Introduction

The scaling of semiconductor devices in the manufacturing industry leads to a new technology node and thus, there is a need to reinvent fundamental transistor architecture and manufacturing processes or both [1–2]. Also, in order to follow Moore's law [3], we have to shrunken dimensions in the nanometre regime. Scaling favours an exponential increase in density of chips with the decrease in power dissipation but it also degrades the performance in terms of short channel effects (SCEs) [4–8]. In short-channel devices, the distance between source and drain regions is reduced when the channel size is small underlies [9], which leads to excessive leakage current. In this regard, Fin Field Effect transistor (FinFET) is one of the favourable advanced MOS devices used in today's advanced microprocessors [10], GPUs [11], and other high-density processors. FinFET has vertical double gates which lead to stronger electrostatic control over the channel and thus, improved its short channel behaviour [12–14]. The performance of conventional FinFET can further be improved by various techniques such as gate engineering, work function engineering, and structural engineering. In Dual material Gate (DMG) [15–16] technology, two different materials with different work functions are used as gate material and here, the work function gate metal near the source is kept higher compared to drain. Such structure is used to improve the transportation efficiency of the device and it also improves the SCEs [17–19]. In addition to gate engineering [20], the concept of channel engineering [21] gate with source/drain underlap and overlap regions also has been an attractive option to enhance the electrical performance along with suppressed SCEs. The FinFET structures with both underlap and overlap regions have been demonstrated in the literature [22]. FinFETs with abrupt or graded overlap show a higher leakage current [23] as the technologies are scaled down in the nanotechnology regime but it offers a very good ON current. On the other hand, the underlap structure received substantial attention in recent years [24–26] as it provides a lower leakage current due to its ungated region. Sachid *et al*., demonstrated the use of high-k spacers in FinFETs with underlap regions to augment the effect of gate fringe induced barrier lowering (GFIBL) which is used to ameliorate the ON current [24]. Further, researchers have investigated the sensitivity of underlap lengths on AC and DC

parameters of FinFETs [25]. Effects of gate work function variation on the performance of underlap structure is also studied [27]. FinFETs also have been investigated with materials beyond Silicon like Ge [17, 27] and GaN [28]. Das *et al.* highlighted the quality factor in GaN FinFET for various supply voltage [28]. However, a comparative study in terms of g_m vs. SS, quality factor, and digital inverter performance for underlap and overlap FinFETs are not yet reported in literature.

In this paper, a comprehensive study among gate underlap, gate overlap, and conventional DMG FinFETs is reported in terms of the transfer characteristics, subthreshold swing (SS), drain induced barrier lowering (DIBL), I_{ON}/I_{OFF} ratio, and threshold voltage for two different channel material Si and Ge. Furthermore, we have highlighted the gm vs. SS and quality factor of these FinFETs using TCAD simulator. Finally, the delay parameters and the noise margins are calculated from transient and transfer characteristics by implementing the digital inverter of these FinFETs. This paper is divided into four sections: Section 2 describes the device structure and models used in the simulation study, Section 3 discusses the various results obtained from the simulator, and finally, the paper is concluded in Section 4.

I I. Device Structure And Simulation Setup

In this study, DMG Si and Ge FinFETs are used for comparison in Gate Overlap and Gate Underlap structures. The 3-D DMG-FinFET architecture is shown in Fig. 1(a) and its Gate Overlap and Gate underlap structures are portrayed in Figs. 1 (b) and (c), respectively. The designed devices have dimensions of channel length (L_G) 20 nm, fin thickness (T_{FIN}) is 10 nm, the oxide thickness (T_{OX}) of 2 nm, and the gate-electrode thickness (T_G)is 2 nm. The doping concentration of the n^+ Source/Drain region is kept at 10^{20} cm^{-3}, while the channel doping concentration is considered as 10^{15} cm^{-3}. The lightly doped channel maximizes the effective mobility and hence, the ON current of the device is improved. The Gate overlap doping values are kept at 10^{20} cm^{-3}, whereas, the underlap doping values are kept at 10^{15} cm^{-3}. The Gate underlap and overlap region lengths are taken 4 nm from both Drain and Source sides.

The simulations have been performed using the multidimensional Sentaurus TCAD tool by Synopsis [29]. A calibration of the TCAD physics model with the experimental data is performed to get realistic data from the simulator. The Drift-Diffusion (DD) model is used as the transport model because the device did not enter into the non-equilibrium region and not a very high electric field is applied. The DD transport model solves Poisson and carrier continuity equations for electrons and holes consistently within the specified boundary conditions. SRH recombination model is considered for recombination and generation rate. The doping-dependent Masetti model with tuned mobility parameter is used to check the effect of doping concentration on the mobility of charge carriers. The Fermi-Dirac statistics model is turned on along with the Old Slotboom model for including Bandgap Narrowing to prevent tapering of bandgap in highly doped Source and Drain regions. The work function of the source side gate material is kept higher (Φ_m = 4.8 eV) and lower on the drain side (Φ_m = 4.3 eV). The Drain to Source supply voltage is kept at V_{DS}=0.5 V. A good agreement of the experimental data with simulated data is shown in Fig. 2.

I I I. Results And Discussion

In this section, the performance metrics of Silicon on Insulator (SOI) DMG FinFET devices have been compared. This comparative study has been carried out among three DMG FinFETs for both Si and Ge materials: Conventional FinFET, Gate Underlap FinFET, and Gate Overlap FinFET structures. These three device structures also have been implemented in digital logic inverter circuits to study the exact behavioural characteristics in low-power digital applications.

III. A: DC Performance Investigation

The Transfer characteristics of three DMG FinFET structures for both Si and Ge are shown in Figs. 3 (a) and (b) in linear and log scales, respectively. From the graphs, it is observed that the DMG Ge FinFET structures have higher ON current drivability because of lower bandgap and high electron mobility as the potential barrier is lower compared to Si-based FinFETs. Figure 3(a) shows the Gate Overlap devices have good drain current (I_{ON}) as compared to Conventional and Gate Underlap FinFETs. This is due to more electrostatic control of the gate over the channel in overlap devices. Figure 3(b) shows the Underlap FinFETs have less leakage current (I_{OFF}) than conventional and overlap devices. This is due to the reduced parasitic source/drain resistances as the effective channel length increases and therefore, there is current deterioration in the ungated region.

The prominent characteristics of each device used in the study can also be explained by the two-dimensional (2D) cross-section of electron density in the channel region. The 2D cross-section of electron density profiles of all six devices in the X-Z plane is shown in Fig. 4. By closer look at the cross-section of electron density profiles, it is evident that the electron concentration in the channel of gate overlap FinFET is more compared with Conventional and Underlap FinFETs for both Si and Ge materials. The root cause of it is due to enhanced gate control over the channel in overlap structure. It is also visualized that due to having a lower bandgap the Ge device has improved electron density than Si. Figure 5 (a) shows the variation of threshold voltage (V_{th}) for conventional, gate underlap, and gate overlap FinFETs. The maximum transconductance method is used for V_{th} extraction during simulation. The higher drain current of the device will require a lower threshold voltage to turn it ON and the same is demonstrated by the graph in Fig. 5 (a). Thus, DMG Ge FinFETs have lower V_{th} values than DMG Si FinFETs. Moreover, the gate overlap FinFET shows the lowest threshold voltage as it has the highest ON current among the three structures. Also in the Overlap structure, the effective channel length decreases which leads to the lesser threshold voltage. For the case of underlap structure, there is an extension of underlap regions from both drain and source sides, hence the effective channel length increases. Therefore, an increase in channel length leads to an increase in threshold voltage for underlap FinFET.

Another common figure of merit for a device is I_{ON}/I_{OFF} ratio, a higher value of this ratio is desirable. This ratio has a remarkable impact on the static power consumption in low standby power applications. This is an important parameter that decides the figure of merit for having high performance (more I_{ON}) and low leakage power (less I_{OFF}) of transistor devices. From Fig. 5 (b), it is observed that underlap structure

shows the highest I_{ON}/I_{OFF} ratio for both Si and Ge as it has the lowest leakage current in its drain characteristics (Fig. 3) which makes it suitable to be implemented in low power devices. The maximum attainable value for I_{ON}/I_{OFF}ratio is found to be $1.57x10^6$ for Si and $1.43x10^6$ for Ge Underlap FinFETs.

Figure 5(c) shows the comparison of DIBL values in three structures for Si and Ge fin material. DIBL is the key parameter that describes the electrostatic integrity of the device and it is basically a reduction in the threshold voltage of the device at higher drain voltages. It is calculated from the Sub-threshold characteristics by taking the horizontal shift caused by a change in the V_{DS} on the log I_{DS}-V_{GS} plot. It causes lowering of the Source barrier height that results in a further decrease of the threshold voltage at high drain bias. DIBL is expressed as [31]:

$$DIBL = \left[\frac{(V_{th1} - V_{th2})}{(V_{ds1} - V_{ds2})}\right] \quad (1)$$

Where V_{th1} is the threshold voltage extracted at a low drain bias of V_{ds1}=0.05 V and V_{th2} is the threshold extracted at a high drain bias of V_{ds2}= 0.8 V. In the case of symmetrical Underlap structure, the effective channel length is the distance between Source and drain ends (L_{SD}), which can be given as L_{SD} = L_G+2L_{UN}. The effect of drain potential on the channel decreases due to the $L_{UN,}$ drain being away from the gate and thus DIBL decreases. From the literature, it is found that DIBL dependence on L_{UN} is more for shorter lengths and is less for longer lengths [32] so, L_{UN} is chosen 4nm in this study. It is seen that DMG Ge FinFETs have lower DIBL values than DMG Si FinFETs.

III. B: *AC Performance Investigation*

The ON and OFF states performance of a device is determined by plotting g_m vs. SS at three different V_{DS} = 0.3, 0.5, 0.8 V as illustrated in Fig. 6 for both Si and Ge DMG FinFETs. DMG Ge FinFETs have higher g_m and SS values than DMG Si FinFETs. g_m is defined as the partial derivative of drain current with respect to the gate voltage at fixed drain to source bias and it can be expressed as [31]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \mid constant, V_{DS} \quad (2)$$

From Fig. 6, it is observed that the g_m value is high for overlap structures while the SS value is found less for underlap structures. It is also seen that there is improvement in g_m with degradation in SS as V_{DS} is changed from 0.3 to 0.8 V. SS characterizes the switching characteristics of the device means how fastly the device can switch between OFF and ON states. For this to happen, below threshold voltage there should be a very large change in drain current with very small change in gate voltage. Sub- threshold swing is given as [31]:

$$SS = \frac{\Delta V_G}{\Delta(log I_D)} \quad (3)$$

The qualitative device performance can also be assessed with the help of the Quality factor (Q) and it is defined as the ratio of transconductance gain with sub-threshold swing (g_m/SS) [28]. The Q of these three structures are shown in Figs. 7(a) and (b) for Si and Ge, respectively. DMG Ge FinFETs have a high value of g_m than DMG Si FinFETs, which leads to improved Quality factor. From the results, it is evident that Overlap structures have high g_m and lower SS value compared to other structures; hence it has highest quality factor and a potential candidate for RF applications. The exact behavioural characteristics of different DMG FinFET Structures in low power applications are studied by implementing them in digital inverter circuit, which is discussed in consecutive section.

III. C: *Digital Inverter Performance Investigation*

The architecture of the complementary Si DMG FinFET inverter circuit is implemented by using both p-DMG FinFET and n-DMG FinFET is shown in Fig. 8(a). The I_D-V_G characteristics of both n-DMG Si FinFET and p- DMG Si FinFET for three different structure is shown in Fig. 8(b) and it is seen that both p and n-type devices shows similar I_{ON}/I_{OFF} ratio. The inverter transient characteristics at V_{DD}=2 V of these three architectures are portrayed in Fig. 8(c). It is revealed from Fig. 8(c), there is no overshoot and undershoot in the transient characteristics at load capacitance (C_L) of $3x10^{-16}$ F.

Table 1
Comparison of propagation delay parameters

Delay parameters	Conventional	Overlap	Underlap
t_{PLH} (ps)	1.76	1.68	1.7
t_{PHL} (ps)	0.182	0.28	0.22
Average delay (ps)	0.971	0.984	0.96

From the inverter transient characteristics, the propagation delay parameters [33] have been calculated as stated in Table 1. As anticipated the t_{PHL} value is lower than t_{PLH}. Through calculations, it is found that gate Overlap structure has slightly more average delay than conventional as it is having more parasitic capacitances in the gate-drain region.

Table 2
Comparison of Noise Margin parameters in three different Si DMG FinFET Structures

Structures	V_{OH} (V)	V_{IL} (V)	V_{OL} (V)	V_{IH} (V)	$N_{MH} = V_{OH}-V_{IH}$ (V)	$N_{ML} = V_{IL}-V_{OL}$ (V)
Conventional	1.490	0.5398	0.00030	0.8774	0.6126	0.539
Overlap	1.498	0.5253	0.00044	0.8156	0.6824	0.524
Underlap	1.494	0.5770	0.00091	0.819	0.675	0.576

Figure 9 shows the voltage transfer characteristics (VTC) of the inverter circuit. The inverter gain is a function of the slope of the drain current in saturation as well as of V_{DD} [34]. The gain of the inverter actually increases with the reduction of supply voltage. The Overlap structure shows more steepness in the logic transition that implies higher current gain than the other two structures considered under this study, as demonstrated in Fig. 9. The gain of a circuit can be characterized by the relation of input high voltage (V_{IH}) and input low voltage (V_{IL}) as [34]:

$$V_{IH} - V_{IL} = -\frac{V_{DD}}{gain} \qquad (4)$$

Lower values of V_{IH} and V_{IL} results in a higher gain. From the VTC characteristics (Fig. 9), the Noise Margin parameters [33–35] have been measured as shown in Table 2. There are two noise margins must be considered in logical inverter one is noise margin high (N_{MH}) and the second one is noise margin low (N_{ML}). For the proper operation of the logical inverter, V_{OH} has to be greater than V_{IL} for detection of logic1' and V_{OL} has to be less than V_{IL} for detection of logic 0'. Noise margin is greater if V_{OH} is closer to the power supply and V_{OL} is closer to zero. From the Table 2, it is found that both gate overlap and underlap structures have higher noise margin than conventional structure.

I V. Conclusion

In this work, a comparative study of transfer characteristics, SCEs, gm vs. SS, and quality factor are reported among conventional, overlap and underlap DMG FinFET structures considering two different channel materials Si and Ge. Further, their potential in lower power digital applications is also analyzed by implementing them in the inverter circuit. DMG Ge FinFETs have improved drain current, g_m, quality factor with degraded SS than DMG Si FinFETs. However, the gate underlap structure has the lowest leakage current which effectively reduces SCEs and thus, it is suitable for low power applications. The gate overlap structure has high drain current, transconductance and quality factor; so it is good for RF applications. From the transient characteristic, it can be concluded that the absence of overshoot and undershoot make them suitable for low-power digital applications. The high state Noise Margin is high

for Gate Overlap structure, whereas, the Underlap structure is suitable for low state noise margin. Moreover, less propagation delay is obtained for underlap DMG FinFET.

Declarations

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Competing interests:

The author does not have involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript. The author declares that there is no conflict of interest in this manuscript.

Author contributions: The work as well as the manuscript is written by Rashi Chaudhary. The grammatical corrections in this paper have been done by Rajesh Saha.

Availability of data and material: There is no any other data and material associated with this manuscript.

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Figures

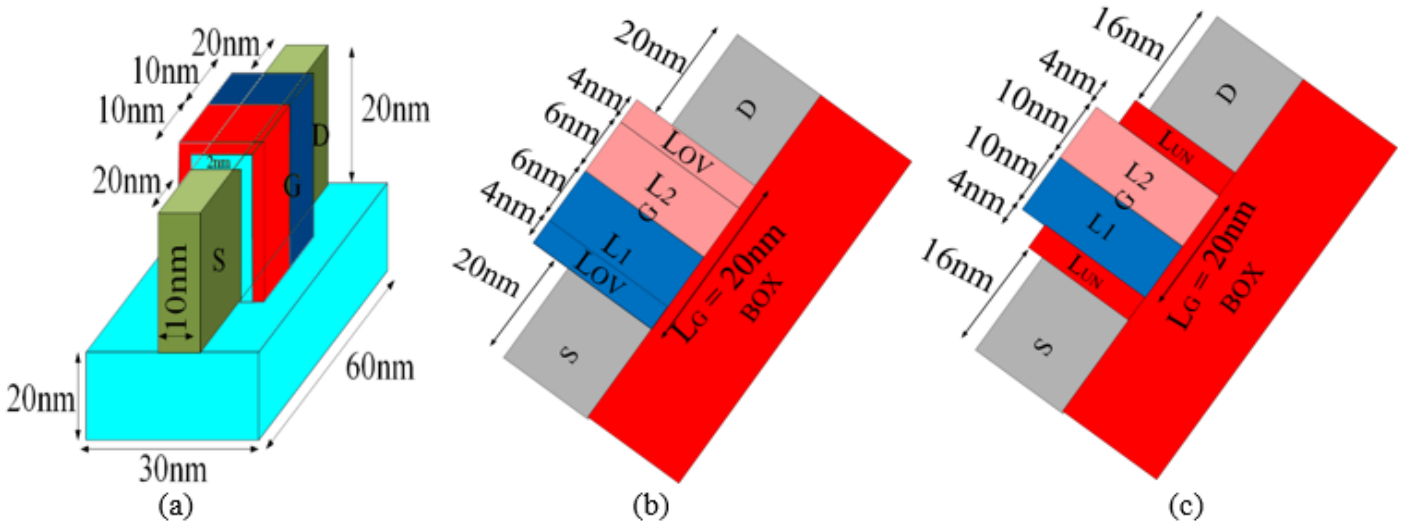

Figure 1

3D Structures of (a) DMG Conventional FinFET (b) DMG Overlap FinFET, and (c) DMG Underlap FinFET.

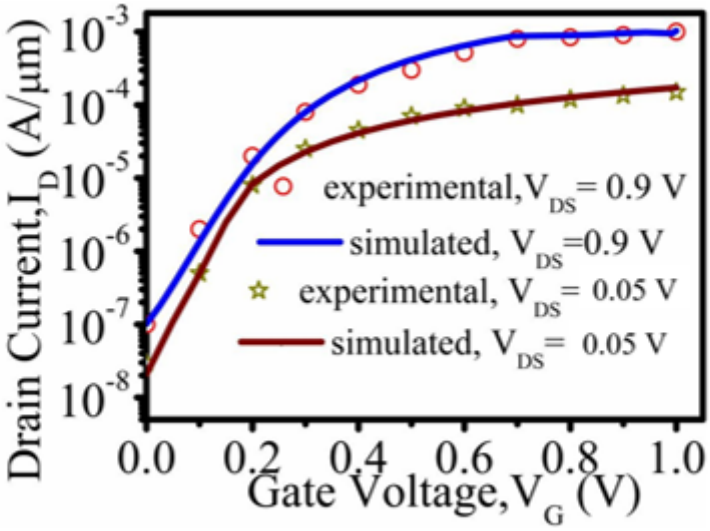

Figure 2

Calibration of TCAD model with the experimental data [30]

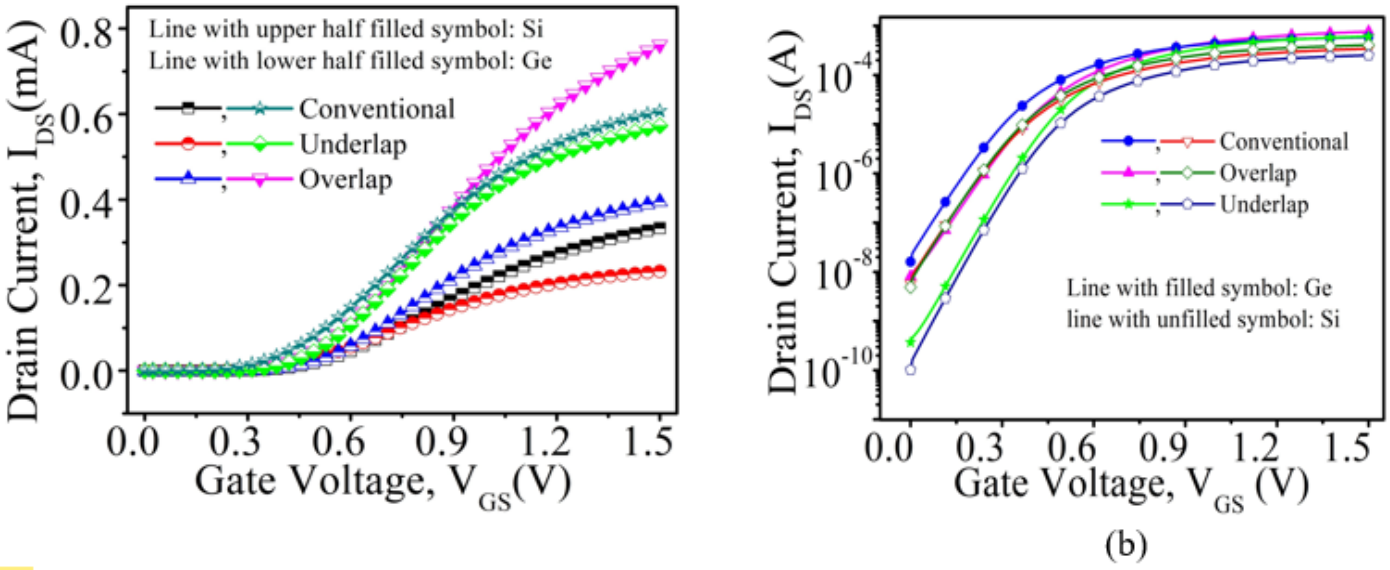

Figure 3

I_D-V_G characteristics of these three structures in (a) linear and (b) log scale.

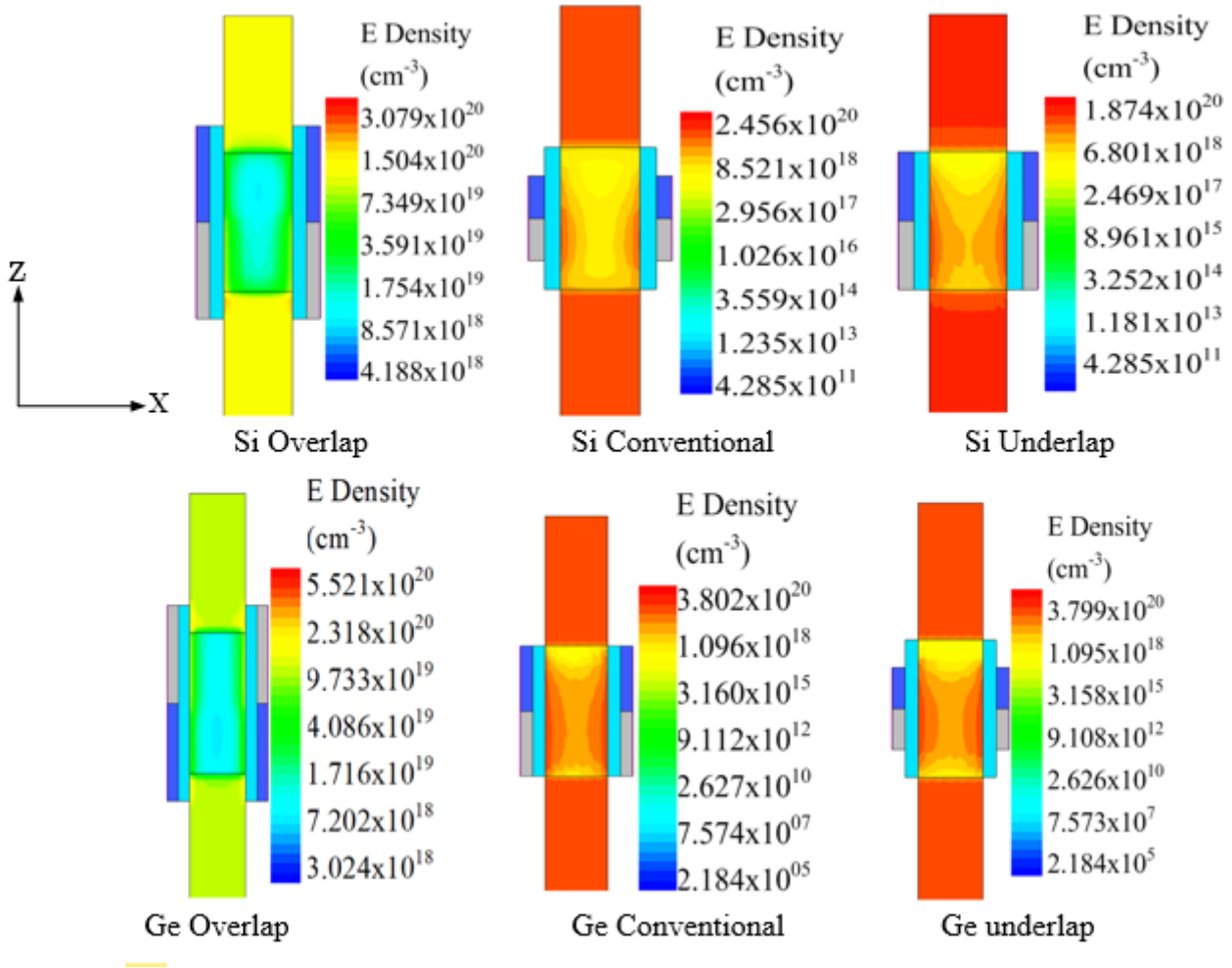

Figure 4

2D cross-section electron density profiles of DMG FinFET Structures.

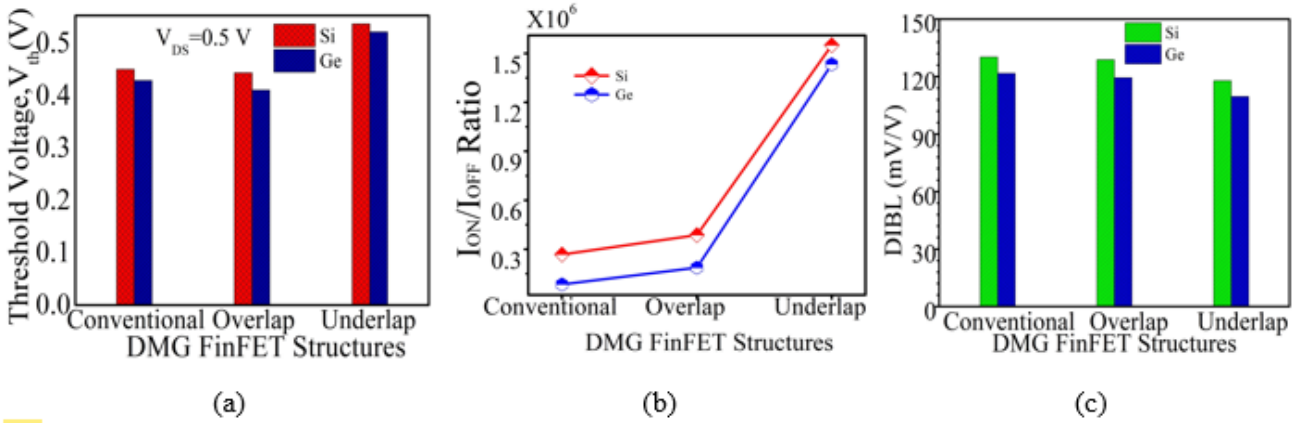

Figure 5

Comparison of (a) threshold voltage (V_{th}), (b) I_{ON}/I_{OFF} ratio, and (c) DIBL for different DMG FinFET structures.

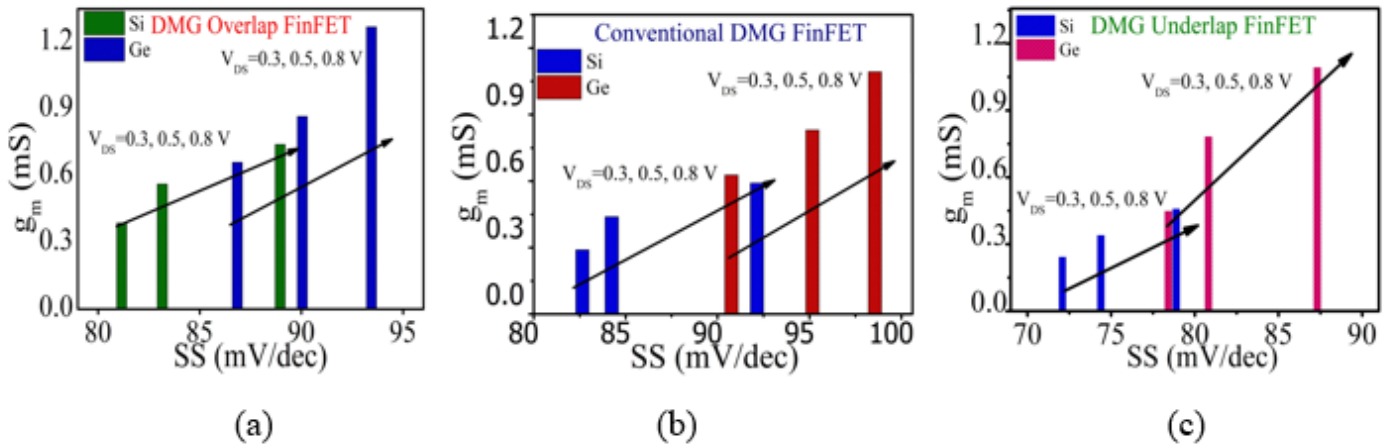

Figure 6

Plot of g_m vs. SS at different V_{DS} for (a) Overlap, (b) Conventional, and (c) Underlap DMG FinFETs for both Si and Ge.

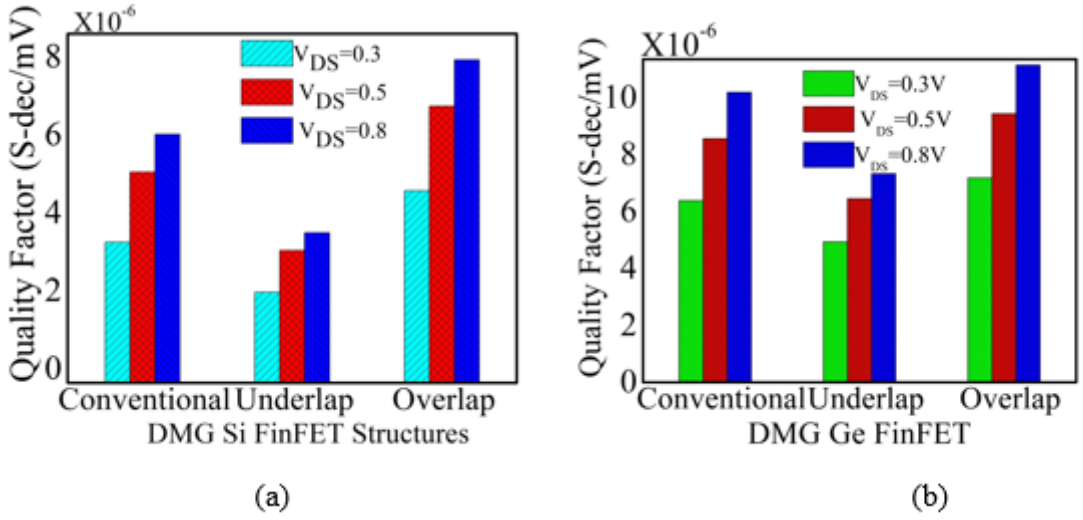

Figure 7

Comparison of the Quality factor of different structures for V_{DS} = 0.3, 0.5, and 0.8 V.

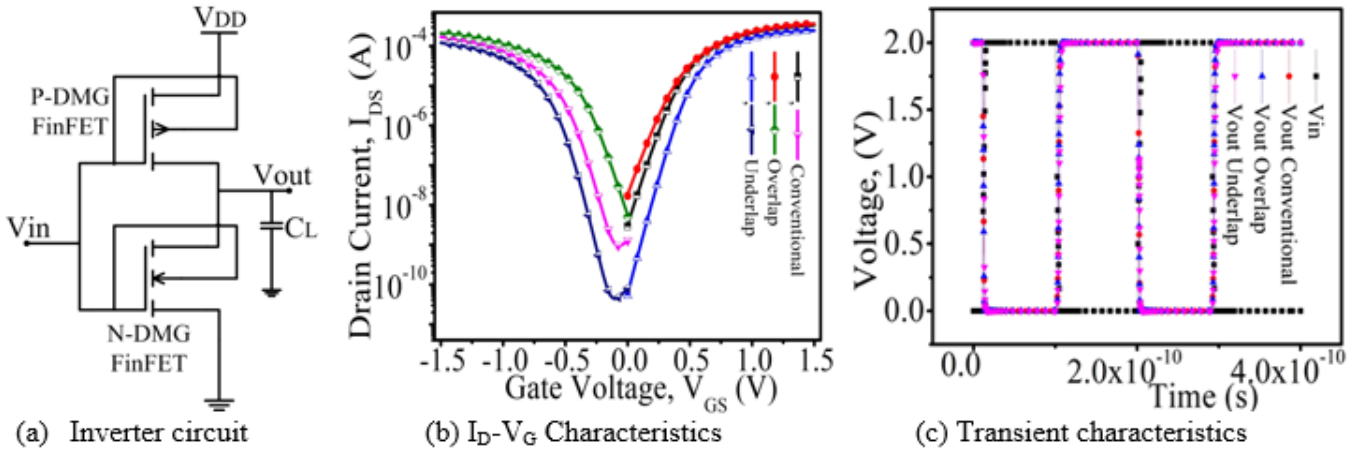

Figure 8

Performance Comparison of different Si DMG FinFET Structures in Inverter for low power application.

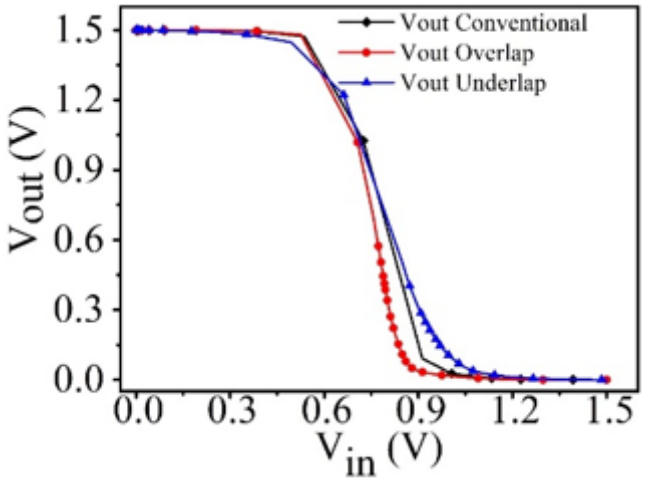

Figure 9

VTC of the inverter circuit.