The Common Mode Voltage Control Using a Hybrid Compensation Structure and Derivative Method

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Article

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The Common Mode Voltage Control Using a Hybrid Compensation Structure and Derivative Method

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ABSTRACT In this paper, the hybrid compensation loop is introduced to the front end of the load, which can increase the electromagnetic interference current shunt loop, and basically eliminate the common mode noise in the three-phase inverter from the perspective of the interference source. The expressions of the controlled voltage source and the parameter calculations of the shunt path are given in detail. The state of the controlled voltage source is determined by the instantaneous voltage of each phase bridge arm, which has already included the sequence of pulse width modulation, so the common mode noise can be eliminated under different modulation modes. An active method of suppressing common mode (CM) is proposed to regulate the high-frequency CM voltages on the AC buses with respect to the ground. The resultant CM compensation voltages are rendered symmetric to the AC common mode noise, so that load midpoint voltage relative to ground remains constant or zero. The experimental results demonstrated that the common mode voltage can be suppressed by the added compensation circuit effectively under the 2D-SVPWM non-zero vector modulation and 3D-SVPWM non-zero vector modulation. The amplitude, harmonics and frequency of the load voltage isn't affected by the method of eliminating the common mode voltage.

INDEX TERMS the hybrid compensation structure, electromagnetic interference, DC-AC power converters,

I. INTRODUCTION

With the rapid development of power electronics technology, the power electronic devices have been widely utilized in various fields due to their excellent energy-saving features and flexible power conversion capabilities. However, the high switching frequency of power electronic devices and the high power density lead to the complicated electromagnetic environment inside the converter. The electromagnetic interference includes conducted interference and radiated interference, which is harmful to the normal operation of converter and the surrounding electronic devices. Conducted interference can be divided into common mode (CM) and differential mode (DM), and common mode interference has a greater impact on the system. The three-phase inverter is widely used in variable-frequency drives, solar energy systems, electric vehicles and the like. Due to common mode voltage, the system reliability is reduced and the failure rate is increased, especially in high voltage and large-capacity systems. Therefore, it is of great concerns to study the conduction interference path and its suppression method, which could affect the converter performance, electromagnetic interference (EMI) prediction, filter design, and electromagnetic pollution reduction.

It is known that, the traditional way for CM interference suppression is to use filter as the compensation method. On the one hand, prevent the spread of electromagnetic interference to the external circuit, and on the other hand, prevent internal circuitry from the interference generated by the different uncontrollable converter. At present, compensation methods commonly used is the active compensation. Videt, Arnold et al provide complete elimination of the CM voltage by synchronizing all the commutations of one converter with commutations of another, so that the overall resulting CM voltage does not vary. [1,2] Paper[3] put forward a feed-forward voltage-detecting-voltage-compensating structure, reduced the CM noise. Paper [4] discusses a CM active EMI filter modeling. The single-phase full-bridge inverter is used to inject the compensation currents into the DC-side of the two three-phase half-wave rectifier, which can reduce the harmonic.[5] Christina M. DiMarino, Dushan Boroyevich proposed an integrated screen increasing the partial discharge inception voltage to reduce the common-mode current by ten times. [6,7] Bingyao Sun, Hemant Bishnoi et al use EMI behavioral models to predict the common mode emissions in the conducted EMI range (150 kHz- 30MHz). [8,9] In paper[10], the proposed control algorithm based on various PM scenarios in terms of injection low and high active power and suitability of energy sources are tested under balanced and unbalanced conditions.

Dahidah M S A et al provide eliminating a set of harmonic components or minimizing the weighted sum of squares of the magnitudes of a set of harmonics so that the energy from the fundamental frequency spreads between sub-harmonics to reduce spectral energy peaks.[11-13] In paper [14,15], the pulse center is randomly offset from the middle of the cycle. This offset is randomly determined within the frequency band limited by the maximum duty

cycle. The common method of EMI suppression interference is to reduce the voltage change rate d*u*/d*t* and the current change rate d*i*/d*t* of the switching device, which include adding soft switches[16-19], gate drive circuits and snubber circuit[20-22]. The common passive filters include DM filters composed of DM choke coils and X capacitors, CM filters composed of CM choke coils and Y capacitors.[23-30]

In this paper, the numerical relationship between CM voltage and each node voltage in three-phase voltage source inverter is discussed, and the hybrid compensation loop eliminating common mode voltage is proposed. The theoretical formulas have been provided to eliminate the CM voltage completely. The parameter calculation between the instantaneous voltage of the controlled voltage source and the midpoint voltage of each arm is analyzed in detail. The backward current introduced by controlled voltage source eliminates the CM noise completely. So the controlled voltage source to suppress circulating current has already included the sequence of pulse width modulation. This method isn't affected by the algorithm. The results that CM voltage is suppressed significantly are shown in experimental section.

II. THE THREE-PHASE INVERTER TOPOLPGY

The mathematical model of the voltage-source inverter is built to analyze and study EMI noise in three-phase inverter. The every variable is used as a scalar to build three-phase scalar system model.

A. THE MAIN CIRCUIT STRUCTURE

As shown in Fig.1, the three-phase inverter includes the DC power U_{dc}, three-leg main circuit, three-phase filter, three-phase symmetrical loads, and the positive direction of all currents are shown in Fig.1. The three-leg main circuit consists of six power devices MOSFET (S_1-S_6). The upper and lower power devices of the each-arm is not turned on at the same time, that is, a complementary working mode is adopted.

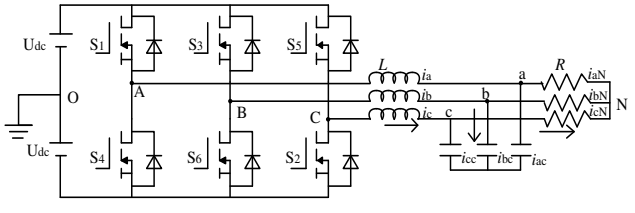


FIGURE1. Three-phase inverter

Taking into the current of the filter wave inductor as a state variable, according to Kirchhoff's voltage law, the corresponding state equation can be written, as in

$$\begin{cases} u_{\mathrm{AO}} = L\dfrac{\mathrm{d}i_{\mathrm{a}}}{\mathrm{d}t} + Ri_{\mathrm{aN}} + u_{\mathrm{NO}} = L\dfrac{\mathrm{d}i_{\mathrm{a}}}{\mathrm{d}t} + u_{\mathrm{aO}} \\ u_{\mathrm{BO}} = L\dfrac{\mathrm{d}i_{\mathrm{b}}}{dt} + Ri_{\mathrm{bN}} + u_{\mathrm{NO}} = L\dfrac{\mathrm{d}i_{\mathrm{b}}}{\mathrm{d}t} + u_{\mathrm{bO}} \\ u_{\mathrm{CO}} = L\dfrac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} + Ri_{\mathrm{cN}} + u_{\mathrm{NO}} = L\dfrac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} + u_{\mathrm{cO}} \end{cases} \tag{1}$$

Where u_{AO}, u_{BO}, u_{CO} denotes the instantaneous voltage of the midpoint of each bridge arm relative to the input side grounding point, *L* is the inductance of the LC filter, and *R* is the symmetric load, which u_{aO}, u_{bO}, u_{cO} is the instantaneous moment of the load input terminal relative to the DC input side grounding point.

According to Kirchhoff's current law, the current $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ flowing through the inductor is determined, as in

$$\begin{cases} i_a = i_{ac} + i_{aN} \\ i_b = i_{bc} + i_{bN} \\ i_c = i_{cc} + i_{cN} \end{cases} \tag{2}$$

Where, i_{ac}, i_{bc}, i_{cc} are the currents flowing through the three capacitors of the *LC* filter.

Considering the three-phase symmetrical connection system from Figure.1, the three-phase load of the three-phase inverter and the three-phase capacitor of the *LC* filter are all star-connected. According to Kirchhoff's current law, (3) is obtained:

$$i_{ac} + i_{bc} + i_{cc} = 0, i_{aN} + i_{bN} + i_{cN} = 0 \tag{3}$$

Equation (2) can then be written as:

$$i_a + i_b + i_c = 0 \tag{4}$$

According to (4), the three equations in equation (1) are added to obtain, as in

$$u_{AO} + u_{BO} + u_{CO} = 3u_{NO} = u_{aO} + u_{bO} + u_{cO} \tag{5}$$

B. ANAYSIS OF COMMMON MODE INTERFERENCE IN THE THREE PHASE INVERTER

The common-mode voltage on the output side of the three-phase inverter is the potential difference between the midpoint of the output load and the reference ground. The star-connected resistors are showed, and the midpoint O of DC input side of three-phase inverter provides a referent ground as shown in Fig.1. According to the definition and Eqn.(5), u_{NO} is the common-mode voltage, and can be showed in (6) :

$$u_{\mathrm{cm}} = \frac{1}{3}(u_{\mathrm{aO}} + u_{\mathrm{bO}} + u_{\mathrm{cO}}) = \frac{1}{3}(u_{\mathrm{AO}} + u_{\mathrm{BO}} + u_{\mathrm{CO}}) = u_{\mathrm{NO}} \tag{6}$$

Where, u_{cm} is the common mode voltage. There is a rate of voltage change that does not necessarily result in a common mode current. The common mode current is produced when the common mode voltage charges and discharges the parasitic capacitor of load midpoint relative to ground.

III. COMPENSATION CIRCUIT ELIMINATING COMMON MODE INTERFERENCE OF THREE PHASE INVERTER

In order to eliminate the influence of the common mode voltage, a hybrid compensation loop is added to the three-phase inverter as shown in Fig.2. The compensation circuit makes (4) invalid, and the sum of three-phase currents flowing through the inductor isn't zero, as shown in (7).

$$i_a + i_b + i_c = i_{ac} + i_{bc} + i_{cc} + i_{aN} + i_{bN} + i_{cN} \neq 0 \tag{7}$$

According to Kirchhoff's current law, it can be seen that the sum of the currents flowing through the three-phase load is always zero, while that flowing through the three-phase capacitor is not zero, as shown in

$$i_{ac} + i_{bc} + i_{cc} = i_f \tag{8}$$

Where, i_{f} is the current flowing through the compensation circuit. Substituting Eqn.(8) into Eqn.(1) and Eqn.(2), Eqn.(9) is derived:

$$\begin{aligned} u_{AO} + u_{BO} + u_{CO} &= u_{aO} + u_{bO} + u_{cO} + L\frac{d(i_a + i_b + i_c)}{dt} \\ &= 3u_{NO} + L\frac{d(i_a + i_b + i_c)}{dt} \\ &= 3u_{NO} + L\frac{d(i_{ac} + i_{bc} + i_{cc})}{dt} \\ &= 3u_{NO} + L\frac{di_f}{dt} \end{aligned} \tag{9}$$

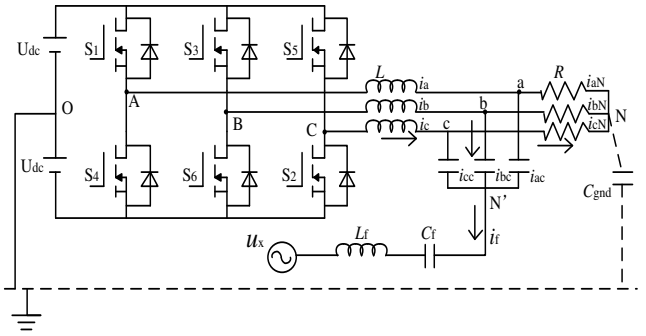


FIGURE 2. Three-phase voltage source inverters with compensation voltage source

The common mode voltage u_{cm} can be rewritten as:

$$\begin{aligned} u_{cm} &= \frac{1}{3}(u_{aO} + u_{bO} + u_{cO}) = u_{NO} \\ &= \frac{1}{3}(u_{AO} + u_{BO} + u_{CO} - L\frac{di_f}{dt}) \end{aligned} \tag{10}$$

The CMI compensation circuit consists of a controlled voltage source and a filter circuit. Formula (11) is shown the relationship between the instantaneous voltage value of the controlled voltage source and the current i_{f} flowing through the $L_{\mathrm{f}}C_{\mathrm{f}}$ filter:

$$\begin{cases} C\dfrac{\mathrm{d}u_{aO}}{\mathrm{d}t} - C\dfrac{\mathrm{d}u_{N'O}}{\mathrm{d}t} = i_{ac} \\ C\dfrac{\mathrm{d}u_{bO}}{\mathrm{d}t} - C\dfrac{\mathrm{d}u_{N'O}}{\mathrm{d}t} = i_{bc} \\ C\dfrac{\mathrm{d}u_{cO}}{\mathrm{d}t} - C\dfrac{\mathrm{d}u_{N'O}}{\mathrm{d}t} = i_{cc} \\ L_f\dfrac{\mathrm{d}i_f}{\mathrm{d}t} + \dfrac{1}{C_f}\int i_f \mathrm{d}t = u_{N'O} - u_x \end{cases} \tag{11}$$

Where , L_{f} and C_{f} are the inductance and the capacitance of the $L_{\mathrm{f}}C_{\mathrm{f}}$ filter in the common mode interference suppression circuit, respectively.

From Eqns.(1), (9), (10)and (11), Eqn.(12) can be obtained as follows:

$$\begin{aligned} u_x &= \frac{1}{3}(u_{AO} + u_{BO} + u_{CO}) + (-L_f - \frac{L}{3})\frac{di_f}{dt} \\ &+ (-\frac{1}{C_f} - \frac{1}{3C})\int i_f dt \end{aligned} \tag{12}$$

To suppress the common mode voltage and make it eventually to be zero, that is $u_{cm} = \frac{1}{3}(u_{AO} + u_{BO} + u_{CO} - L\frac{di_f}{dt}) = 0$ The relationship between the instantaneous voltage u_x of the controlled

voltage source and the midpoint voltage u_{AO}, u_{BO}, u_{CO} of each bridge arm of the three-phase inverter can be further derived from Eqn.(12).

$$\begin{aligned} u_x &= \frac{L}{3}\frac{di_f}{dt} + (-L_f - \frac{L}{3})\frac{di_f}{dt} + (-\frac{1}{C_f} - \frac{1}{3C})\int i_f dt \\ &= -L_f \frac{di_f}{dt} + (-\frac{1}{C_f} - \frac{1}{3C})\int i_f dt \\ &= -\frac{L_f}{L}(u_{AO} + u_{BO} + u_{CO}) \\ &+ (-\frac{1}{C_f} - \frac{1}{3C})\frac{1}{L}\int(\int(u_{AO} + u_{BO} + u_{CO})dt)dt \end{aligned} \tag{13}$$

If the controlled voltage source u_x is designed based on the midpoint instantaneous voltage of each bridge arm, the common mode voltage at the output side of the three-phase inverter should be zero. The midpoint voltage of each bridge arm is directly related to the control strategy in the three-phase inverter.

IV. PARAMETER CONFIGURATION AND DERIVATIVE METHOD

As can be seen from (13), a compensation loop is added to introduce a backward current to the output side of the three-phase inverter. This method increases the current loop of the electromagnetic interference source and completely eliminates common mode noise in the three-phase inverter. After adding a controlled loop, the common-mode voltage on the output side of the three-phase inverter is zero, which doesn't generate the common-mode current through the parasitic capacitance to the ground, and the high-frequency components are eliminated in the original common-mode voltage. The value of the controlled voltage source directly depends on the instantaneous value of the bridge arm voltage u_{AO}, u_{BO}, u_{CO}, which is independent of the control algorithm of the three-phase inverter. An active CM method is incorporated to regulate the low-frequency CM voltages on the AC buses with respect to the ground, the leakage current to the ground is suppressed.

A. About L_f

In theory, PWM waveform of the bridge arm voltage u_{AO}, u_{BO}, u_{CO} contains only AC component, no DC component. After the second term on the right side of (13) is integrated twice, the gain coefficient $1/\omega^2$ will emerge, which makes the second term small enough to be ignored. When only considering the influence of the first term of Eqn.(13) on the controlled voltage source, it can be divided into the following three situations:

(1) When L_f is equal to 0, the power supply u_x is approximately zero, degrading to the passive filter arrangement. The capacitor C_f can be directly connected to ground or connected to the midpoint O of the DC power supply side. These two methods are commonly used in common mode passive filter. The theoretical basis is provided here.

The resultant impedance of the capacitors C_f should effectively shunt the CM path on the load side. The large inductance of the CM choke L_f causes a voltage drop almost equal to the CM voltage, which allows compensation of this voltage at the output of the filter in Fig.3. The simple connection of the CM compensation part does not affect, additionally, sinusoidal shapes of line-to-line voltages.

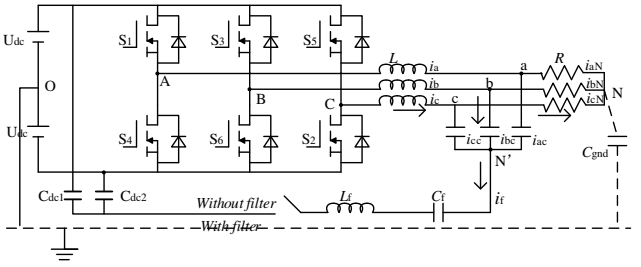


FIGURE 3. Compensator arrangement with three phase input CM choke

(2) When L_f is in the range of 0~L, the maximum value of the compensation power can be reduced without changing the control strategy. For example, when L_f=1/3L, the peak-to-peak value of the compensation power supply is U_{dc}; when L_f=1/6L, the peak-to-peak value of the compensation power supply is 1/2U_{dc}. Proportionally reducing the value of L_f can make the peak-to-peak value of the compensation power supply significantly smaller than the value of the DC voltage U_{dc}, which is beneficial to the selection of the controlled voltage source.

(3) Considering the symmetry of the filtering structure, L_f = L is selected. However, when the instantaneous voltage value at the midpoint of the three bridge arms is high, the instantaneous value and on-off frequency of the controlled voltage source are greatly restricted. Therefore, in practice, the bridge arm composed of active devices can be used to replace the controlled voltage sources, but control strategies and effective voltage space vectors must also be screened.

B. About C_f

In Fig.2 the connection structure between C and C_f reduces the required capacitance C_f in three-phase power conversion by allowing a large voltage ripple on the intermediate AC link. The adaptive ac-link control voltage is adopted to achieve high efficiency.

The CM path with the key parasitic impedance with respect to the ground will be considered. For the generated CM current to be derived from the ground to the compensation loop, the impedance of compensation loop, especially at high frequency, must be much lower than that of the ground path. The condition required to effectively divert the CM current from the ground path to the compensation loop may be summarized as follow:

$$Z_f \ll Z_{gnd} \tag{14}$$

Where, Z_f and Z_{gnd} are the impedance of the compensation loop and ground paths, respectively. Considering the parasitic elements shown in Fig.2, these impedance be defined as follows: $Z_{gnd} = 1/(j\omega C_{gnd})$; calculate the characteristic impedance of the compensation loop: $Z_f = 1/j\omega C_f$. This work focuses on maximizing C_f in a general theoretical analysis of CM impedance.

V. ACTIVE DEVICES COMPENSATION CIRCUIT

The third case in part IV is further discussed. The neutral point of the filter capacitor is connected to the output side of the fourth bridge arm. The inductor connected to the fourth bridge arm is consistent with the former three-phase filter inductor, which is used to reduce the influence of the high-frequency component of the current flowing through the fourth bridge arm on the three-phase load.

In the 3D-SVPWM modulation mode, the zero vectors u_0 and u_7 are $\pm U_{dc}$ at the 0-axis components，respectively . In the same way as 2D-SVPWM modulation mode, non-zero vectors are used to construct zero vectors to reduce the common-mode voltage. The non-zero voltage vector selected by the synthesis of the zero vectors in each sector is consistent with the selection principle of the 2D-SVPWM modulation mode.

The equivalent voltage state in the dead zone interval is introduced into the compensation control algorithm of the fourth phase bridge arm, and the original disordered dead zone state is encoded. Although it doesn't eliminate the influence of dead time setting on the output voltage harmonics in the original topology, it can accurately grasp the output voltage state of each phase in each control cycle, and propose the precise compensation mode of the fourth bridge arm, which is more effective and flexible to suppress common-mode interference.

The capacitance C_f should be increased as much as possible, so as to ignore the influence of the high frequency change rate of the midpoint voltage of the fourth bridge arm on the capacitance. Let $C_f=\delta C$. However, when the capacitance C_f is increased, the resonance point of the fourth bridge arm will be changed and reduced to $1/\sqrt{\delta}$ of the original resonance frequency, which will affect the filtering effect. According to theoretical analysis and experimental measurement, the value of δ is selected from 1.5 to 3. Combined with the actual capacitance of the capacitor C, $\delta = 2$ is selected in this paper.

VI. EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of introducing compensation current to the three-phase inverter proposed in this paper, which can effectively suppress the common mode voltage at the output side, the experiment circuit was built as shown in Fig.4 The parameters of experimental components are shown in Table 1. Each bridge arm is composed of a power device MOSFET IRFP450, and each power device is equipped with an anti-parallel diode MUR3080.The microprocessor TMS320F28335 provides the trigger signal for the first three bridge arms, and the trigger signal for the fourth bridge arm is provided by the XOR gate chip SN74ACT86. The power device selected by the fourth bridge arm is completely consistent with that of the front three-phase bridge arm. The fourth bridge arm is added to eliminate the common-mode voltage and should not affect the load voltage waveform.

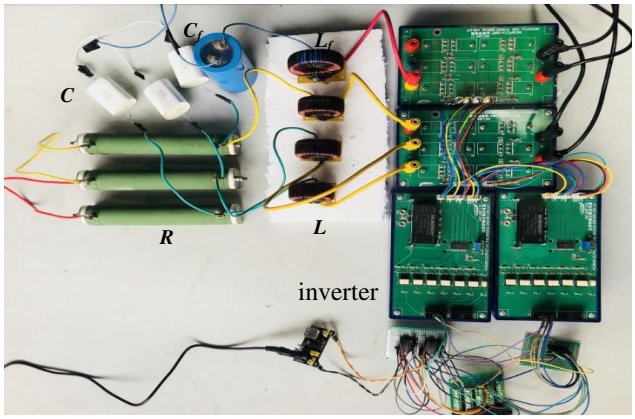
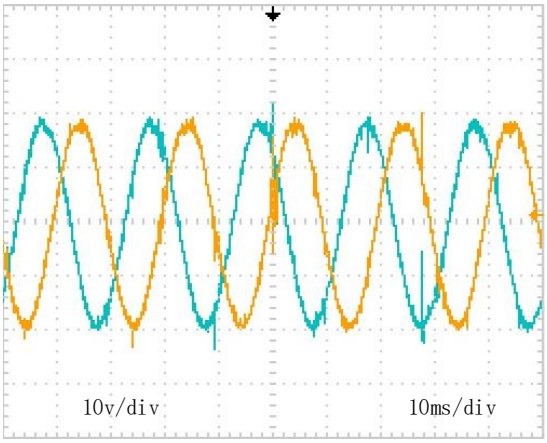


FIGURE 4. The experimental setup

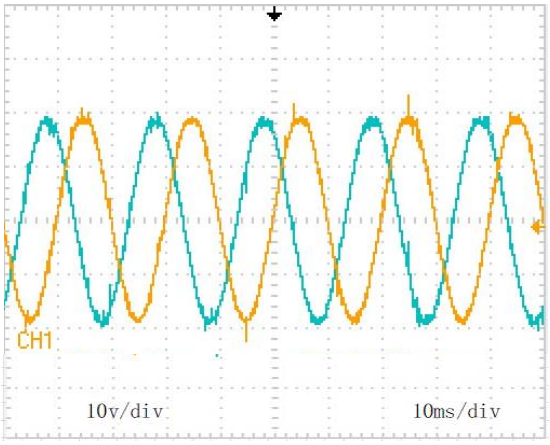
TABLE I
THE PARAMETERS OF EXPERIMENTAL COMPONENTS

Symbol	Parameter	Value
U_{dc}	DC voltage	50V
L_f	Output filter inductor	1mH
C	Output filter capacitor	10μF
C_f	Fourth bridge arm filter capacitor	20μF
R	load	180Ω

The method of eliminating the common-mode voltage should not affect the load voltage waveform. The output A and B phase load voltage waveform of the three-phase inverter with and without the compensation current circuit are shown in Fig.5(a) and (b), respectively. The amplitude, harmonics and frequency of the load are not affected. Compared with Fig.5(a), the peak interference of the load waveform is reduced in Fig.5(b). The peak-to-peak voltage of the load is 45.6V, and the root mean square value is 13.3V in Fig.5(b).



(a)without the compensation current circuit

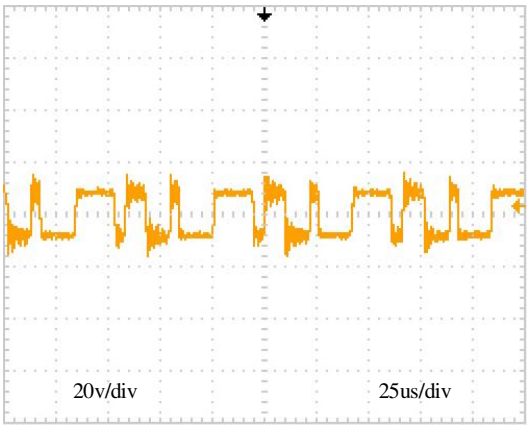


(b)with the compensation current circuit

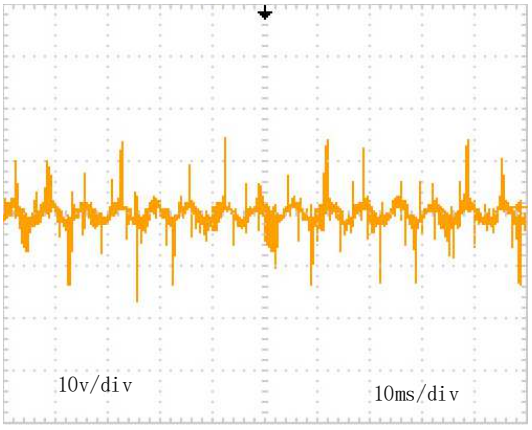
FIGURE 5. The output A and B phase load voltage waveform (V_{aN} and V_{bN})

The common-mode voltage waveform of the three-phase inverter without and with a compensation circuit is shown in Fig.6. Different from the previous experiments, this experiment shows the amplitude of the common-mode voltage, which is more conducive to verifying the effect of the proposed method on the instantaneous value of the common-mode voltage. The Fig.6(a) shows common-mode interference on the output side of the three-phase inverter with an amplitude of approximately 16.67V. Accompanied by high-frequency interference, it conforms to the common mode calculation formula (6). In Fig.6(b) with 2D-SVPWM non-zero vector modulation, the output-side common-mode voltage drops below 4V, and a few peak voltages are still around 14V. In Fig.6(c) with 3D-SVPWM zero-vector modulation, the peak voltage in the common mode interference is further reduced to below 6V. Compared with the 2D-SVPWM modulation mode, the peak value is reduced by 57%, mainly due to the fact that the common mode voltage compensation during the dead time is not considered in the 2D-SVPWM modulation mode. It can be seen that, regardless of any modulation mode, the common mode voltage is suppressed through the compensation loop.

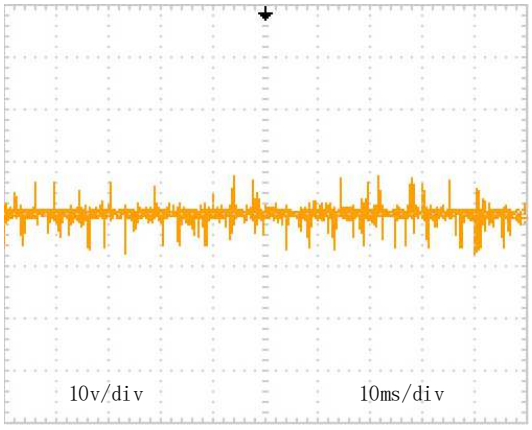
In addition, under the 10ms / div scale of the time axis, the low frequency component of the output common mode voltage in the 2D-SVPWM modulation mode is mainly the third harmonic, while that in the 3D-SVPWM modulation mode does not contain such component. According to the frequency range defined by common mode interference, this third harmonic may not be considered as common mode interference. In the two modulation modes, the spike interference occurs in the common mode voltage, which is related to the instantaneous interference caused by the power device in the converter at the moment of switching on and off. The instantaneous interference is conducted to the output side of the converter through lumped parameters such as parasitic inductance in the converter circuit. As the switching frequency of the power device increases, the influence of common mode interference on the output side will be strengthened. If the common mode interference on the output side of the inverter remains constant, the influence of the common mode voltage interference on the converter through the parasitic capacitor to the earth can be effectively suppressed.



（a） without a compensation circuit



（b）non-zero vector 2D-SVPWM with a compensation circuit



（c）non-zero vector 3D-SVPWM with a compensation circuit

FIGURE 6. the common-mode voltage waveform(V_{NO})

VII. CONCLUSION

In general, the overall efficiency and performance of the electric motor is considered dependent on the quality of the current to the motor, so the AC converter is considered a major source of both conducted and radiated electromagnetic interference (EMI). The CM current can flow in the loop, which is formed between the load and the inverter with the ground path. In general, CM interference suppression might use the external circuit, active or passive filter. Compared with previous similar studies, a backward loop at the front end of the load is introduced, so that load midpoint voltage relative to ground remains constant or zero. It can basically eliminate the common mode noise in the three-phase inverter from the perspective of the interference source. The hybrid compensation loop is proposed to control the drift of neutral point voltage, which is the low-frequency CM voltage, and effectively mitigate the ground leakage current. The high-frequency noise is filtered by passive components. The state of the controlled voltage source in the compensation loop is determined by the instantaneous voltage of each phase bridge arm, which is not affected by the modulation algorithm, so the common mode noise can be eliminated under different modulation modes. There is a trade-off between voltage source and the shunt inductor L_f. In addition, the compensation loop can also be derived other active or passive structures to enrich the suppression methods. The passive structures add the interference shunt path between the inverter input and output.

This loop can be extended to any circuit with three-phase load. The three-phase inverter is widely utilized for AC grid connection and motor speed control. The motor side, due to the high inverter switching frequencies (typically between 2kHz to 20kHz), high frequency harmonics up to 10 MHz (RFI) are generated by the inverter and conducted along the cable to the motor. The EMI radiations from this cable are therefore of relatively high frequency, due to high values of dv/dt. The voltage at the neutral point of the load is stable, reducing the high-frequency noise of the motor operating current. Considering the symmetry of the three phase output load currents, which may be required in the motor driven system, the number of magnetic volume and coil remains unchanged.

Data Availability statement

ll data generated or analysed during this study are included in this published article.

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