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Zhiyong Zhang (✉ zyzhang@pku.edu.cn)

Peking University <https://orcid.org/0000-0003-1622-3447>

Maguang Zhu

Peking University <https://orcid.org/0000-0001-7037-0136>

Peng Lu

Institute of Microelectronics, Chinese Academy of Sciences

Xuan Wang

National Space Science Center, Chinese Academy of Sciences

Chen Qian

National Space Science Center, Chinese Academy of Sciences

Huiping Zhu

Institute of Microelectronics, Chinese Academy of Sciences

Yajie Zhang

Peking university

Jianshuo Zhou

Peking University

Haitao Xu

Beijing Institute of Carbon-based Integrated Circuits

Zhengsheng Han

Institute of Microelectronics, Chinese Academy of Sciences

Jianwei Han

National Space Science Center, Chinese Academy of Sciences

Rui Chen

National Space Science Center, Chinese Academy of Sciences

Bo Li

Institute of Microelectronics, Chinese Academy of Sciences

Lian-Mao Peng

Peking University <https://orcid.org/0000-0003-0754-074X>

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Ultra-strong comprehensive radiation effect tolerance in carbon nanotube electronics

Maguang Zhu^{1, †}, Peng Lu^{2, †}, Xuan Wang^{3,4, †}, Chen Qian^{3,4}, Huiping Zhu², Yajie Zhang¹, Jianshuo Zhou¹, Haitao Xu⁵, Zhengsheng Han^{2,4}, Jianwei Han^{3,4}, Rui Chen^{3,4}, Bo Li^{2*}, Lian-Mao Peng^{1,5} and Zhiyong Zhang^{1,5*}*

¹ Key Laboratory for the Physics and Chemistry of Nanodevices and Center for Carbon-based Electronics, School of Electronics, Peking University, Beijing 100871, China.

² Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China.

³ National Space Science Center, Chinese Academy of Sciences, Beijing, China.

⁴ University of Chinese Academy of Sciences, Beijing, China.

⁵ Beijing Institute of Carbon-based Integrated Circuits, Beijing, China.

[†] These authors contributed equally to this work.

*Correspondence to: (R. C.) chenrui2010@nssc.ac.cn, (B. L.) libo3@ime.ac.cn, and (Z. Z.) zyzhang@pku.edu.cn.

ABSTRACT

Carbon nanotube (CNT) field-effect transistors (FETs) have been considered ideal building blocks for radiation-hardened integrated circuits (ICs), the demand for which is exponentially growing, especially in outer space exploration and the nuclear industry. Many studies on the radiation tolerance of CNT-based electronics have focused on the total ionizing dose (TID) effect, while few works have considered the single event effects (SEEs) and displacement damage (DD) effect, which are more difficult to measure but may be more important in practical applications. We first executed measurements of the SEEs and DD effect of CNT FETs and ICs and then presented a comprehensive radiation effect analysis of CNT electronics. The CNT ICs without special irradiation reinforcement technology exhibit a comprehensive radiation tolerance, including a 1×10^4

MeV·cm²/mg level of the laser-equivalent threshold linear energy transfer (LET) for SEEs, 2.8×10^{13} MeV/g for DD and 2 Mrad (Si) for TID, which are at least 4 times higher than those in conventional radiation-hardened ICs. The ultrahigh intrinsic comprehensive radiation tolerance will promote the applications of CNT ICs in high-energy solar and cosmic radiation environments.

Keywords: Carbon nanotube, radiation tolerance, single event effect, displacement damage, total ionizing dose

Benefitting from the ultrathin body, high carrier mobility and high saturation velocity, carbon nanotubes (CNTs) have been demonstrated to be an excellent channel to construct ultra-scaled field-effect transistors (FETs) with high performance and low power dissipation¹⁻⁴. Furthermore, CNT-based electronics can provide complementary metal-oxide-semiconductor (CMOS) transistors containing symmetric p- and n-type characteristics through a simple and well-compatible manufacturing process⁵ and have been considered promising candidates for integrated circuits (ICs), which act as the physical basis of modern information technology⁶ but are encountering development bottlenecks arising from the physics, power dissipation and manufacturing costs⁷. Subject to the immature technologies of wafer-scale material preparation, transistor fabrication and interconnection processes, the developing CNT electronics are thus far unable to meet the requirements of mainstream digital ICs, which contain tens of billions of transistors in one chip⁷. To promote the utility of CNT electronics as soon as possible, many researchers have explored some special purpose applications of CNT-based ICs that can take full advantage of CNT FETs while avoiding the integration density requirement. As the most popular special purpose ICs, ICs radiation-hardened to high-energy solar and cosmic radiation have received increasing attention with the increasing ambition of humankind to explore outer space, ranging from launching spacecrafts to establishing space stations and exploring distant celestial objects such as the Moon or Mars. CNT FETs and ICs have shown high radiation tolerance because of the strong C-C bonds, nanoscale cross-sections, low atomic number and negligible

substrate parasitic effect from CNT channels, and their first application in radiation-hardened electronics is highly expected^{8,9}. Furthermore, two additional advantages, *i.e.*, energy efficiency and low-temperature stability, enable CNT transistors to further meet the strict and harsh requirements for ICs used in deep space exploration¹⁰⁻¹³. Recently, great advances in radiation-hardened CNT ICs have been achieved, but these works mainly focused on the total ionizing dose (TID) effect^{8,9,14}, which is not sufficient to characterize the comprehensive radiation tolerance performance of an IC in the real space radiation environment. Compared to the TID effect, single event effects (SEEs)¹⁵ and the displacement damage (DD) effect¹⁶ are at least equally important in practical applications but are rarely studied in CNT-based transistors and ICs because they are more difficult to measure due to the challenges from the requirements on irradiation source as well as the complex circuits and electromagnetic environment. Moreover, the radiation tolerance to the TID effect increases with shrinkage of the pitch size of transistors¹⁷, which makes the radiation tolerance to SEEs become the bottleneck of the radiation performance of ICs¹⁸. To completely evaluate the radiation tolerance properties of CNT ICs, the comprehensive radiation effects, including TID, SEEs and DD, must be studied.

Here, we first executed measurements of SEEs and the DD effect of CNT FETs and ICs by using a pulse laser as the SEE irradiation source and high-energy Xe^+ ions as the DD irradiation source and then presented a comprehensive radiation effect analysis of CNT electronics. Device structure optimization strategies were then proposed to improve the comprehensive radiation tolerance of CNT ICs. The CNT ICs without special irradiation reinforcement technology exhibit a comprehensive radiation tolerance, including a $1 \times 10^4 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ level of the laser-equivalent threshold linear energy transfer (LET) for SEEs, $2.8 \times 10^{13} \text{ MeV/g}$ for DD and 2 Mrad (Si) for TID, which are at least 4 times higher than those in conventional radiation-hardened ICs ($100 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ for SEEs, 10^{11} MeV/g for DD and 500 krad (Si) for TID)¹². The ultrahigh intrinsic comprehensive radiation tolerance will promote the application of CNT ICs in high-energy solar and cosmic radiation environments, even in the development stage of

CNT electronics.

Physics of radiation-induced electronic failures in CNT FETs

High-energy photons (X-rays and γ -rays) and particles interact with the space environment and may deposit energy on the materials along their incident path. For CNT FETs, radiation-induced damage predominantly occurs in the CNT films, the surrounding oxide layers (gate oxide or substrate) and the gate/contact metals and may then result in temporary or permanent effects in ICs¹⁹. Radiation-induced damage is classified into three kinds of radiation effects, as shown in Fig. 1, *i.e.*, TID, DD and SEEs.

As shown in Fig. 1a, TID-induced degradation is long-term and permanent damage that starts with ionization of atoms and then results in electron-hole ($e-h$) pairs in the gate oxide of the CNT FET (Fig. 1b). The electrons easily escape from the gate oxide to the CNT channel, driven by the negatively biased gate (in p-FET), and the holes are then trapped in bulk defects (Fig. 1c). The trapped charges induced by TID radiation may cause degradation of the carrier mobility and on-state current, increased leakage current and a threshold voltage shift in CNT FETs.

DD is a permanent radiation effect induced by the collision of particles with the atoms of the materials in CNT FETs and may result in physical damage to the lattice of CNTs²⁰. As shown in Fig. 1d, the collision of particles with CNTs may displace the C atoms from their initial position and create vacancies and interstitial defects in the lattice. These defects and vacancies can create deep-level traps in the bandgap of CNTs and then cause an increase in the recombination rates and a reduction in the charge carrier lifetime (Fig. 1e). As a result, the DD effect may degrade the on-state current and subthreshold swing (SS) of CNT FETs.

SEEs in CNT FETs are temporary radiation effects caused by concentrated bursts of excess charges generated at random locations in the CNT channel and subsequently collected by the source/drain (Fig. 1f)²¹. As shown in the mechanism diagram in Fig. 1g, the SEE response starts with the creation of $e-h$ pairs along the track of the striking

particle in the CNT channel, gate oxide (HfO_2) and substrate (SiO_2), and is then caused by two combined effects: the radiation-sensitive volume current (Fig. 1h) and the gate electric field induced by SEEs (Fig. 1i). The SEE-induced transient pulse may introduce soft errors during the operation of CNT ICs (e.g., single event transients in CNT FETs and single event upsets in CNT static random-access memories (SRAMs)).

Generally, radiation-hardened ICs must be simultaneously tolerant to TID, DD and SEEs. With scaling down of the technology node in Si ICs, the radiation tolerance to the TID effect increases while the tolerance to SEEs degrades. For example, CMOS ICs at 22 nm or a more advanced node exhibit TID tolerance as high as approximately 1 Mrad (Si)²², and the radiation tolerance to SEEs then becomes the bottleneck of the radiation performance of ICs¹⁸. Although some low-dimensional semiconductors have been demonstrated to be excellent materials for building radiation-hardened FETs and ICs²³, almost all of these works focused on TID rather than SEEs owing to the great technology challenge in measuring SEEs.

SEE Measurements in CNT electronics

FETs and 6T SRAM cells are fabricated through a well-developed doping-free process on solution-derived randomly oriented CNT thin films with a semiconducting purity higher than 99.99% (see the details of the fabrication process in the Experimental Section). Two kinds of gate structures, including a local bottom gate and a top gate (Supplementary Fig. 1), are used in CNT FETs to satisfy the different irradiation sources used in this work. In particular, local bottom gate FETs and ICs are necessary to measure SEEs using pulse-laser testing technology.

Although SEEs in outer space (especially the single event transient and single event upset effects) are usually caused by heavy ion irradiation, directly testing the SEEs of ICs induced by heavy ions is a major challenge due to the complex electromagnetic environment in an accelerator. Pulse-laser testing has become a valuable method to study SEEs in transistors and ICs since recent developments in terms of a laser dosimeter approach and numerical methods suggest that a quantitative correlation

between the pulse laser and heavy charge deposition is possible²⁴. Therefore, we choose a pulse laser to test the SEEs in CNT FETs and ICs (see the experimental setup in Fig. 2a and the test details in the Experimental Section). Since the bandgap (typically 0.78 eV by scanning tunnelling microscopy (STM) measurement, as shown in Supplementary Fig. 2) of CNTs in the channel is smaller than the photon energy of the laser (1064 nm, ~ 1.2 eV), a single event charge can be generated in the CNT films through single photon absorption (SPA). Local bottom gate CNT FETs (see the structural diagram in Fig. 2b and transfer curve in Supplementary Fig. 3) are used as the device under test (DUT) to ensure that the laser completely reaches the surface of the CNT channel. It is worth mentioning that although the SEE measurements are carried out in local bottom gate CNT FETs, the results are still available to top gate FETs owing to the superior penetration of high-energy particles. As shown in Fig. 2c, the transient source-drain current (I_{ds}) curves are monitored by irradiating the single event-sensitive region with different laser energies (see the details to find the sensitive region in Supplementary Fig. 4). A peak current appears in the transient I_{ds} curves as the laser pulse energy increases to 5.2 nJ/pulse, which is quantified as the threshold laser energy for single event transients (SETs) in CNT FETs. Beyond the threshold laser energy, the pulse laser begins to excite SET behaviour, indicated by a peak current, which increases with the laser pulse energy. Note that the transient current peak in Fig. 2c exhibits a short tail of approximately 3 ns, which is much smaller than that in a Si FinFET (approximately 70 ns)²⁵. The short tail in the transient current mainly originates from the high carrier mobility of CNTs, which promotes diffusion of the charges induced by SETs, and indicates the low SET response of CNT FETs. We further explore how the channel length of CNT FETs affects the threshold laser energy for SETs, as shown in Fig. 2d. The threshold laser energy for SETs decreases with decreasing channel length, which is similar to that in Si FETs¹⁸. Although these results imply that the SET response of CNT FETs may increase as the channel length scales down, the threshold energy of 3.8 nJ/pulse in 0.18 μm channel length CNT FETs is still much higher than that in 0.18 μm Si MOSFETs (0.0985 nJ/pulse)²⁶.

As another SEE apart from SETs to be concerned with for electronic systems used in spacecraft, a single event upset (SEU) can also make electronic systems fail either by causing false logic functionality or scrambling storage values. Although SEU tolerance is very important for radiation-hardened ICs, there is still no study on the SEU effects in CNT ICs. To explore the radiation tolerance to SEUs of CNT ICs, we fabricate 6T SRAM cells consisting of p-type CNT FETs with a local bottom gate structure (see the schematic in Fig. 3a and equivalent circuit in Fig. 3b) and execute SEU measurements through a pulse-laser test. The transfer characteristics of CNT SRAMs can be seen in Supplementary Fig. 5. Before the SEU test, CNT SRAMs are biased to the write state, and the logic value “1” or “0” is written. Then, we monitor the transient voltage transfer curves ($V_{Q'}$ or V_Q) at node 2 or node 1 to record the SEU signals in an SRAM cell by irradiating a pulse laser on the most sensitive transistor (P1 or P2, respectively). When the laser pulse energy increases to the threshold laser energy for a SEU, a voltage peak appears in the transient $V_{Q'}$ curve, as shown in Fig. 3c and 3d. The measured threshold laser energy for SEUs in SRAM is 5.2 nJ/pulse, which is strictly consistent with the threshold laser energy for SETs measured in CNT FETs with a similar gate length. Different from the SET response of an individual FET, there are two transient voltage peaks induced by one effective pulse in the SEU measurement of SRAM, and the second transient voltage peak is higher than the first one. In an SRAM cell, the logic data are stored in the two back-to-back inverters consisting of transistors P1-P4, as shown in Fig. 3b. Once a SEE causes one of the nodes (node 1 or 2 in Fig. 3b) in the inverter to flip, the disturbance may propagate forward through the inverter with a gain higher than 1 and cause a transient with an increased amplitude on the other node. As evidence, the time difference between the two peaks is approximately 1 ns (0.95 ns in Fig. 3c and 1.06 ns in Fig. 3d), which is equal to the gate propagation time of the CNT network-based inverter with a similar (1 μm) gate length²⁷. As a result, a positive feedback effect appears and causes both nodes to flip to a wrong value²⁸, which means that an SEU occurs in the SRAM. However, the CNT SRAM must be recovered to the right state by the bitline retained in write mode during our measurements, and then, only two peaks, rather than a series

of peaks, are observed in the transient voltage transfer curves for one SEU, as shown in Fig. 3c and d. If transistor P2 is struck by an effective pulse laser, then the first SEU transient voltage peak in V_Q is negative, as shown in Fig. 3d, since the induced signal is out-of-phase amplified by the inverter consisting of P1 and P3.

Although the pulse laser has proven to be an available and powerful tool for studying SEEs²¹, the measured threshold laser energy must be converted to an equivalent LET, which is the standard parameter to benchmark SEEs in the real space environment. In dosimetry, LET is the average radiation energy deposited per unit path length along the track of an ionizing particle, which largely determines the consequence of SEE radiation²⁴. Here, we analyse the laser energy deposited on CNT devices and use the laser effective energy equivalent LET (ELET) model (referring to the Si-based devices)^{21,29} to estimate the ELET from the pulse-laser energy (the details are given in the Supplementary Information). According to the measured threshold laser energy values (5.2 nJ/pulse for the SRAM in Fig. 3c and 3.8 nJ/pulse for the CNT FET in Fig. 2d), the estimated ELET is approximately 1.49×10^4 MeV·cm²/mg in 1 μm CNT FETs and SRAMs and declines to 1.08×10^4 MeV·cm²/mg in 0.18 μm CNT FETs and ICs. Therefore, CNT FETs and ICs exhibit ELETs approximately 2 orders of magnitude higher than Si-based FETs and ICs³⁰, indicating that CNT electronics present great potential for radiation hardened properties with respect to SEEs.

Mechanisms of SEEs in CNT electronics

The mechanisms of SEEs in an FET can be explained as two correlated effects: (1) the radiation-sensitive volume and (2) the gate electric field induced by SEEs (Supplementary Fig. 6a)³¹. For Si-based devices (bulk Si, fully depleted silicon on insulator (FDSOI) or FinFET) with a large sensitive channel volume, the SEE response is mainly caused by the first mechanism. In CNT FETs with ultrathin channels and nanoscale cross sections, the SEE-sensitive channel volume is almost negligible. Therefore, the SEE response in CNT FETs mainly originates from the second mechanism, which is much more difficult to achieve than the first SEE mechanism in

conventional bulk semiconductor. As a result, CNT electronics exhibit much better SEE radiation hardened properties than Si-based electronics. TCAD simulations, which can decouple these two mechanisms^{31,32}, are used to prove this explanation.

Fig. 3e shows the transient characteristics of two kinds of transistors with no physical gate. In the transistors without a gate, the SET current is only caused by the radiation-sensitive channel volume (see the details of the charge density profile at $LET=10^4$ MeV·cm²/mg with a normal incidence angle to the channel for the 180 nm node FDSOI FET and CNT FET in Supplementary Fig. 6b and Fig. 6c, respectively). Notably, compared with the FDSOI FET, the CNT FET with a similar node shows almost no SEE-sensitive channel volume current at $LET=10^4$ MeV·cm²/mg. When scaled down to the 5 nm node, the SEE-sensitive channel volume current of the CNT FET is still much lower than that of a nanosheet FET (NSFET), which has the smallest SEE-sensitive volume in Si-based transistors in theory (shown in Supplementary Fig. 6d-f). Therefore, we can conclude that the SEE response in the CNT FET is mainly caused by the gate electric field, which means that the SEE radiation hardening level can be further improved by increasing the gate efficiency. According to the experimental results shown in Fig. 3f, the threshold laser energy for SETs increases from 3.76 nJ/pulse to 8.19 nJ/pulse as the gate oxide thickness (t_{ox}) decreases from 12 nm to 6 nm. Not only can these experimental results further prove the SEE response mechanism of the CNT FET, but also, they indicate that we can significantly strengthen SEE radiation hardened properties in CNT electronics by scaling the thickness of the gate oxide, by which we can simultaneously strengthen the rad-hard level for TID³³ and DD (we will discuss this in the next section).

DD effect measurements and mechanisms in CNT transistors

To systematically emulate device degradation in the space environment, analysing the DD induced by high-energy particle incidents on CNT FETs is also critical¹⁶. As the fact that the gate metal cannot resist heavy ions is well known³⁴, 2225 MeV Xe⁺ ion irradiation tests are performed on top-gate CNT FETs (Fig. 4a) to investigate the DD effect (see the details of the DD experimental method in the Experimental Section and

Supplementary Fig. 7). The CNT films as the channel region are first characterized by Raman tests before and after heavy ion irradiation. According to the Raman spectra of CNT films irradiated by various heavy ion fluences (Supplementary Fig. 8), Xe^+ radiation has a relatively small impact on the I_D/I_G up to fluences (ions) of $5 \times 10^{12} \text{ cm}^{-2}$ (Fig. 4b), implying that few displacement defects are generated in the CNT films.

Although the CNT film shows a strong tolerance against heavy ion irradiation, Xe^+ radiation still causes crucial performance degradations in CNT FETs (Fig. 4c). Both the I_{ON}/I_{OFF} and SS degrade with increasing Xe^+ fluence, with a significant nonlinear correlation (Fig. 4d). The $1 \times 10^{12} \text{ cm}^{-2}$ Xe^+ radiation leads to little degradation of I_{ON}/I_{OFF} and SS, indicating that the CNT FETs remain intact. However, the $5 \times 10^{12} \text{ cm}^{-2}$ Xe^+ radiation causes significant degradation of the I_{ON}/I_{OFF} ratio (lowers it by over 1000 times) and SS (increases it by 330 mV/dec), which indicates electronic failure in CNT FETs owing to a significant trap generation process in the dielectrics³⁵. The statistical test results of 20 CNT FETs (Supplementary Fig. 9) further confirm that $1 \times 10^{12} \text{ cm}^{-2}$ Xe^+ radiation induces negligible degradation, while $5 \times 10^{12} \text{ cm}^{-2}$ Xe^+ radiation causes electronic failure. Interestingly, Xe^+ ion irradiation has little impact on the gate leakage current (Supplementary Fig. 9d), indicating that the DD effect does not form a leakage path in the HfO_2 gate dielectric. As a widely used key parameter, the DD dose (D_d) is employed here to benchmark the CNT FET DD tolerance³⁴. The 10^{12} cm^{-2} Xe^+ ion irradiation can induce a D_d of $2.79 \times 10^{13} \text{ MeV/g}$, which is significantly ($>10^2 \times$) higher than the radiation tolerance requirement for outer space exploration missions¹³.

We further reveal the mechanism of the DD effect in CNT FETs through Monte Carlo simulations (see the details of the SRIM simulation in the Experimental Section). Simulation results (Fig. 4e and Supplementary Fig. 10a) reflect that the damage to a transistor is approximately uniformly distributed in the CNT film and substrate, which indicates that neither the HfO_2 gate dielectric nor the Pd gate metal has a shielding effect on the heavy ions. Meanwhile, few vacancies form in the CNT film (Fig. 4f and Supplementary Fig. 10b), confirming the robustness of CNTs to DD radiation,

consistent with the Raman test results (Fig. 4b and Supplementary Fig. 8). Although a high concentration of vacancies appears in the gate metal, they may be shielded by the high-density electrons in the metal and do not affect the electrical properties of the CNT channel. Therefore, the gate oxide is identified as the most vulnerable component in CNT FETs, and its damage will provide a major contribution to device failure. Then, scaling t_{ox} can effectively reduce the radiation-sensitive volume and improve the DD tolerance. We also simulate the DD hardening effect of CNT FETs through TCAD simulation tools (see the details of the TCAD setup and calibration in the Experiment Section)³⁶, and the simulated transfer curves (Fig 4g) present good agreement (error <10%) with the experimental data. As shown in Fig. 4h, t_{ox} scaling can also be utilized as an effective improvement method for DD hardening.

Comprehensive radiation effects in CNT electronics

Although in this work we have respectively shown that CNT FET and CNT based ICs have excellent radiation harden properties to SEEs and DD, there are multiple radiation effects combined (DD, TID and SEE) in the real space environment at the same time which may cause more severe comprehensive radiation damage to electronic systems. Here for the first time, we fabricate radiation-hardened CNT FETs and CNT SRAMs by thinning the gate oxide thickness to 8 nm and then investigate the comprehensive radiation effects, including SEEs, DD and TID. As shown in Fig. 5a, the CNT FETs and SRAMs are exposed to Xe^+ DD radiation, γ -ray TID radiation (Supplementary Fig. 11) and a 1064 nm pulsed laser for SEEs in turn. Since defects induced by DD and trapped charges induced by TID will remain in FETs and then influence the following SEE response measurement¹¹, this experimental method can be used to emulate radiation effects on CNT-based ICs in the real space environment.

The transfer characteristics of CNT FETs and SRAMs with different Xe^+ fluences and TIDs are shown in Supplementary Fig. 12a-d. Fig. 5b and Supplementary Fig. 12e present the SEEs of CNT FETs and SRAMs after being exposed to $1 \times 10^{12} \text{ cm}^{-2} Xe^+$ DD and 2 Mrad (Si) TID radiation. The threshold pulse laser energies for the SET response in CNT FETs and the SEU response in CNT SRAMs do not change with the

DD and TID radiation. Although the full width at half maximum of SETs in CNT FETs slightly increases after exposure to DD and TID, the SET peak current can still be restored to 0 for approximately 500 ps. This is because the defects caused by DD and the trap charge introduced by TID can reduce the g_m of CNT FETs, which may reduce the SEE diffusion current. These results demonstrate that the CNT ICs used in this work can withstand DD up to 2.79×10^{13} MeV/g, TID up to 2 Mrad (Si) and SEEs up to 1.78×10^4 MeV cm²/mg simultaneously.

We benchmark the radiation tolerance of CNT ICs in this work with that of other radiation-hardened FETs³⁷, such as reported CNT FETs^{8,38,39}, 2-D materials⁴⁰⁻⁴², metal oxide thin films⁴³ and Si FinFETs^{26,44,45}, based on important metrics involving TID, DD influences and the SET threshold energy, as shown in Fig. 5c. Compared with previously reported FETs, the CNT FETs in this work can withstand a higher threshold laser energy for SEEs and a higher heavy ion energy for DD. Although some reported works show higher radiation tolerance than this work (e.g., 15 Mrad TID for the ion gel CNT FET or 1×10^{14} cm⁻² He⁺ for the MoS₂ FET), they only tested a single radiation effect. In addition, considering that the radiation hardened properties of devices depend on the channel length to some extent, we compare the comprehensive radiation hardened properties of 0.18 μm CNT FETs with those of 0.18 μm Si FETs, as shown in Fig. 5d. Note that Si-based FETs require different radiation hardening methods for different irradiation effects, so we choose different reported works to compare the radiation tolerance^{12,26,30,46}. Compared with radiation-hardened Si FETs, CNT FETs with similar gate lengths lead by more than one magnitude in DD dose, TID and LET for SEEs, indicating the huge advantage for radiation-hardened or harsh environment electronics.

Conclusions

In this work, we systematically demonstrate that CNT electronics are a promising radiation hardened technology for outer space exploration. We thoroughly test and analyse the SEE, DD and TID tolerance of CNT FETs and ICs and estimate their comprehensive radiation effect tolerance. By using a pulse laser as the SEE irradiation

source, 2225 MeV Xe⁺ as the DD irradiation source and Co-60 γ -ray as the TID irradiation source to simulate the radiation environment in space, rad-hard CNT ICs are tested and exhibit a radiation tolerance level of up to 2 Mrad (Si) for TID, 2.8×10^{13} MeV/g for DD and threshold LET= 10^4 MeV·cm²/mg for SEEs, which are far beyond the radiation tolerance requirements for outer space exploration (500 krad (Si) for TID, 10^{11} MeV/g for DD and 100 MeV·cm²/mg for SEEs). Moreover, these levels of radiation tolerance for different radiation effects can be realized on CNT FETs at the same time without special irradiation reinforcement technology. This work showcases CNT-based ICs as a promising radiation-hardened technology for application in space exploration and nuclear industry.

Experimental Section

Preparation of CNT thin films:

Uniform initially semiconducting single-walled CNT (s-SWCNT) films were prepared by deposition. Arc-discharged CNTs were purchased from Carbon Solutions Inc. Dispersants (poly[9-(1-octylonoyl)-9H-carbazole-2,7-diyl (PCz)]) were synthesized by Suzuki polycondensation. A total of 100 mg AP-SWCNTs and 100 mg PCz were added to 100 mL toluene. Then, the solution was dispersed with a top-tip dispergator (Sonics VC700) at 300 W for 30 min. The dispersed solution was centrifuged for 0.5 h at 50000 g to remove most metallic CNTs and insoluble materials. The upper 90% of the supernatant was collected and centrifuged for a second time for 2 h at 50000 g. Finally, we collected the upper 90% of the supernatant for fabrication of a thin film with the dip-coating method. The sorted CNT solution was diluted ten times with toluene. The Si/SiO₂ substrate was immersed in the diluted solution for 72 h. The substrate was then removed from the solution, rinsed with toluene for 30 min, purged with 99.999% N₂ and baked at 120°C for 30 min in air. Finally, to reduce the influence of the polymer on the radiation hardened properties of CNTs, the film was

annealed in a tube furnace with a forming gas (Ar/H₂: 5/1) at a temperature of 600°C for 3 h to remove the polymer.

Fabrication Processes:

Local bottom gate CNT FET:

The local bottom gate window was patterned by electron beam lithography (EBL), followed by evaporation of 20 nm Pd and growth of 10 nm HfO₂ through atomic layer deposition (ALD) with a standard lift-off process. Next, CNTs were solution-deposited and oxygen plasma etched for 60 s to define the channels of the CNT FETs. The active channel region was defined by EBL, followed by oxygen plasma etching for 60 s. The top gate window was patterned through EBL, followed by growth of 10 nm HfO₂ through ALD and evaporation of 20 nm Pd with a standard lift-off process. Finally, the source and drain electrodes were patterned by EBL, followed by evaporation of 0.3 nm Ti and 70 nm Pd to fabricate a p-type contact.

Top-gate CNT FET:

Source and drain electrodes were patterned by EBL, followed by evaporation of 0.3 nm Ti and 70 nm Pd to fabricate a p-type contact. Next, the active channel region was defined by EBL, followed by oxygen plasma etching for 60 s. The top gate window was patterned through EBL, followed by growth of 10 nm HfO₂ through ALD and evaporation of 20 nm Pd with a standard lift-off process. Finally, the upper interconnect was patterned by EBL, with deposition of 20/90 nm Ti/Au metal by electron beam evaporation (EBE) and a standard lift-off process.

CNT-based 6T SRAM:

The local bottom gate window was patterned by EBL, followed by evaporation of 20 nm Pd and growth of 10 nm HfO₂ through ALD with a standard lift-off process. Next, CNTs were solution-deposited and oxygen plasma etched for 60 s to define the channels of the CNT-based 6T SRAM. An interlayer dielectric was formed using poly(methyl methacrylate) (PMMA) 200 K via EBL with a dose of 10000 $\mu\text{C}/\text{cm}^2$. Finally, the upper interconnect was patterned by EBL with 20/90 nm Ti/Au metal deposited by EBE and a standard lift-off process. The CNT-based 6T SRAMs in this

work were measured using a probe station with a semiconductor analyser (Keithley 4200) in air.

Radiation exposure:

SEE pulse-laser irradiation:

An oscilloscope with a 50 Ω input impedance was used to visualize and record the SETs. The laser beam was focused using a 100x microscope objective to create a charge generation spot size of approximately 2 μm . Laser pulses with a wavelength of 1064 nm and a normal pulse width of 150 fs at a repetition rate of 1 kHz were used. During the SET pulsed-laser test, the CNT FETs and CNT-based SRAMs were fixed on the x - y - z stage with a 0.1 μm resolution.

Xe⁺ ion DD irradiation:

The Xe⁺ ion irradiation experiment was carried out at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences (IMP-CAS). The Xe⁺ ion energy was modulated by employing both aluminium foils and air as degraders, and the value in Si was calibrated to be 27.9 MeV·cm²/g. Tests with various ion fluences were performed at a normal angle of incidence (0°).

Co-60 γ -ray TID irradiation:

The radiation experiments were carried out by using a Co-60 source in vacuum. The radiation rate used for all samples was approximately 480 rad (Si)/s. The transistor curves were measured after each radiation exposure.

SRIM simulation setup:

The simulated Xe⁺ ion fluence in the SRIM simulation was set to $5 \times 10^{12} \text{ cm}^{-2}$, while its incident angle and energy were set according to the experimental conditions. The incident location was assumed to be uniformly distributed on the Pd surface (depth 0 Å). In the simulated 60 nm \times 60 nm cross-section, the Pd gate metal electrode, HfO₂ gate dielectric, CNT channel and SiO₂ substrate were included. A 2 nm-thick graphene-carbon-graphene sandwich layer, featuring a middle layer with reduced carbon atom

density, was used to emulate the structure of a CNT. The default material parameters of Pd, HfO₂ and SiO₂ were utilized for the corresponding materials.

Sentaurus TCAD setup and calibration

A schematic of the simulated device is shown in Fig. S1, and the geometric parameters were set according to the experimental data discussed in the previous section. The channel CNT network was emulated by a 2 nm-thick quasi-2D layer. Since this work focuses on p-type CNT FET analysis, hole transport was investigated in detail. To accurately calculate the CNT film carrier density, the following equations were set in the quasi-2D channel⁴⁷:

$$p = 2N_V \exp\left(-\frac{E_F - E_V}{kT}\right)$$

$$N_V \approx \frac{g_0}{4} \sqrt{\pi k T E_G}$$

$$E_G = 0.85 / d_{CNT}$$

where d_{CNT} is the diameter of the CNT and is set to 2 nm. A modified drift-diffusion (DD) model with high field velocity saturation was used for carrier transport:

$$\mu_p = \mu_{0p} \times \left[\frac{1}{1 + \left(\frac{\mu_{0p} \times \varepsilon}{v_{satp}} \right)^\beta} \right]^{\frac{1}{\beta}}$$

where ε is the lateral electric field, μ_{0p} is the low-field hole mobility, v_{satp} is the saturation velocity and β is an empirical parameter, set to 1.4. The low-field mobility empirically captures the scattering term induced by various components of the CNT FET:

$$\mu_{0p} = \left(\mu_{CNT}^{-1} + \mu_{DD}^{-1} \right)$$

where μ_{CNT} is extracted from the pristine device performance and μ_{DD} represents the

scattering caused by DD (extracted to be $1.1 \text{ cm}^2/\text{V-s}$ after $5 \times 10^{12} \text{ cm}^{-2}$ Xe⁺ ion irradiation). Meanwhile, both the interface states and fixed charges in the dielectrics were extracted through threshold voltage shift and subthreshold performance analysis. The Pd S/D metals were modelled as ohmic contacts. Since the off-state leakage is strongly affected by the surface contamination, which varies between samples and cannot be effectively calibrated, no leakage model was included in the simulations.

References

- 1 Shulaker, M. M. *et al.* Carbon nanotube computer. *Nature* **501**, 526-530 (2013).
- 2 Liu, L. *et al.* Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics. *Science* **368**, 850-856 (2020).
- 3 Zhong, D. *et al.* Gigahertz integrated circuits based on carbon nanotube films. *Nature Electronics* **1**, 40-45 (2018).
- 4 Qiu, C. *et al.* Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches. *Science* **361**, 387-392 (2018).
- 5 Yang, Y., Ding, L., Han, J., Zhang, Z. & Peng, L.-M. High-performance complementary transistors and medium-scale integrated circuits based on carbon nanotube thin films. *ACS nano* **11**, 4124-4132 (2017).
- 6 Hills, G. *et al.* Modern microprocessor built from complementary carbon nanotube transistors. *Nature* **572**, 595-602 (2019).
- 7 Bishop, M. D. *et al.* Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities. *Nature Electronics* **3**, 492-501 (2020).
- 8 Zhu, M. *et al.* Radiation-hardened and repairable integrated circuits based on carbon nanotube transistors with ion gel gates. *Nature Electronics* **3**, 622-629, doi:10.1038/s41928-020-0465-1 (2020).
- 9 Zhu, M., Zhou, J., Sun, P., Peng, L.-M. & Zhang, Z. Analyzing Gamma-Ray Irradiation Effects on Carbon Nanotube Top-Gated Field-Effect Transistors. *ACS Applied Materials & Interfaces* **13**, 47756-47763 (2021).
- 10 Council, N. R. *NASA space technology roadmaps and priorities: restoring NASA's technological edge and paving the way for a new era in space.* (National Academies Press, 2012).
- 11 Barnaby, H. Total-ionizing-dose effects in modern CMOS technologies. *IEEE Transactions on Nuclear Science* **53**, 3103-3121 (2006).
- 12 Hafer, C., Mabra, J., Slocum, D. & Kalkur, T. in *2006 IEEE Aerospace Conference.* 8 pp. (IEEE).
- 13 Meyyappan, M., Koehne, J. E. & Han, J.-W. Nanoelectronics and nanosensors for space exploration. *MRS Bulletin* **40**, 822-828 (2015).
- 14 Kanhaiya, P. S. *et al.* Carbon Nanotubes for Radiation-Tolerant Electronics. *ACS nano* **15**, 17310-17318 (2021).
- 15 Sexton, F. W. Destructive single-event effects in semiconductor devices and ICs. *IEEE Transactions on Nuclear Science* **50**, 603-621 (2003).
- 16 Srour, J., Marshall, C. J. & Marshall, P. W. Review of displacement damage effects in silicon devices. *IEEE transactions on nuclear science* **50**, 653-670 (2003).
- 17 Fleetwood, D. M. Evolution of total ionizing dose effects in MOS devices with Moore's law scaling. *IEEE Transactions on Nuclear Science* **65**, 1465-1481 (2017).
- 18 Benedetto, J., Eaton, P., Mavis, D., Gadlage, M. & Turflinger, T. Digital single event transient trends with technology node scaling. *IEEE Transactions on Nuclear Science* **53**, 3462-3465 (2006).
- 19 Prinzie, J., Simanjuntak, F. M., Leroux, P. & Prodromakis, T. Low-power electronic technologies for harsh radiation environments. *Nature Electronics* **4**, 243-253,

- doi:10.1038/s41928-021-00562-4 (2021).
- 20 Smith, B. W. & Luzzi, D. E. in *AIP Conference Proceedings*. 360-363 (American Institute of Physics).
- 21 Buchner, S. P., Miller, F., Pouget, V. & McMorrow, D. P. Pulsed-laser testing for single-event effects investigations. *IEEE Transactions on Nuclear Science* **60**, 1852-1875 (2013).
- 22 Brewer, R. M. *et al.* Total ionizing dose responses of 22-nm FDSOI and 14-nm bulk FinFET charge-trap transistors. *IEEE Transactions on Nuclear Science* **68**, 677-686 (2021).
- 23 Vogl, T. *et al.* Radiation tolerance of two-dimensional material-based devices for space applications. *Nature communications* **10**, 1-10 (2019).
- 24 Pouget, V., Lapuyade, H., Fouillat, P., Lewis, D. & Buchner, S. Theoretical investigation of an equivalent laser LET. *Microelectronics Reliability* **41**, 1513-1518 (2001).
- 25 El-Mamouni, F. *et al.* Laser-and heavy ion-induced charge collection in bulk FinFETs. *IEEE Transactions on Nuclear Science* **58**, 2563-2569 (2011).
- 26 Jin-Shun, B. *et al.* Estimation of pulsed laser-induced single event transient in a partially depleted silicon-on-insulator 0.18- μm MOSFET. *Chinese Physics B* **23**, 088505 (2014).
- 27 Xie, Y., Zhang, Z., Zhong, D. & Peng, L. Speeding up carbon nanotube integrated circuits through three-dimensional architecture. *Nano Research* **12**, 1810-1816 (2019).
- 28 Karnik, T. & Hazucha, P. Characterization of soft errors caused by single event upsets in CMOS processes. *IEEE Transactions on Dependable and secure Computing* **1**, 128-143 (2004).
- 29 Hales, J. M. *et al.* Experimental validation of an equivalent LET approach for correlating heavy-ion and laser-induced charge deposition. *IEEE Transactions on Nuclear Science* **65**, 1724-1733 (2018).
- 30 Aditya, K., Jha, C. K., Basra, S., Jatana, H. & Dixit, A. Transient Response of 0.18- μm SOI MOSFETs and SRAM Bit-Cells to Heavy-Ion Irradiation for Variable SOI Film Thickness. *IEEE Transactions on Electron Devices* **65**, 4826-4833 (2018).
- 31 Kim, J., Lee, J.-S., Han, J.-W. & Meyyappan, M. Single-event transient in FinFETs and nanosheet FETs. *IEEE Electron Device Letters* **39**, 1840-1843 (2018).
- 32 Han, J.-W., Kim, J., Moon, D.-I., Lee, J.-S. & Meyyappan, M. Soft error in saddle fin based DRAM. *IEEE Electron Device Letters* **40**, 494-497 (2019).
- 33 Zhu, M., Zhou, J., Sun, P., Peng, L.-M. & Zhang, Z. Analyzing Gamma-Ray Irradiation Effects on Carbon Nanotube Top-Gated Field-Effect Transistors. *ACS Applied Materials & Interfaces* (2021).
- 34 Srour, J. a. & Palko, J. Displacement damage effects in irradiated semiconductor devices. *IEEE Transactions on Nuclear Science* **60**, 1740-1766 (2013).
- 35 Schwank, J. R. *et al.* Radiation Effects in MOS Oxides. *IEEE Transactions on Nuclear Science* **55**, 1833-1853, doi:10.1109/tns.2008.2001040 (2008).
- 36 Xu, L., Qiu, C., Peng, L.-m. & Zhang, Z. Suppression of leakage current in carbon nanotube field-effect transistors. *Nano Research* **14**, 976-981 (2021).
- 37 Gong, H. *et al.* Scaling effects on single-event transients in InGaAs FinFETs. *IEEE Transactions on Nuclear Science* **65**, 296-303 (2017).
- 38 Zhu, M. G., Zhang, Z. & Peng, L. M. High-Performance and Radiation-Hard Carbon Nanotube Complementary Static Random-Access Memory. *Advanced Electronic Materials* **5**, 1900313 (2019).
- 39 Luo, M. *et al.* Radiation-Hard and Repairable Complementary Metal–Oxide–Semiconductor

- Circuits Integrating n-type Indium Oxide and p-type Carbon Nanotube Field-Effect Transistors. *ACS Applied Materials & Interfaces* **12**, 49963-49970 (2020).
- 40 Arnold, A. J., Shi, T., Jovanovic, I. & Das, S. Extraordinary radiation hardness of atomically thin MoS₂. *ACS applied materials & interfaces* **11**, 8391-8399 (2019).
- 41 Liang, C. *et al.* Laser-Induced Single-Event Transients in Black Phosphorus MOSFETs. *IEEE Transactions on Nuclear Science* **66**, 384-388 (2018).
- 42 Liang, C. *et al.* Defects and low-frequency noise in irradiated black phosphorus MOSFETs with HfO₂ gate dielectrics. *IEEE Transactions on Nuclear Science* **65**, 1227-1238 (2018).
- 43 Park, B. *et al.* Solution-Processed Rad-Hard Amorphous Metal-Oxide Thin-Film Transistors. *Advanced Functional Materials* **28**, 1802717 (2018).
- 44 El Mamouni, F. *et al.* Fin-width dependence of ionizing radiation-induced subthreshold-swing degradation in 100-nm-gate-length FinFETs. *IEEE Transactions on Nuclear Science* **56**, 3250-3255 (2009).
- 45 Paillet, P. *et al.* Total ionizing dose effects on deca-nanometer fully depleted SOI devices. *IEEE transactions on nuclear science* **52**, 2345-2352 (2005).
- 46 Tan, F. *et al.* Effect of Heavy Ion Irradiation on the RF Performance of 0.18 μm Bulk Si MOSFETs. *ECS Transactions* **44**, 141 (2012).
- 47 Liang, J., Akinwande, D. & Wong, H.-S. P. Carrier density and quantum capacitance for semiconducting carbon nanotubes. *Journal of Applied Physics* **104**, 064515 (2008).

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Author contributions

Z. Z. proposed and supervised the project. M. Z. fabricated CNT FETs and SRAM cells for radiation tests. P. L. set up the numerical simulation and interpreted the governing mechanism of the radiation effects. M. Z., X. W. and C. Q. carried out the laser single event effect experiments. Y. Z. performed the STM tests of CNTs. M. Z., H. X. and J. Z. performed the total ionizing dose tests. M. Z., P. L. and H. Z. performed the displacement damage irradiation test. M. Z. performed the Raman spectroscopy characterization before and after irradiation. P. L. and H. Z. performed the SRIM Monte Carlo calculation. J. H. and R. C. supervised the radiation experiments. B. L. and Z. H. supervised the theoretical comparison between CNT FETs and Si-based transistors. M. Z., P. L., R. C., B. L. and Z. Z. analysed the data. M. Z., P. L. and Z. Z. cowrote the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing financial interest.

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Correspondence and requests for materials should be addressed to Z.Z.

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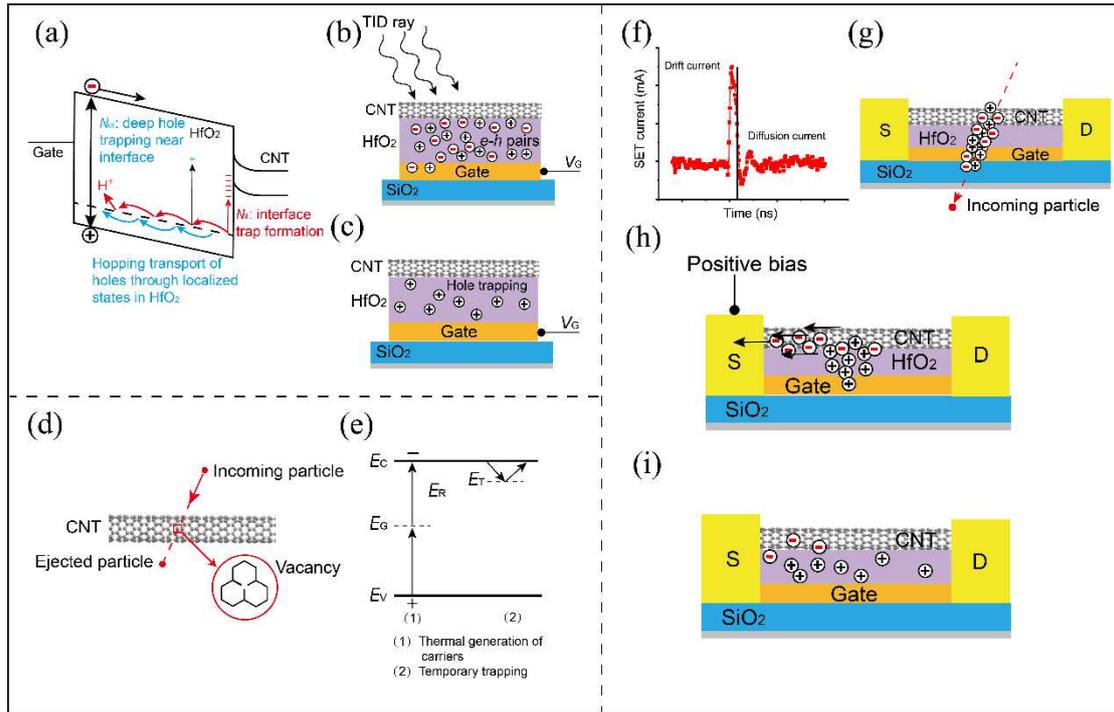


Fig. 1 | Radiation damage mechanisms (TID, DD and SEEs) in CNT FETs and ICs. a, Schematic of the TID degradation mechanism of a CNT FET. **b,** TID-induced e-h pairs generated in the oxide. **c,** TID-induced holes trapped at the interface. **d,** Schematic of the DD degradation mechanism of a CNT FET. **e,** DD in a CNT FET can affect carrier recombination, trapping and concentration. **f,** Typical single event transient current of a CNT FET. **g,** Schematic of the SEE degradation mechanism of a CNT FET. **h,** Schematic of the radiation-sensitive channel volume current induced by SEEs. **i,** Schematic of the gate electric field induced by SEEs.

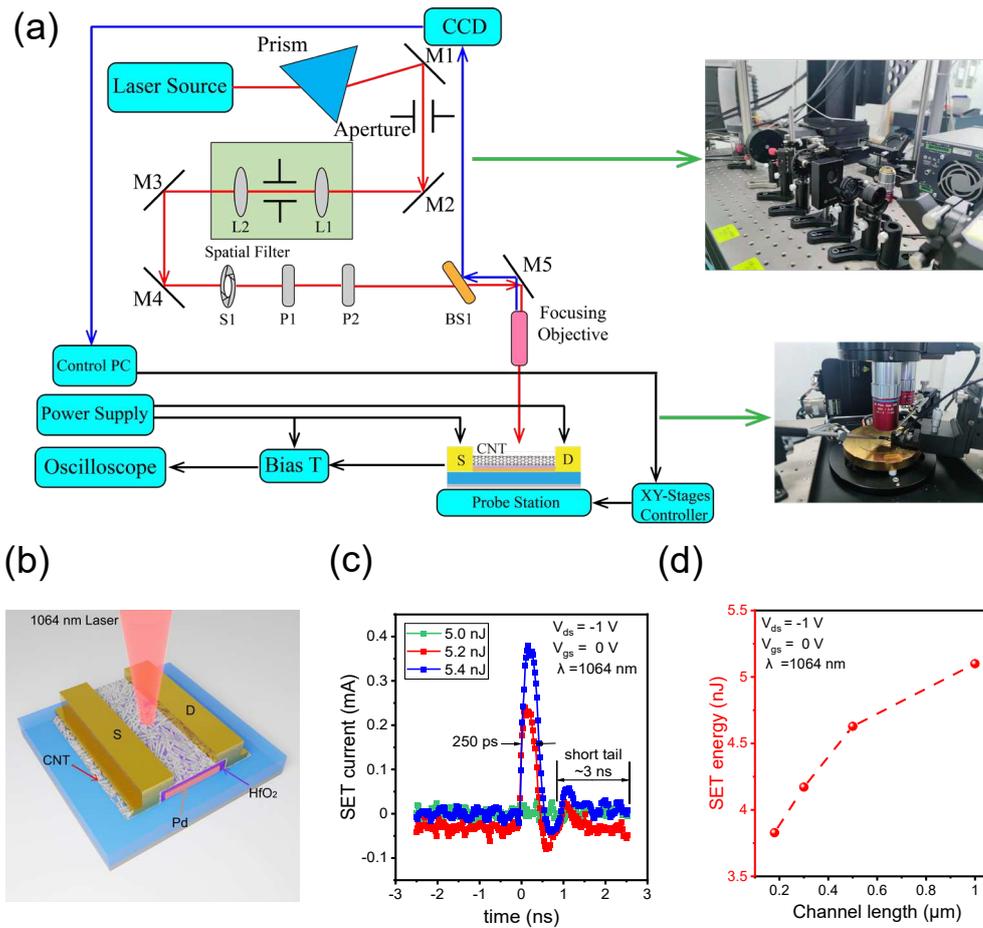


Fig. 2 | SEEs in CNT FETs. **a**, Simplified block diagram of the SPA test setup. In the figure, L represents a lens, M represents a mirror, S represents a shutter, P represents a polarizer, and BS represents a beam splitter. **b**, Schematic of a local bottom gate CNT FET exposed to a 1064 nm laser to test the SET effects. The CNT FET presents a channel length/width of $1 \mu\text{m}/10 \mu\text{m}$ and is measured under a bias condition of $V_{ds} = -1$ V and $V_{gs} = 0$ V. **c**, SETs of a CNT FET when irradiating the single event-sensitive region with different laser energies. **d**, Threshold SET energy for CNT FETs with different channel lengths.

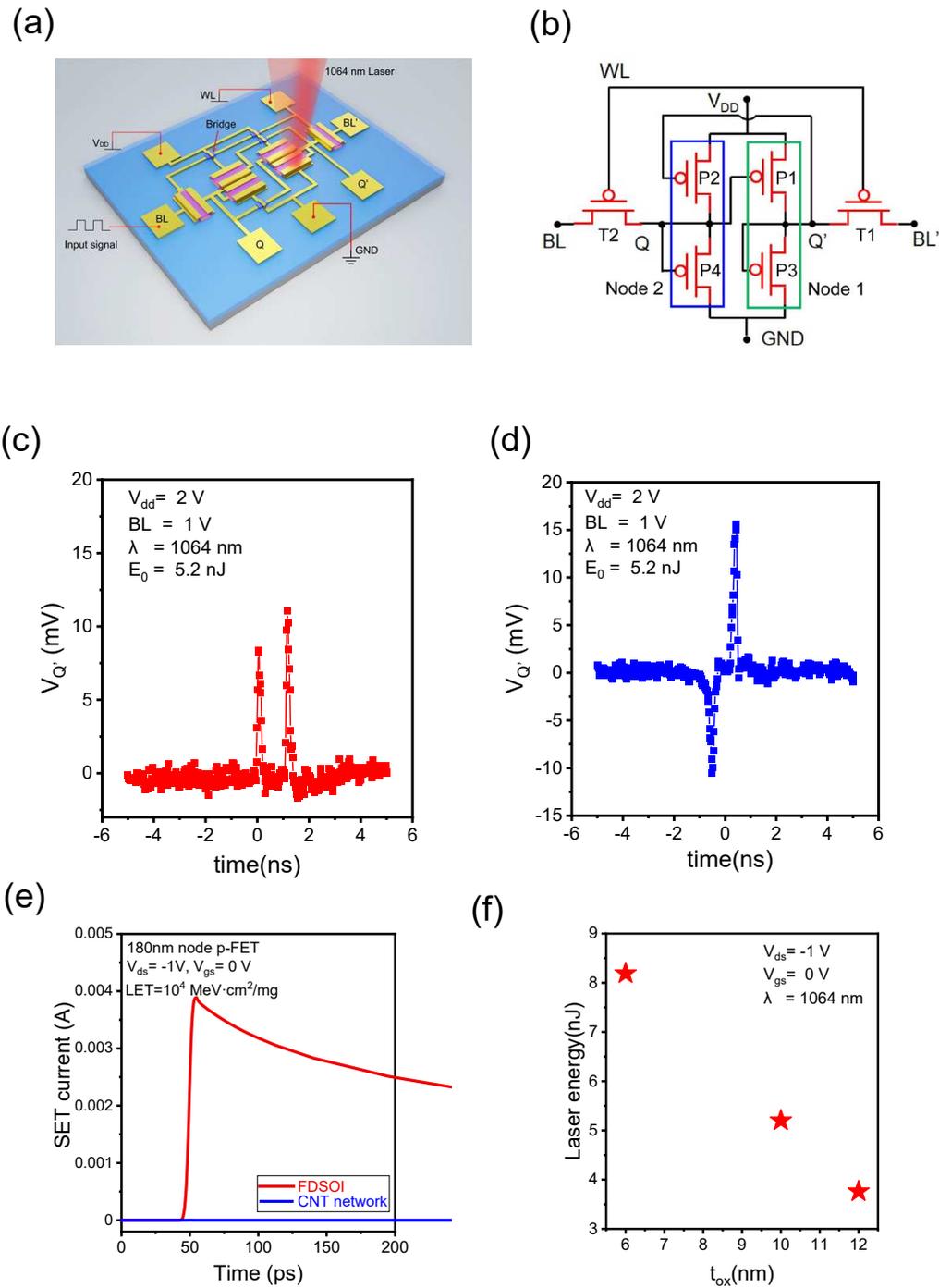


Fig. 3| SEEs in CNT SRAMs. **a**, Schematic of a local bottom gate CNT SRAM being exposed to a 1064 nm laser to test the SEU effects. **b**, Equivalent circuit diagram of the CNT SRAM. **c**, SEU effect for the CNT SRAM being exposed to a 1064 nm laser at P1. **d**, SEU effect for the CNT SRAM being exposed to a 1064 nm laser at P2. **e**, Simulated SET current of a 180 nm FDSOI FET and a CNT network FET. **f**, Threshold laser energy for SETs in CNT FETs with different gate oxide thicknesses.

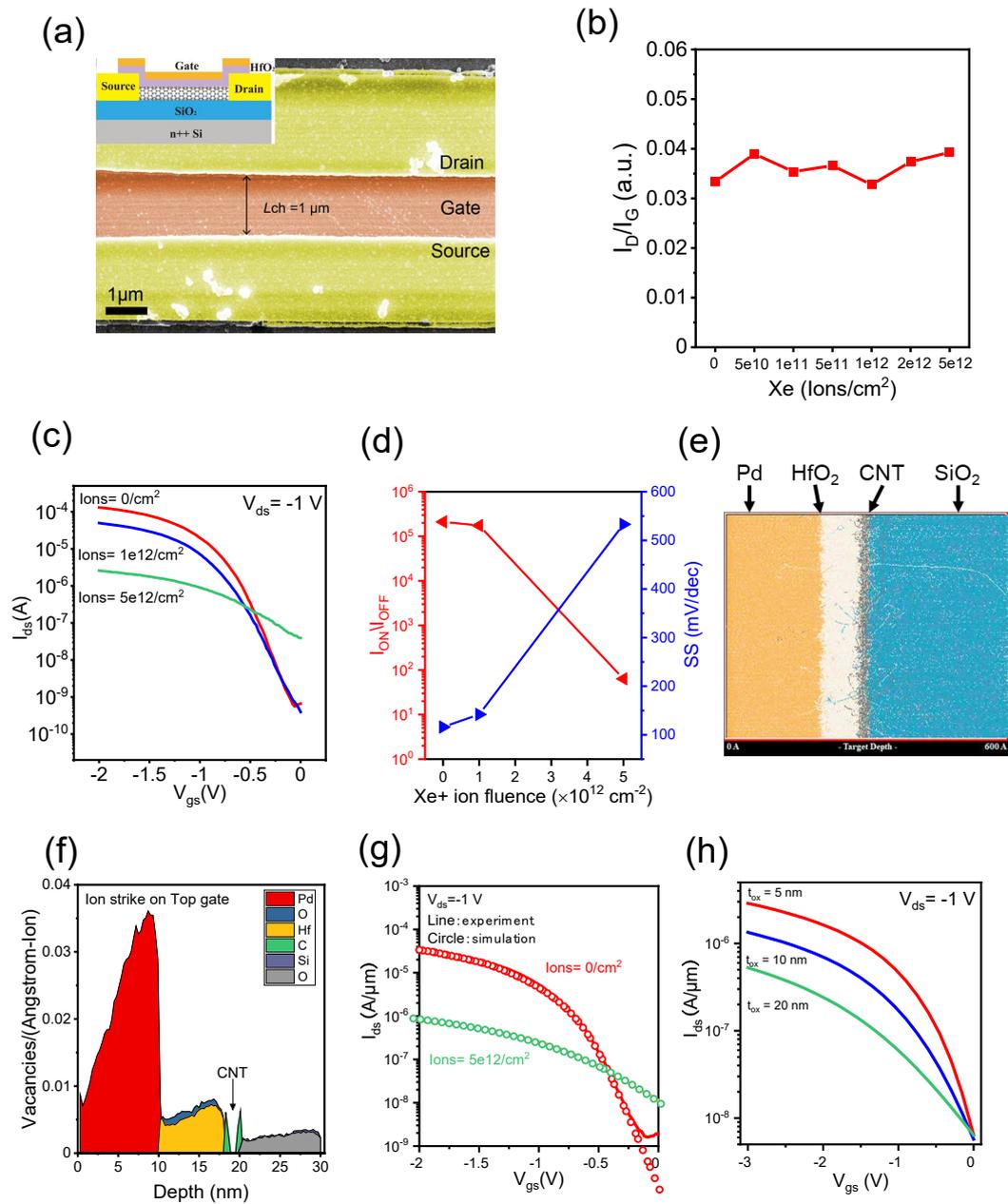


Fig. 4| DD radiation effects in radiation-hardened CNT FETs. **a**, False-coloured SEM image of an as-fabricated top-gated CNT FET. **b**, The statistical study on the ratio of the D peak intensity to the G peak intensity (I_D/I_G) with different heavy-ion fluences. Raman spectra of top-gated CNT FETs before and after Xe⁺ heavy-ion irradiation with different ion fluences excited by a 785 nm laser. **c**, Transfer characteristics of CNT FETs with different heavy ion fluences. **d**, I_{ON}/I_{OFF} and SS degradation trends in CNT FETs after irradiation with various Xe⁺ fluences. **e**, Simulation results of the radiation-induced vacancy distribution in the channel region. **f**, Vacancy densities in the depth direction. **g**, Simulated transfer characteristics of CNT FETs before and after $5 \times 10^{12} \text{ cm}^{-2}$ Xe⁺ ion irradiation. **h**, Performance predictions of CNT FETs with various HfO₂ dielectric thicknesses after $5 \times 10^{12}/\text{cm}^2$ Xe⁺ ion irradiation.

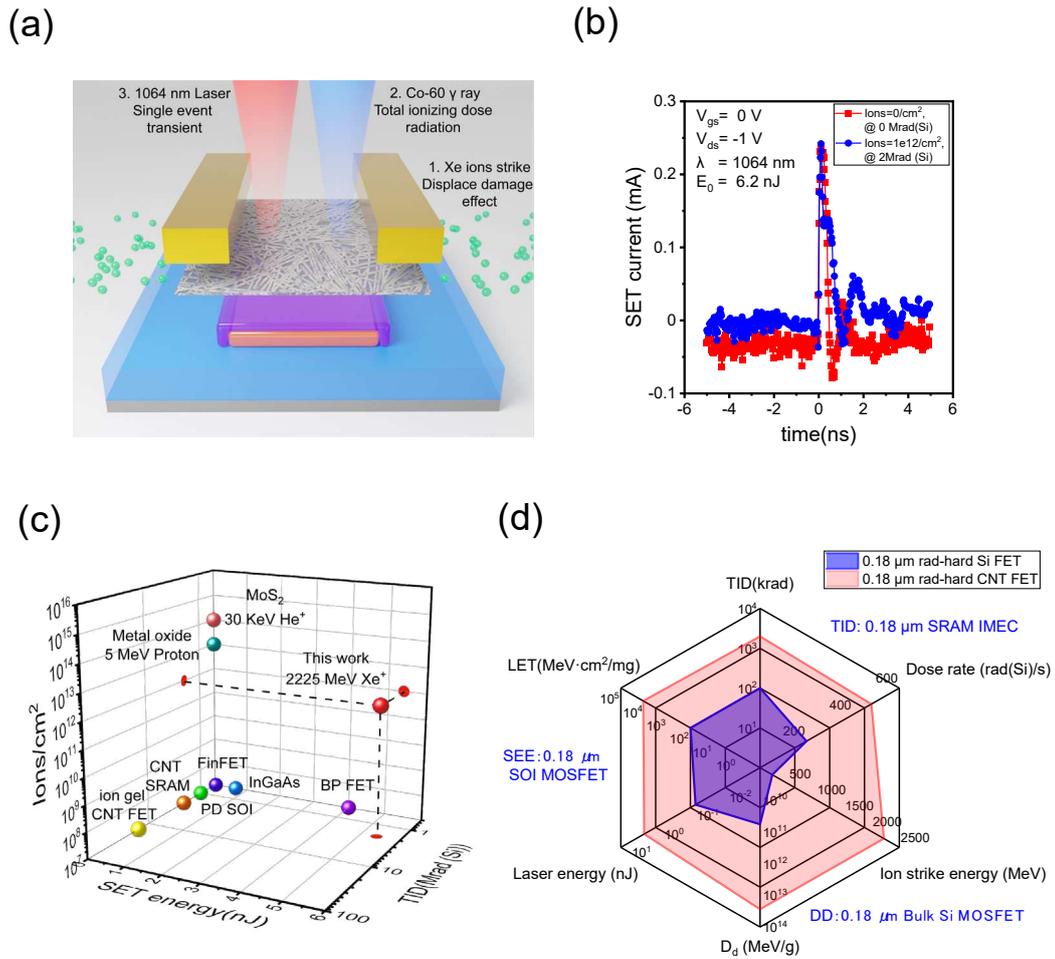


Fig. 5 | Comprehensive radiation effects in rad-hard CNT FETs and SRAMs. **a**, Schematic diagram of the experimental method to test the comprehensive radiation effects of CNT FETs and ICs. **b**, SETs of a CNT FET after being exposed to Xe⁺ and γ -ray irradiation. **c**, Comparisons of the radiation hardness properties of reported advanced technology devices with those of our CNT FETs and ICs. **d**, Benchmarking of the comprehensive radiation hardness properties of 0.18 μ m CNT FETs with those of reported rad-hard Si MOS FETs.

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