A Novel Hardmask-to-Substrate Pattern Transfer Method for Creating 3D, Multi-level, Hierarchical, High aspect-ratio Structures for Applications in Microfluidics and Cooling Technologies

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Abstract

This letter solves a major hurdle that mars photolithography-based fabrication of micro-mesoscale structures in silicon. Conventional photolithography is usually performed on smooth, flat wafer surfaces to lay a 2D design and subsequently etch it to create single-level features. It is, however, unable to process non-flat surfaces (already etched wafers) to create more than one level to give rise to multi-level, 3D, hierarchical structures in the substrate. In this study, we have described a novel cleanroom-based process flow that allows for easy creation of such multi-level, hierarchical structures in a substrate. This is achieved by introducing an ultra-thin sacrificial silicon dioxide hardmask layer on the substrate, which is first 3D patterned via multiple rounds of lithography. Then, this 3D pattern is scaled vertically by a factor of 200 – 300 and transferred to the substrate underneath via a single shot deep etching step. The proposed method is also easily characterizable. Using features of different topographies and dimensions, the etch rates and selectivities were quantified, these characterization information were later used while fabricating specific target structure. Furthermore, this study comprehensively compares the novel pattern transfer technique to already existing methods of creating multi-level structures, like grayscale lithography, chip stacking and double-sided etching. The proposed process was found to be cheaper, faster, and easier to standardize compared to other methods – this makes the overall process more reliable and repeatable. We hope it will encourage more research into hybrid structures that hold the key to dramatic performance improvements in several micro-mesoscale devices.

Introduction

Advances in lithography based micro-nano processing techniques have revolutionized the technology around the world for its ability to cost effectively mass produce structures ranging from sub-10 nm lengthscale all the way up to millimeter scale. Some of these structures include nanometer scale electronics components like FETs, IGBTs [1], sub-micron features like optical waveguides [2], Fresnel lenses [3], photonic devices [4], and micro-nanofluidic devices for DNA manipulation [5]. Slightly larger micro (1–100 μm) and meso (0.1–1 mm) scale features are even more useful in modern technology and has seen myriads of applications in microfluidics [6], cooling technologies [7, 8], battery research [9], sorption-desorption [10], desalination [11] and catalysis [12]. Although ubiquitous, versatile and indispensable as a micro-nano manufacturing technique, conventional cleanroom-based lithography suffers from one major limitation – it is unable to reliably create multi-level, hybrid, 3D hierarchical structures (structures with more than two levels of height or depth as shown in Fig. 1 (b, c)) of depths more than 1–2 μm. Conventional cleanroom processing can efficiently create only 2.5D or single-level structures (Fig. 1 (a)) but not true 3D multi-level ones (Fig. 1 (b, c)). Through conventional LELE (Litho-Etch Litho-Etch) route, a 2D design/pattern (full control available over the design in 2D) is first laid on a sacrificial mask layer deposited on the wafer using photolithography techniques. This mask is now used to cut/etch (or extrude if material is deposited/grown) that design onto the wafer. Through one round of (lithography + etching) the entire design can be etched to only one specific depth (different parts of the design cannot be etched to different depths). Conventional LELE cleanroom processes flows would normally require multiple rounds of (lithography + etching) to achieve the desired multi-level structures. The bottleneck arises due to unsatisfactory second round of lithography on wafers which have already gone through one round of (lithography + etching) and thus has etched features (~ 5 μm or more) in them. This comes as a major manufacturing hurdle in a time when hybrid surfaces hold the key to dramatic improvements in the performance of existing state-of-the-art devices.

Multi-level, 3D structures can be made with ease from soft materials like PDMS (polydimethylsiloxane), thermoplastics using deforming techniques (two-step soft lithography [36], sequential thermal [37] and UV [38]

Nano Imprint Lithography (NIL), Capillary Force Lithography [39], Nano Transfer Printing (NTP) [40]) although reliable methods for fabrication of 3D multi-level structures in rigid material like silicon is still lacking [35]. Recently, two-photon lithography have enabled us to make complicated fully 3D patterns in photopolymers [41, 42], but these systems have an extremely small print volume (< 300 x 300 x 300 μm^3 in the Nanoscribe GT, a state-of-the-art multi-photon system used in academia and industry) with equally long write times of more than 12 hours per structure. These reasons make two-photon lithography prohibitively expensive to use and difficult to integrate in commercial mass manufacturing scenarios [42, 43, 44]. Another technique called grayscale lithography (35–56) has gained some traction, which involves multiple steps of precisely controlled partial exposure (grey dose) of the photoresist to create a 3D multi-level structure, although, this method is often expensive, tedious, difficult to characterize. [] Waites et al. discussed the lack of standardization of grayscale lithography process steps because of severely limited control over several parameters that is inherently associated with gray-litho [47]. Some of these challenges encountered in grayscale lithography are complicated and expensive mask modelling, dose dependent dimension distortion, feature size dependent shifting of characteristic response curve of photoresists, profile welling and sidewall tapering at gray doses, all of which make the target resist profile difficult to achieve [44]. Waites et al. further states that making accurately controlled gray features is so heavily dependent on process conditions and operate within such tight tolerances that transferring recipe or process knowledge from one lab to another is almost impossible.

Recently, an ingenious double-sided processing technique (also demonstrated in Fig. 1 (d)) has been developed by Hazra et al. to create extremely high aspect ratio microchannel (~ 100 μm width) 2-level manifold structures [58, 62]. Although this method is not suitable for creation for all kinds of structures (Fig. 1 (c), (f)) since these 2-level structures are made via intersection of two designs etched from both sides of the wafer. Furthermore, the yield of 3D structures made via conventional or double-sided micro-lithography techniques on rigid Si wafers, drop drastically to about 50% because of manual handling of fragile wafers which have already gone through a round of deep Si etch. [57, 58]. Commercially, the creation of taller (> 50 μm) multi-level structures have traditionally been performed via chip stacking methods [24, 62]. In this approach, a fully 3D design is split into several different 2.5D structures, these 2.5D structures are fabricated in separate wafers using conventional lithography which are then stacked together using solder die-attach or thin eutectic bonding technologies. The wafer thicknesses determine the step heights achievable through this process and often to achieve small step heights, the wafers need to be thinned down using a back-grinding tool. Wafer thinning is also not possible below 30–50 μm which puts quite a large limitation on the minimum step height that is achievable through this process. Moreover, extremely thin wafers are prone to warping, chipping and breakage. The final bonded chip-stacked configurations are short-lived and unreliable, the bonding sites being the primary source of failure in devices that go through massive cyclical thermal or mechanical stresses [59, 60], especially, microfluidic cooling devices. Additionally, chip stacking techniques have their limitations in terms of the device configurations it can fabricate, since the middle wafer layers of the stack cannot have free standing structures (for e.g., multi-level pin fin array structures cannot be made using this technique). Thus, current microfabrication community is in desperate need of a standardized, easily characterized process to make high aspect ratio, tall (> 100 μm) micro-mesoscale multi-level structures that is cost-effective, uses commonly used microfabrication processes, can operate between reasonable process and tool tolerances, and thus can be translated easily from one lab to another.

In this paper, a novel Silicon Oxide to Silicon pattern transfer process is described to reliably create multi-level structures using photolithography techniques in order to solve several of the practical challenges that arise while employing existing state-of-the-art methods like chip stacking, double side processing and grayscale lithography.

The pattern transfer process is achieved through a single shot deep silicon etching steps which translates into an improvement in manufacturing yield by more than 40%. Furthermore, Si : SiO_2 etch selectivity is more than an order of magnitude higher compared to Si:Photoresist etch selectivities [49–55], the use of Silicon dioxide as a sacrificial layer during this pattern transfer process, enables us to create really tall structures (up to 500 μm) the likes of which will be immensely useful in applications that rely on mesoscale structures and features. The process described is easy to standardize and thus, eliminates difficult characterization associated with grayscale lithography. Coupled with easy characterization, the process also employs very commonly used cleanroom-based tools and functions to create multi-level microstructure – this makes knowledge transfer from one lab to another much easier. This letter additionally details a one-shot characterization method and data of SiO_2 and Si etch specific to the tools and step conditions used. Finally, this letter shows SEM images of several 2-level and 3-level microstructure that were fabricated using 3D patterned SiO_2 hard-mask obtained via two rounds of lithography and etch, although the possibilities are endless. Finally, this letter ends by listing a few exciting structures whose fabrication is now made possible, and which could pave the way for the next generation of high-performance microfluidics and cooling devices.

Methods

The novel process described in this paper draws inspiration from multi-lithography techniques and grayscale lithography. It cleverly combines the two to solve several practical challenges associated with Photoresist based grayscale lithography technique for reliable fabrication of multi-level 3D structures. In conventional lithography, creation of etched features usually follows these steps delineated in Fig. 1 (h, i, j) – a) Coating Photoresist (PR) on the wafer; b) Exposing 2D design on the PR and developing the design and c) Deep Si etch to define the features. To achieve multi-depth structures using this conventional LELE (litho-etch-litho-etch) technique, where different parts of the wafer need to have different etch depths, the sequence of steps (a, b and c) needs to be repeated multiple times with a different exposure design in step b, and different etch time in step c. The primary challenge arises in the photoresist spinning step (a) itself when PR is attempted to be spun on the wafer with features already etched in them. The spinning process works via PR being puddle dispensed at the center of a Silicon wafer spinning at a high RPM, making it spread radially outward to create a thin (1 μm to 10 μm depending on PR viscosity and spin RPM), uniform and conformal coating over the wafer. The second step spinning process is satisfactory (thin and uniform) when the PR thickness (1–10 μm) is much larger compared to the etch height of the features. Thus, in cases (some cases of IC fabrication) where the already etched feature height is < = 1 μm, the LELE process works perfectly, but in several applications of microfluidics, liquid cooling, optics and semiconductor fabrication, these etch depths can range anywhere from 1 μm to 500–600 μm. PR spinning on such large step heights lead to unsatisfactory coating in step a (Fig. 1 (k)). Several problems like streaking (PR layer being wrinkled after hitting an etched feature), fingering (PR getting trapped in a deep cavity/channel and progressing along those channels only), and incomplete coverage (PR hitting the corner of an etched feature and failing to cover the rest of the wafer) mar the spin coating process in step a – thereby leading to failure of the whole process.

In this context, we have invented a novel process flow using commonly used cleanroom tools which mitigates all these problems and enables us to create multi-level hierarchical structures with ease. Inspired by grayscale lithography's idea of 3D patterning the photoresist, we have first introduced an additional ultra-thin SiO_2 layer (< 3 μm) in between the PR and the Silicon wafer. The idea is to perform multiple rounds of conventional LELE lithography and SiO_2 etch to pattern this newly introduced SiO_2 mask layer, instead of attempting to pattern the Silicon directly. After this, by deep Si etching, this 3D multi-level pattern in the SiO_2 gets scaled vertically and

transferred to the Silicon. In this new process flow (Fig. 2) the steps are as follows – i) Deposit Silicon Oxide hard-mask on the wafer; ii) Spin coat PR on the SiO_2 (same as step (a)); iii) Expose 2D design on the PR using appropriate UV light source and develop the exposed zone away (same as step (b)); iv) SiO_2 etch to desired height followed by stripping the remaining PR. Multiple rounds of step (ii, iii and iv) (lithography + SiO_2 etch) are performed on the wafer to create a hierarchical multi-level structure in the SiO_2 layer itself. In this situation, the most crucial step (step a or step ii) of spinning the PR on the SiO_2 coated wafer works perfectly since the PR coat (4 μm) is much thicker than the step heights (1–3 μm) in the SiO2 layer. These multiple litho rounds enable creation of a multi-level, 3D, structure in the SiO_2 hard-mask layer. The final step (v) single shot Deep Si etch enables us to translate the 3D structure that was created in the SiO_2 by scaling it vertically and transferring it to the Silicon layer underneath. The scaling ratio is the etch selectivity or ratio of etch rate of Si to etch rate of the mask layer, SiO_2 obtained using specific etching tools or recipes. Additionally, SiO_2 is much superior to hardened PR as an etch stop mask layer providing Si : SiO_2 selectivity of 200–300 during deep Si etch using the Bosch process (for comparison, same etching recipe provides a maximum Si : PR selectivity of 80–100), which enables us to create structures as tall as 400–500 μm. The specific process flow employed in this study can be found in the Supplementary Information.

Processes like lithography (step a, b, ii, iii), SiO_2 deposition or growth on Si wafer (step i), SiO_2 etch (step iv) and DRI Etch of Silicon (step v) are very commonly employed in the cleanroom microfabrication community, thus making it easy to characterize (using a simple mask with varying feature dimension) and standardize for general use. Preliminary tests have demonstrated the ability to create 3D hierarchical features of nominal dimensions (width) ~ 5–10 μm with aspect ratios (height/width) as large as 10–15. The resolution can be further improved by using e-beam lithography instead of conventional lithography.

The process flow of creating multi-level structures has been tested 3 times with different orders of step heights (250 nm through 900 nm) to establish reliability and repeatability. Moreover, this process employs only a single step of deep Si etch, thus making it much less expensive and time consuming as compared to the conventional lithography route which employs multiple rounds of deep Si etch (number of levels required in the structure = number of deep Si etch steps). This will increase throughput while simultaneously reducing cost per device when used in an industrial mass production scenario.

The proposed concept of fabrication, which involves multi-lithographically patterning a thin masking layer and then transferring that pattern to an underlying substrate through etching can be extended to other mask material and substrates as well. Instead of CVD Silicon dioxide, thin metal layers (Au, Pt, Cr, W, Al) or other oxide materials (Alumina) can also be used as the mask layer. Superior etch selectivity of 10^5 has been observed during DRIE of Silicon with an Al mask layer [61] – thus combining this with our method will enable the creation of extreme aspect ratio (> 35) multi-level structures. These new masking materials can also be deposited or grown on our wafer through other techniques like evaporation, sputtering, ALD or electroplating. Similar to our current process, a single characterization run will be required to quantify the etch rates and selectivities specific to the tools and process conditions used – these parameters will then be used to design the process flow for obtaining our final target multi-level structures.

The resolution and repeatability of the process depends on our ability to precisely characterize the etch rate of Silicon, etch selectivity between Si and SiO_2 during DRI etching in the PTDSE and the etch rate of Silicon dioxide in the Oxford RIE. Three different characterization wafers with several designs of straight microchannels and square

pillar arrays were used on three different days. They were etched for varying durations using a 600–800W plasma of CHF_3 and CH_4 in a 3:1 ratio in the Oxford RIE. The findings are summarized in Fig. 3.

Following detailed characterization of the oxide etch rate using our specific recipe, we can precisely construct 3D structures in Silicon oxide. The target structures for our extreme heat flux cooling devices are extremely tall (~ 500 μm) needing 3–4 μm SiO_2 layer as the mask. We have chosen an aggressive oxide etch recipe with good PR: SiO_2 selectivity of > 1. This is necessary in order to be able to etch the thick SiO_2 layers (up to 4–6 μm) using relatively thinner PR layer (4 μm, thus maintaining sub-10 micron resolution). Although, the drawback of choosing an aggressive etch recipe leads to increase in vertical resolution of our target structures. As seen in Fig. 3, which plots the etch per second (Å/s) as a function of the total etch time and feature dimension, the average etch rate was well controlled within 45 and 54 Å/s for a wide range of target structures and for all etch durations above 1 seconds (at 1 second, the etching is severely starved of plasma and etch rate is much lower, ~ 30 Å/s) Thus, the vertical resolution of the 3D structures using our etching recipe is limited around 10 nm (obtained through a 2 sec etch) in the SiO_2, which translates to around 2–3 μm when the step is scaled and transferred to the Silicon wafer through DRIE. The etching recipe can be tuned (flow rates of respective gases can be reduced, CHF_3 and CH_4 ratio could be decreased) to make it less aggressive, and thus reduce the etch per second value – this will lead to better control of the etch, and sub 10-nm resolution in the SiO_2 3D structure (and sub-micron level vertical resolution in the final Silicon structure). Following characterization of the oxide etching step, the Deep Silicon etching recipe used in the PTDSE for pattern transfer was then estimated using a test wafer and straight channel dimensions of 100–200 μm. The average etch selectivity over 200 μm of etch was found to be around 270–275. This etching recipe was developed extensively by a previous work by Hazra et al. who reported etch selectivity of 220–240, and etch rate of 8 μm/min. [58] The DSE recipe used by Hazra et al. [58] was also extremely aggressive in order to accommodate their extreme total etch height of 1000 μm, although this aggressive recipe leads to a reduced Si : SiO_2 selectivity. In our present study, the recipe was slightly modified (etchA time was reduced to 3.1 sec from 3.3 [58]) to increase selectivity and attain straighter, more anisotropic etch profile. The progression of etch for our characterization structures (perpendicularly placed straight channels arrays of different widths and spacings between 100 and 400 μm) were investigated. 172 μm of Silicon was found to be etched for 0.61 μm of oxide, thus making the average Si : SiO_2 etch selectivity ~ 282.

Results And Discussion

Different types of multi-level features with varying feature widths and heights and topographies are presented in Fig. 4.

Usually, the number of (lithography + SiO_2 etch) steps is equal to the number of levels required in the multi-level structure (observe Fig. 2 (1)–(9)), although it was soon realized that further simplifications could be made easily to reduce the number of processing steps required for these structures. For example, the final step height in the SiO_2 layer could be entirely replaced with a baked Photopolymer, thus reducing one round of (litho + SiO_2 etch). Although this would require designing the fabrication flow while accounting for the different etch rates and selectivities of PR, SiO_2 and Si during the process. In addition to these simplifications, mask designs themselves can be cleverly combined and overlapped between different rounds of (litho + SiO_2 etch) which gives rise to more levels using lesser number of rounds of (litho + etch). An example has been demonstrated in Fig. 5, where two rounds of (litho + etch) involving 2 masks could generate a 3-level structure. More such structures are seen in Fig. 4 (g, i, j, l, m) all of which are made by overlapping 2 masks (the exact mask designs are left as exercises for the reader). Figure 5 also

briefly discusses an issue that might arise during the design exposure phase of lithography while making extremely tall structures. The dimensional accuracy and exposure quality by the MLA Heidelberg Maskless aligner depends on two main parameters – the exposing light energy (dose) and the location of focus (defocus) with respect to the PR top surface, although the exposing energy is the primary determinant. It has been observed previously that a ± 1 μm change in the defocus value from the optimal does not affect the exposure step significantly – this suggests that if the 3D features and step heights in the SiO_2 is low enough (sub-micron), exposure quality is relatively unaffected. Overlapping designs were tested for step heights from 0.5 μm to 1 μm and exposures were found to be satisfactory on both the levels (Fig. 5a – c). When photolithography is attempted on SiO_2 step heights which are more than 1.5 μm apart, the exposure qualities on the two different levels of the SiO_2 might be slightly different (as shown in the schematic in Fig. 5d – e, one of the levels might be over or underexposed) and this should be taken into consideration during the exposure step. One easy and quick fix is to not alter the defocus value (indicating that the lower level might be under-exposed and residual PR might be left behind), but increase the downstream descumming step duration to 2 mins or more. The extra O_2 plasma step removes all the residual PR from both the SiO_2 step surfaces.

The novel method has been extensively compared with existing methods in Table 1.

Table 1

Detailed comparison between existing state-of-the-art fabrication methods with SiO2-Si pattern transfer process

	1. Chip Stacking	*2. Double Sided Processing*	3. Grayscale Lithography (Photoresist – Si substrate)		4. Novel SiO_2-Si pattern transfer (PR – SiO_2 – Si)
			A. Optical Mask Assisted	*B. Maskless Direct Write*	
Brief Description	Produces multi-level 3D structures by breaking them in multiple 2.5D structures – current commercial go-to (Fig. 1 (e), (g))	Double sided etching to make 2-level structures out of 1 wafer instead of 2 that would be needed by conventional chip stacking (Fig. 1 (d))	Relies on accurately designed micro-nano scale patterns in the gray zone of an optical photomask, which partially blocks the full exposure dose to achieve a gray dose and partial development of the PR. 3D pattern on the PR is transferred to Si through DRIE etch.	Instead of an optical photomask, this process depends on the exposure tool's capability to directly modulate exposure energy between different parts of the design to achieve varying amounts of PR washed away from these zones during development.	Multiple rounds of (maskless direct write full exposure photolithography + SiO_2 etch) is performed to make a 3D pattern on a thin SiO_2 layer on top of the Si. Compared to grayscale lithography, an additional SiO_2 layer is introduced between the PR and Si substrate, which will now act as the etch stop layer during DRIE etch.
Lithography Mask	Optional. Both masked methods or maskless methods can be used for full exposure lithography.		YES, requires a physical optical photomask • Very expensive to fabricate [49–55] • Designing step requires multi-objective complex modelling to determine gray zone pattern dimensions – tedious [44] • Designing mistakes are costly – leads to wastage of processing time and money	NO, does not require a physical mask • Digital mask increased room for error during design • No wastage of time and money associated with physical Chrome-on-glass mask fabrication	NO, does not require a physical mask Although, our process involves full exposure lithography only, thus maskless litho can be replaced by multiple masked lithography for mass manufacturing scenarios (note, this is easy since no gray litho masks are involved)
Etch stop layer	Usually PR	PR or SiO_2	Photoresist (can be up to 5μm thick)	Photoresist (thin, usually < 2 μm)	Ultra-thin (up to 3–4 μm) SiO_2 layer

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Etch Selectivity	Up to 100	180–240	Up to 100 for specific design and RIE recipe	Demonstrated up to 30	200–280
Total feature height demonstrated	Wafers in the middle of the stack can NOT have free standing structures. Eg. A micro-pillar array with different heights cannot be made using this method since pillars are free standing features.	Since double sided etching is needed, one of the levels must be the wafer backside (through etched) – this severely limits the type of structures that can be made	Up to 250 μm [46]	• Low height, 10 μm based on > 10 published research [49–55] • Eckstein et al. [53] developed a special illumination tool to achieve 75 μm tall structures • Heidelberg instruments, a premier maskless tool manufacturer reports an upper height limit of 60 μm [44, 53]	• No restrictions on structure type like in Chip stacking or double sided processing. • Capability more than 500–600 μm (demonstrated up to 350 μm) The use of high etch selectivity SiO_2 as the intermediate layer solves the issue of low feature heights. Using 3 μm of SiO_2 potentially enables us to create > 600 μm tall structures.
Feature lateral dimensions	Sub-10 μm resolution	Limited by aspect ratio achievable through DRIE	~ 10 μm or much more than the pixel dimension (1–2 μm) in gray zones.	Sub 10-μm resolution	Sub 10-μm resolution
Number of gray-levels (Maximum number of levels in the structure that can be made in the multi-level structure)	n gray levels require n wafers carefully ground to specified level heights	2 level only (1 level has to be through etched)	Limited by the mask fabrication capability, stepper resolution, upper dose level without pixel recreation	Limited by stepper resolution, PR response curve	No limit (number of lithography step which can be as few or as many = number of levels)
Etch stop layer profile control			Most issues regarding etch stop profile arises during the gray level exposure step		

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	Standard	Standard	Very difficult even with a perfectly difficult mask [44, 48] • Rough PR surface after partial development • Gray zone profile tapering, "well"-ing • Higher dose unwanted pattern recreation	Very difficult [52] • Gray zone profile tapering, "well"-ing • messy PR surface after partial exposure and development • High post etch surface roughness	Standard – Our process eliminates all gray exposure steps. Full exposure multiple round photolithography is used to 3D pattern the SiO_2 layer with the steps being perfectly vertical anisotropic (SiO_2 wall profile angle can be changed too by tuning oxide etch recipe)
Etch stop profile correction	Standard	Standard	Difficult – Expensive (physical mask) and time-consuming (mask making lead time)	Two methods which are both expensive and cumbersome [44] – • Through thorough characterization – tedious • 3D proximity effect correction (PEC) – expensive	Profile correction only involves characterizing oxide etch rate as a function of feature dimension which can be easily done using a simple characterization mask
Characterization Step	Difficulty of the etch stop layer profile control and correction directly correlates with the difficulty of the characterization step				

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	Only etch needs to be characterized Extremely low yield (50–60%) since it requires handling of fragile wafers with deep etches [57, 58]		Extremely difficult characterization step [49–55] – • Difficult profile control and correction • Each design requires extensive, individual, characterization • involves making a detailed dependence map from pattern dimension ◊ reduced light intensity ◊ PR height – this is difficult and cumbersome especially with physical masks • Dimensional inaccuracies by gray zone profile distortion	Extremely difficult characterization step [44, 49–55] – • Difficult profile control and correction • Each design requires extensive, individual, characterization • Feature dimension dependent PR response curve shifting • Dimensional inaccuracies in gray exposure regions • Almost impossible to correct profile distortion issues (e.g. Profile “well”-ing) that arise due to gray level exposure	Standard, only etching needs to be characterized – • Easy profile control and correction • Individual Characterization step NOT required for each design • Full exposure photolithography eliminates all the issues regarding profile distortion and dimensional inaccuracies • For each lab (set of tools), one etching run using a characterization mask is sufficient to quantify Si, SiO_2 etch rates and selectivities. These data can then to be used to design masks for the final target structure.
Standardizability	High level of failure at bond sites during stress cycling [59, 60]	Wafer breakage during handling [57, 58]	Difficult because of gray profile distortion issues	Difficult because of gray profile distortion issues	Easy (no gray exposure step). Single etch step replaces multiple ones thus eliminating any manual handling. Also, since the multi-level structure is made of one wafer no bonding required
Process tolerances		Tight	Tight (narrow window of process parameters)	Tight (narrow window of process parameters)	No tight process tolerance (easy to use tools and processes)

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Knowledge transfer	Easy	Difficult	Difficult because of tight process tolerance	Difficult because of tight process tolerance	Easy, because of relatively simpler characterization and standardization steps.
Potential for commercial use	Commercially used	Usable	Difficult to use commercial because of poor process reliability, difficult characterization, tight process tolerance [49–55]	Difficult to use commercial because of poor process reliability, difficult characterization, tight process tolerance [44]	Easy since it is easy to characterize and standardize. This recipe also uses very commonly used tools and processes (SiO_2 CVD deposition, lithography, SiO_2 and Si etch) so easily integrable with existing cleanroom-based manufacturing lines
Process cost	$$$ (expensive)	$$$ (higher cost because of lower yield)	(most of it coming from physical masks)	$ (process) $$ (profile correction, characterization, and distortion correction)	$$ (slightly additional cost compared to 3B, associated with multiple rounds of lithography and SiO_2 etch)

Impact

This novel approach delineated in the letter allows us to precisely create multi-level, hybrid structures through an easy to characterize and standardizable process flow. Additionally, this novel method can also be used to introduce well-ordered surface roughness elements at the base of the microstructure and can replace conventional methods of creating stochastic surface roughness elements (wires [32], tubes [31], needles [34], broccoli [33], polyp [29]) which are harder to control and repeat. The ability to create 3D, multifunctional and hierarchical structures is especially important to the academic and industrial research environment right now, since myriads of micro-meso scale applications can benefit in performance by merely replacing conventional single-level device structures into multi-functional and multi-level, hybrid features.

Hybrid structures have been used in optical waveguides [13], micro-lens array systems [14], solar cells [15], photonic crystals [16], IR sources, metamaterials, surface area enhancement for water absorption, desalination, Carbon capture, battery technology, catalysis [6–12]. Hybrid structures also form the working principle behind several bio-inspired designs with targeted functionality [17, 36] like superhydrophobicity of self-cleaning lotus leaf, antifouling and drag reducing textures of shark skin and mollusk shells, anti-reflective moth-eye, photonic band gaps in

butterfly wings and superhydrophilicity or “water harvesting” capability of the micro-bumped Namib beetle skin [17]. Digital droplet microfluidics is hugely benefitted from hybrid structures, where structures with special surface enhancements can alter its wetting between the hydrophilic Wenzel and superhydrophic Cassie state [18, 31] Flow type microfluidic devices too are fully 3D multi-level hierarchical structures consisting of different types and sizes of features that have been etched to different depths in the substrate – microchannels for liquid flow (50–500 μm wide, 50–500 μm tall), inlet and outlet conduits (need to be etched through whole layer), and an active area (usually with much smaller feature dimension ~ 0.5–50 μm, which can consist of micro-pillar arrays for flow mixing [19], nanochannels ports and features for DNA manipulation [5], particle and cell sensing [20], sorting [21], separation [22] and analysis [23], contraction / expansion regions and jets for droplet generation) for device functionality. Moreover, hybrid structures probably have the most significant impact on improving the device performance in the field of microfluidic cooling. Hybridization of the Cold Plate side microchannel base (by introducing a microwick or surface features at the bottom of a straight microchannel) lead to increased thermal performance in forced fed microchannel cooling scenarios. [8] Zhu et al. reported heat transfer coefficient improvements from 17% to over 117% for microstructured microchannel compared to smooth microchannel, for 25 and 75 μm tall micropillars, respectively, using methanol as the working fluid without significant increase in pressure drop. [24] Passive heat spreaders like Heat Pipes and Vapor chambers with hybrid, bi-porous wicks instead of a conventional mono-porous one showed significant improvement in their heat spreading capabilities. [25] Dai et al. demonstrated that a complex hybrid wick when used in a heat pipe, leads to a massive 30 folds increase in maximum spreadable heat load as compared to solid Copper. [26] Zhou et al. validated the superior performance of hybrid two-level wicks in Vapor Chambers by reporting a 28% and 17% decrease respectively in device thermal resistance as compared to a state-of-the-art commercial monoporous and biporous wick TGP (Thermal Ground Plane) [27]. Moreover, our ability to reliably create multi-level hierarchical structures will allow us to aggressively scale up forced convection based active cooling device using a second 3D manifold layer for efficient fluid delivery. Pan et al. performed numerical simulations in ANSYS Fluent to compare Manifolded Coolers (MMC) design with Traditional 2D Coolers (TMC)s and showed that at same flow rates, the MMCs can achieve similar levels of thermal performance as the TMCs but achieve a massive 4x to 6x reduction in total device pressure and thus, 4x to 6x improvement in Coefficient of Performance (COP) [28]. Combining features of different dimensions and heights, within the same cold plate microstructure would also lead to increased device performance by increasing surface area and nucleation sites during single-phase and two-phase flow boiling respectively in forced feed microchannel coolers. Additionally, such hybrid wicks will also enable us to solve the mass transport limitations inherently imposed by thin evaporator wicks. In ultra-thin vapor chamber designs, the short pillars could be placed over the hot-spots to hold a very thin liquid film, leading to smaller thermal resistance and superior thermal performance and the tall pillars will act as liquid replenishment routes supplying enough wicking mass flow from the condenser back to the evaporator over large device areas. In addition to the above mentioned uses for multi-level structures, the active heat transfer 3D micro-featured surfaces themselves can be surface enhanced using this novel method. These surface enhancements lead to massive improvements in device metrics by enhancing the capillary wicking-based transport from the condenser back to the evaporator. This has been demonstrated by creating hybrid wicks using UV laser induced roughness [29, 33], hydrothermal ZnO Nanowire synthesis on silicon microstructure [24] and then performing capillary rate of rise tests and comparing with their non-hybrid smooth counterparts with no surface enhancements. Surface enhancements additionally increases the overall area available for heat transfer in forced fed convection and thin film evaporation scenarios [30], and leads to increased bubble nucleation sites in pool and flow boiling regimes. [7, 8, 32]

Some of the above mentioned applications help motivate the superiority of hybrid structures. Several orders of improvement will be achieved in many applications when conventional monoporous or single-level wicks are replaced by hybrid, multi-level wicks. We hope that this standardized recipe for manufacturing such multi-level structures will encourage more research, and eventually adoption of such structures in commercial devices and real life scenarios.

Conclusion

In this letter, we have detailed a novel Silicon Oxide (SiO_2) to Si pattern transfer process which uses multiple lithographically patterned thin SiO_2 layer to pattern the Si layer underneath. The extreme high etch selectivity between Si : SiO_2 etch of 200–300 enables us to create multi-level structures of extreme heights of > 500 μm in Silicon with a relatively thin (< 3) oxide layer on top. With the current oxide etch recipe selected, we obtain a stable resolution of 90–100 Å in SiO_2 for 2 secs of etch, this yields a vertical Si etch resolution of 2–3 μm in Si. With more tweaks to the etch recipe, the oxide etch per second can be reduced and resolution further refined. This process provides several advantages over conventional chip stacking, double-sided etching or grayscale lithography approaches, all of which have been summarized in detail in Table 1. The novel process has been used to create myriads of multi-level structures as shown in Fig. 4, furthermore, Fig. 5 shows how multiple lithography masks can be overlapped to create more levels using lesser number of litho masks. Such multi-level structures in the micro and mesoscale have far reaching applications in the fields of microfluidics, cooling technologies, biology, filtration, and energy as mentioned briefly in the introduction. Furthermore, our novel process solves several practical characterization and standardization challenges that mar the use of grayscale lithography to make multi-level hierarchical structures and thus arguably is more suited for commercial use. Difficult fabrication process is the primary reason behind multi-level, 3D structures not observed in commercial use. Having a standard recipe that can be easily translated from one lab to another will open a range of possibilities in research and development of such hybrid structures for the working devices and increase their performance by many folds.

Declarations

Data Availability

All data generated or analyzed during this study are included in this published article and its Supplementary Information files.

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References

1. Chen, Y. (2015). Nanofabrication by electron beam lithography and its applications: A review. Microelectronic Engineering, 135, 57–72.
2. Bojko, R.J., Li, J., Baehr-Jones, T., Hochberg, M. (2011). Electron beam lithography writing strategies for low loss, high confinement silicon optical waveguides. Journal of Vacuum Science & Technology B 29, 06F309.
3. Fricke-Begemann, T., Ihlemann, J. (2018). Hybrid micro-optical elements by laser-based fabrication of Fresnel lenses on the end face of gradient index lenses. Optics Express Vol 26, Issue 18, 23751–23759.
4. Fedeli., J.M., Cioccio, L.D., Marris-Morini, D., Vivien, L.,Orobtchuk, R., Rojo-Romeo, P., Seassal, C., Mandorlo, F. (2008). Development of Silicon Photonics Devices Using Microelectronic Tools for the Integration on Top of a CMOS Wafer. Advances in Optical Technologies, Vol 2008, ID 412518
5. Wang, C., Nam, SW., Cotte, J. (2017) Wafer-scale integration of sacrificial nanofluidic chips for detecting and manipulating single DNA molecules. Nature Communications 8, 14243.
6. Gale, B.K., Jafek, A.R., Lambert, C.J., Goenner, B.L., Moghimifam, H., Nze, U.C., Kamarapu, S.K. (2018). A Review of Current Methods in Microfluidic Device Fabrication and Future Commercialization Prospects. Inventions. 3, 60.
7. Liang, G., Mudawar, I., (2019). Review of poo boiling enhancement by surface modification. International Journal of Heat and Mass Transfer 128, 892–933.
8. Liang, G. Mudawar, I., (2020). Review of channel flow boiling enhancement by surface modification, and instability suppression schemes. International Journal of Heat and Mass Transfer 146, 118864.
9. Lixiang, L., Weng, Q., Xueyi, S., Zhang, L., Schmidt, O.G. (2017). Advances on Microsized On-Chip Lithium-Ion Batteries.
10. Chen, Y., Guo, M., Liang, H., Yang, W., Xu, L., Meng, J., Tian, X., Ma, X., Yu, Q., Hong, X., Mai, L. (2019). Scalable microfabrication of three-dimensional porous interconnected graphene scaffolds with carbon spheres for high-performance all carbon-based micro-supercapacitors. Journal of Materiomics 5, 303–312
11. Zhang, Y., Xiong, T., Nandakumar, D.K., Tan, S.C., (2020). Structure Architecting for Salt-Rejecting Solar Interfacial Desalination to Achieve High-Performance Evaporation with in Situ Energy Generation. Advanced Science News, 7, 1903478.
12. Navin, C.V., Krishna, K.S., Theegala, C.S., Kumar, C.S.S.R. (2013). Lab-on-a-chip devices for gold nanoparticle synthesis and their role as a catalyst support for continuous flow catalysis. Nanotechnology Reviews, vol. 3, no. 1, 2014, pp. 39–63.
13. Khan, M.U., Justice, J., Petaja, J., Korhonen, T., Boersma, A., Wiegersma, S., Karppinen, M., Corbett, B. (2015). Multi-level single mode 2D polymer waveguide optical interconnects using nano-imprint lithography. Optical Society of America Optics Express, vol 23, no. 11, 14630–14639
14. Aristizabal, S.L., Cirino, G., Montagnoli, A.N., Sobrinho, A.A., Rubert, J.B., Hospital, M., & Mansano, R.D. (2013). Microlens array fabricated by a low-cost grayscale lithography maskless system. Optical Engineering, 52.
15. Asim, N., Mohammad, M., Badiei, M. (2018). Nanomaterials for Green Energy Chap. 8: Novel Nanomaterials for Solar Cell Devices. Elsevier.
16. Camposeo, A., Persano, L., Farsari, M., Pisignano, D. (2018). Additive Manufacturing: Applications and Directions in Photonics and Optoelectronics. Advanced Optical Materials, vol 7, Issue 1, 1800419
17. Sun, J., Bhushan, B. (2019). Nanomanufacturing of bioinspired surfaces. Tribology International,, 67–74.

18. Dou, X., Zhang, D., Feng, C., Jiang, L. (2015). Bioinspired Hierarchical Surface Structures with Tunable Wettability for Regulating Bacteria Adhesion. ACS Nano. Vol 9, No. 11, 10664–10672.
19. Zhou, B., Wei, X., Syed, A.A., Chau, Y., Chen, L., Chew, B., Yassine, O., Wu, X., Yao, Z., Wen, W. (2015). Design and fabrication of magnetically functionalized flexible micropillar arrays for rapid and controllable microfluidic mixing. Lab on a Chip. 15, 2125–2132.
20. Feng, J., Liu, K., Bulusev, R.D., Khlybov, S., Dumcenco, D., Kis, A., Radenovic, A. (2015) Identification of single nucleotides in MoS2 nanopores. Nature Nanotechnology. 10, 1070–1076
21. Wunsch, B.H., Smith, J.T., Gifford, S.M., Wang, C., Brink, M., Bruce, R.L., Austin, R.H., Stolovitzky, G., Astier, Y. (2016). Nanoscale lateral displacement arrays for the separation of exosomes and colloids down to 20 nm. Nature Nanotechnology. Vol 11, 936–940
22. Huang, L.R., Cox, E.C., Austin, R.H., Sturm, J.C. (2004). Continuous particle separation through deterministic lateral displacement. Science. Vol 304, (5673), 987–90
23. Lam, E.T., Hastie, A., Lin, C., Ehrlich, D., Das, S.K., Austin, M.D., Deshpande, P., Cao, H., Nagarjan, N., Xiao, M., Kwok, P. (2012). Genome mapping on nanochannel arrays for structural variation analysis and sequence assembly. Nature Biotechnology. Vol 30 (8)
24. Zhu, Y., Antao, D.S., Chu, K., Chen, S., Hendricks, T.J., Zhang, T., Wang, E.N. (2016). Surface Structure Enhanced Microchannel Flow Boiling. Journal of Heat Transfer, vol 138, No. 9, 091501
25. Weibel, J.A., Garimella, S.V. (2013). Recent Advances in Vapor Chamber Transport Characterization for High Heat Flux Applications.
26. Dai, X, Tran, L, Yang, F, Shi, B, Yang, R, Lee, YC, & Li, C. Characterization of Hybrid-Wicked Copper Heat Pipe. Proceedings of the ASME/JSME 2011 8th Thermal Engineering Joint Conference. ASME/JSME 2011 8th Thermal Engineering Joint Conference. Honolulu, Hawaii, USA. March 13–17, 2011. T30005. ASME. https://doi.org/10.1115/AJTEC2011-44088
27. Zhou, F., Liu, Y., Dede, E.M. (2019). Design, Fabrication, and Performance Evaluation of a Hybrid Wick Vapor Chamber. Journal of Heat Transfer. Vol 141 (8), 081802.
28. Pan, M., Hu, M. (2020). Numerical Simulation of Manifold Microchannel Heat Sinks for Thermal Management in a Li-ion Battery. Chemical Engineering Technology. Vol 43, no. 12, 2501–2513.
29. Hazra, S., Liu, T., Asheghi, M., Goodson, K. (2020). Lasered Roughness to Increase Wicking Rates in Pin-Fin Microstructure. ASME 2020 International Electronic Packaging Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems. IPACK2020-2640
30. Bigham, S., Fazeli, A., Moghaddam, S. (2017). Physics of microstructures enhancement of thin film evaporation heat transfer in microchannels flow boiling. Scientific Reports 7, 44745.
31. Chen, C., Cai, Q., Tsai, C., Chen, C., Xiong, G., Yu, Y., Ren, Z. (2007). Dropwise condensation on superhydrophobic surfaces with two-tier roughness. Applied Physics Letter. Vol 90, 173108.
32. Yao, Z., Lu, Y.W., Kandlikar, S.G. (2013). Pool Boiling Heat Transfer Enhancement Through Nanostructures on Silicon Microchannels. Journal of Nanotechnology in Engineering and Medicine. Vol 3(3): 031002 (8).
33. Long, J., He, Z., Zhou, P., Xie, X., Zhou, C., Hong, W., Hu, W. (2018). Low-Cost Fabrication of Large-Area Broccoli-Like Multiscale Micro- and Nanostructures for Metallic Super-Hydrophobic Surfaces with Ultralow Water Adhesion and Superior Anti-Frost Ability. Advanced Materials Interfaces. Vol. 5, 1800353
34. Kang, Y., Wu, T., Han, X., Gu, H., Zhang, X. (2018). A needle-like reusable surface-enhanced Raman scattering substrate, and its application to the determination of acetamiprid by combining SERS and thin-layer

chromatography. Microchicmica Acta, 185: 504.

35. Kim, J.U., Lee, S., Kim, T. (2016). Recent Advances in Unconventional Lithography for Challenging 3D Hierarchical Structures and Their Applications. Journal of Nanomaterials. ID 7602395.
36. Greiner, C., Arzt, E., Campo, A. (2009). Hierarchical gecko-like adhesives. Advanced Materials, vol. 21, no. 4, 479–482.
37. Hirai, Y., Yoshida, S., Takagi, N. (2003). Defect analysis in thermal nanoimprint lithography. Journal of Vacuum Science and Technology B. vol. 21, no. 6, 2765–2770.
38. Kwak, R., Jeong, H.E., Suh, K.Y. (2009). Fabrication of monolithic bridge structures by vacuum-assisted capillary-force lithography. Small. vol. 5, no. 7, 790–794.
39. Suh, K.Y., Lee, H.H., (2002). Capillary force lithography: large area patterning, self-organization, and anisotropic dewetting. Advanced Functional Materials, vol. 12, no. 6–7, 405–413.
40. Carlson, A., Bowen, A.M., Huang, Y., Nuzzo, R.G., Rogers, J.A. (2012). Transfer printing techniques for materials assembly and micro/nanodevice fabrication," Advanced Materials, vol. 24, no. 39, 5284–5318.
41. Meza, L.R., Zelhofer, A.J., Clarke, N., Mateos, A.J., Kochmann, D.M., Greer, J.R. (2015). Resilient 3D hierarchical architected metamaterials. Proceedings of the National Academy of Sciences (PNAS). Vol 112, no. 37, 11502–11507
42. Piazza, A., Wu, Q. (2019–2020). Electroplated, Porous, 3D Metallic Structures using Sacrificial Two-Photon Lithography (Nanoscribe) Templates. Research Report, ENGR241, SNF, Stanford University. https://snfexfab.stanford.edu/sites/g/files/sbiybj8726/f/sections/diplayfiles/wq_finalreport_qw_ap.pdf
43. Houbertz, R., Declerck, P., Passinger, S., Ovsianikov, A., Serbin, J. (2007). Phys. Status Solidi A 204, 3662–3675
44. Grushina, A. (2019). Direct-write grayscale lithography. Advanced Optical Technologies. 8(3–4): 163–169
45. Waits, C.M., Modafe, A., Ghodssi, R. (2003). Investigation of gray-scale technology for large area 3D silicon MEMS structures. Journal of Micromech. Microeng. 13, 170–177
46. Waits, C.M., Morgan, B., Kastantin, M., Ghodssi, R. (2005). Microfabrication of 3D silicon MEMS structures using gray-scale lithography and deep reactive ion etching. Sensors and Actuators A 119, 245–253
47. Morgan, B., Waits, C.M., Krizmanic, J., Ghodssi, R. (2004). Development of a Deep Silicon Phase Fresnel Lens Using Gray-Scale Lithography and Deep Reactive Ion Etching. J. Microelectromechanical Systems, Vol. 13, No. 1
48. Khazi, I., Muthiah, U., Mescheder, U. (2018). 3D free forms in c-Si via grayscale lithography and RIE. Microelectronic Engineering 193, 34–40.
49. Stilson. C., Pal, A., Coutu, R.A. (2014). Fabrication of 3D Surface Structures Using Grayscale Lithography. Proceedings of SPIE 8973: Micromachining and Microfabrication Process Technology XIX, No. 8973.
50. Deng, Q., Yang, Y., Gao, H., Zhou, Y., He, Y., Hu, S. (2017). Fabrication of Micro-Optics Elements with Arbitrary Surface Profiles Based on One-Step Maskless Grayscale Lithography. Micromachines. 8, 314.
51. Dillon, T., Sure, A., Murakowski, J., Prather, D. (2004). Continuous-tone grayscale mask fabrication using high-energy-beam-sensitive glass. J. Microlith., Microfab., Microsyst., Vol. 3 No. 4.
52. Dixon, J., Solomon, M. (2018). Grayscale lithography for chiral nanophotonic structures. Research Report. ENGR241, SNF, Stanford University. https://snfexfab.stanford.edu/sites/g/files/sbiybj8726/f/sections/diplayfiles/finalreport2_jd_ms.pdf
53. Eckstein, H., Zeitner, U.D., Leitel, R., Stumpf, M., Schleicher, P., Brauer, A., Tunnermann, A. (2016). High dynamic grayscale lithography with an LED based micro-image stepper. Proceedings of SPIE Vol. 9780 97800T-1.

54. Huang, Y., Jeng, J. (2012). Forming a Fresnel Zone Lens: Effects of Photoresist on Digital-micromirror-device Maskless Lithography with Grayscale Exposure. Journal of the Optical Society of Korea, Vol. 16, No. 2, 127–132.
55. Ma, X., Kato, Y., Kempen, F., Hirai, Y., Tsuchiya, T., Keulen, F., Tabata, O. (2015). Experimental Study of Numerical Optimization for 3-D Microstructuring Using DMD-Based Grayscale Lithography. Journal of Microelectromechanical Systems, vol. 24, no. 6.
56. Mortelmans, T., Kazazis, D., Guzenko, V.A., Padeste, C., Braun, T., Stahlberg, H., Li, X., Ekinci, Y. (2020). Grayscale e-beam lithography: Effects of a delayed development for well-controlled 3D patterning. Microelectronic Engineering 225, 111272
57. Yadavali, S., Lee, D., Issadore, D. (2019). Robust Microfabrication of Highly Parallelized Three-Dimensional Microfluidics on Silicon. Scientific Reports, 9:12213.
58. Hazra, S., Piazza, A., Jung, K.W., Asheghi, M., Gupta, M.P., Jih, E., Degner, M., Goodson, K.E. (2020). Microfabrication Challenges for Silicon-based Large Area (> 500 mm2) 3D-manifolded Embedded Micro-cooler Devices for High Heat Flux Removal. 19th IEEE ITHERM Conference.
59. Chuang, R.W., Kim, D., Park, J., Lee, C.C. (2004). A Fluxless Process of Producing Tin-Rich Gold-Tin Joints in Air. IEEE Transactions on Components & Packaging Technologies, vol. 27, no. 1.
60. Hazra, S., Singh, Y., Asheghi, M., Goodson, K.E. (2020). Characterization and Prevention of Metal Overflow in Ultra-Thin Au-Sn Eutectic Chip Bonding for Packaging and Integration of Extreme Heat Flux Micro-coolers. Proceedings of the ASME 2020 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, InterPACK2020-2533.
61. Bagolini, A., Scauso, P., Sanguinetti, S., Bellutti, P. (2019). Silicon Deep Reactive Ion Etching with aluminum hard mask. Materials Research Express. Vol. 6, 085913.
62. Zhou, F., Joshi S.N., Liu, Y., Dede, E.M. (2019). Near-junction cooling for next-generation power electronics. International Communications in Heat and Mass Transfer 108 (2019) 104300

Figures

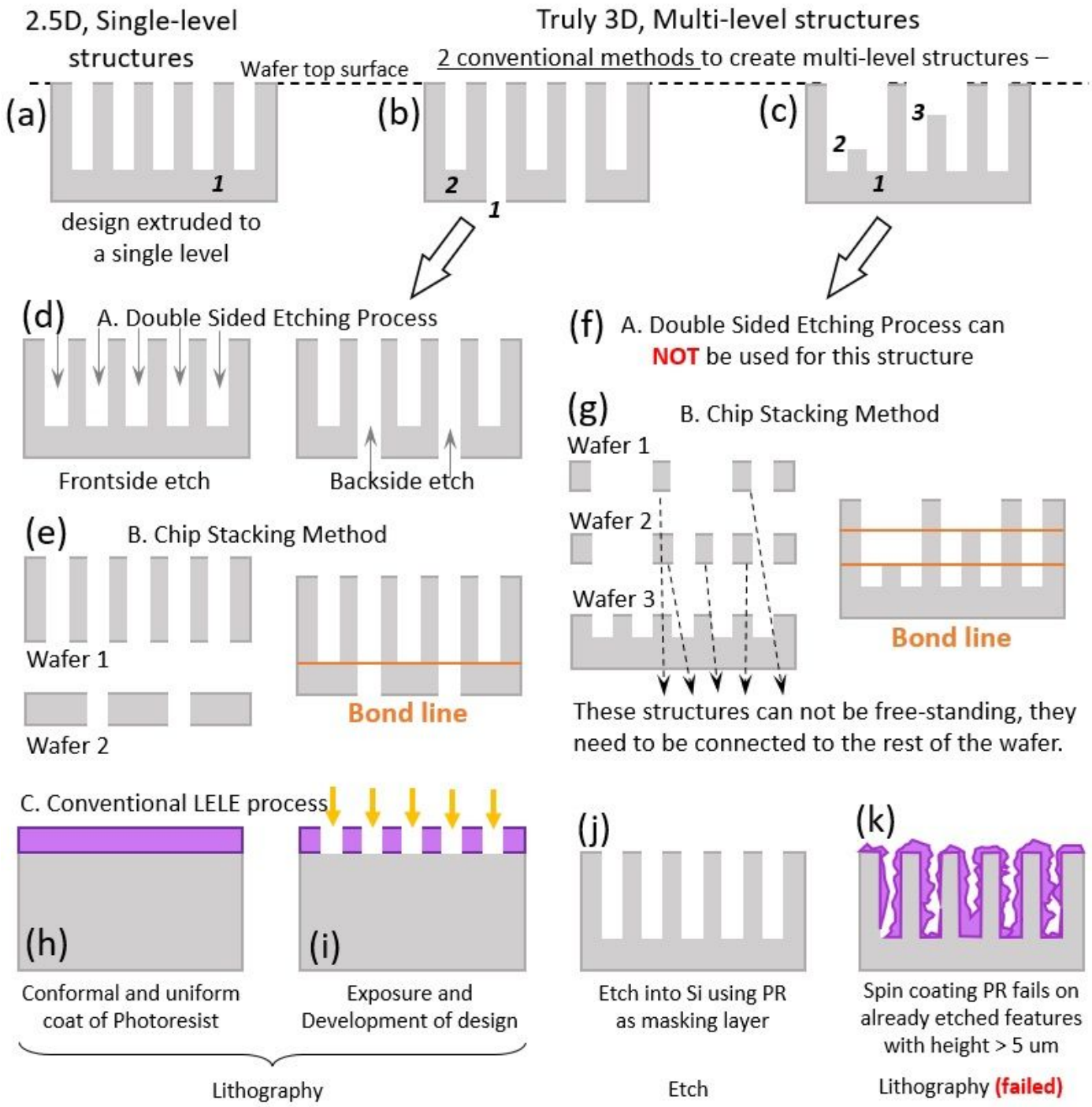

Figure 1

(a) Shows single-level structures, where all the features are of the same depth / height. These are also the structures that we will refer to as 2.5D structures throughout the rest of this letter. (b, c) In contrast to 2.5D structures, we show two different fully 3D structures which are multi-level; different parts of the wafer have different etch depth / height. (d) A newly developed solution of etching the wafer from both sides, for making specific kinds of 2-level structures where one of the levels are completely through etched. (e) Shows how the structure is (b) can be made using the commercial go-to approach of chip stacking. In this approach, the fully 3D multi-level structures are broken into several 2.5D, single-level structures. Each of these structures are made in separate wafers of appropriate thickness and then bonded together. (f) Shows severe limitations of double-sided etching process – this technique cannot make more than 2-levels, neither can it process wafers which do not have through etched

features. (g) Chip stacking is more versatile than double sided etching although it is not without limitations – the middle wafers cannot have free standing features. This explains why multi-level channels can be made using chip stacking but not multi-level pin fins (channels are attached to rest of the chip, while pins are free standing) (h, i, j, k) Shows the conventional LELE (Litho-Etch Litho-Etch) route that fail to create 3D structures. (h) PR is first coated uniformly on the wafer. Thin, uniform PR is crucial for success of the next step. (i) Exposure using a mask design – exposure quality is determined greatly by the uniformity of the PR layer obtained after the previous coating step. (j) The PR layer is used as a mask to etch into the Silicon. (k) To make another level, another round of lithography and deep Si etching needs to be performed, but lithography fails completely on wafers with already etched features. Since the etched feature heights are larger than the PR layer thickness, the spinning process employed to coat the resist on the wafer is not uniform and conformal – PR flowing over large feature steps encounter several problems like streaking, incomplete filling and fingering. Conventional LELE thus cannot be employed to make 3D, multi-level structures.

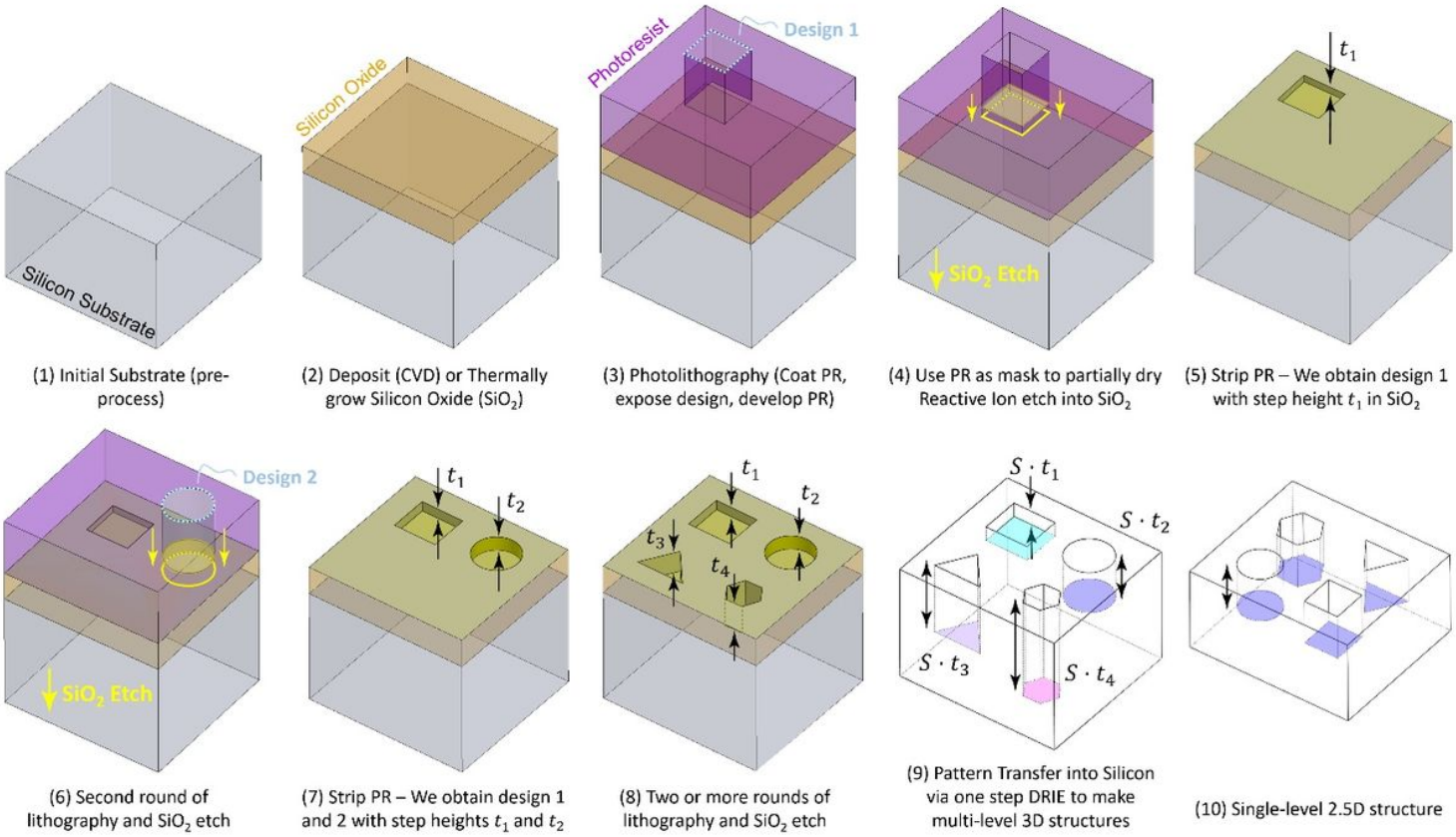

Figure 2

Overall process flow for creation of multi-level structures using proposed flow - (1) Clean bare wafer without features; (2) Intermediate ultra-thin masking material is deposited – in our case, SiO_2 is CVD deposited; (3) Photoresist spinning, exposure of Design 1, and development; (4) Using PR as mask layer, the underlying SiO_2 is etched to a precise amount, t_1; (5) Stripping PR; (6) Second round of lithography is performed – in this situation PR thickness is at least 1.5 times the maximum SiO_2 feature thickness already on the wafer, thus spin coating process is successful, yielding a thin conformal coat all over the 3D featured SiO_2. This time design 2 was etched in SiO_2 to a different depth, t_2; (7) After two rounds of litho, a 2-level structure is made on the SiO_2; (8) After two more rounds of litho, 2 more levels can be made. In theory, n rounds of lithography is able to make at least n levels in the

structure; (9) The wafer with structured SiO_2 is now etched in a deep Si Reactive Ion Etcher (RIE) to vertically scale the SiO_2 3D pattern by the Si:SiO_2 selectivity (which is around 200 – 300 for our case) and formed in the silicon wafer underneath. Finally, we are left with an n level, high aspect ratio structure, deep structure in Si; (10) In contrast to the multi-level structure in (9), this is a single-level structure shown for comparison

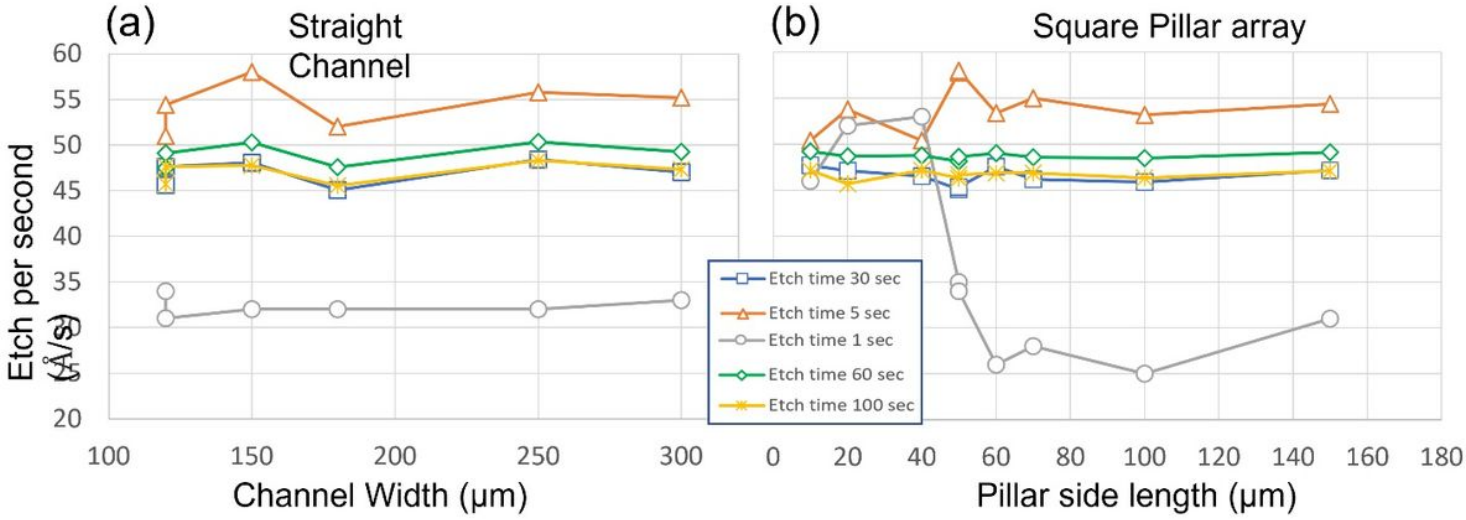

Figure 3

To establish repeatability and standardizability of our method, precise characterization of the oxide etch rate is imperative. Resolution of was found to be ~ 5 nm. For the characterization mask consisting of straight channels and square pillar arrays, the etch per second in Å/s has been plotted as a function of the feature type and dimensions for the specific tools and processes used in our study. The raw data used to plot these curves can be found in the Supplementary Information. The etch rate values will change depending on the recipe and process condition. However, the important observation is the fact that no Aspect Ratio Dependent Etching (ARDE) in SiO_2 is noticed (the maximum variation in etch per second in different geometries was found to be ~ 1 nm/s) showing a consistent etch per second value for different feature dimension and loading conditions. Etch per second was seen to be more influenced by total etch time, especially when total etch time is low (< 5 secs) – this is the result of unpredictable plasma distribution when etch time is only a few seconds. At higher etch times (30s, 60s, 100s) the etch per second showed less variation and were closer to each other (45 – 50 Å/s) indicating good process control, repeatability, and reliability.

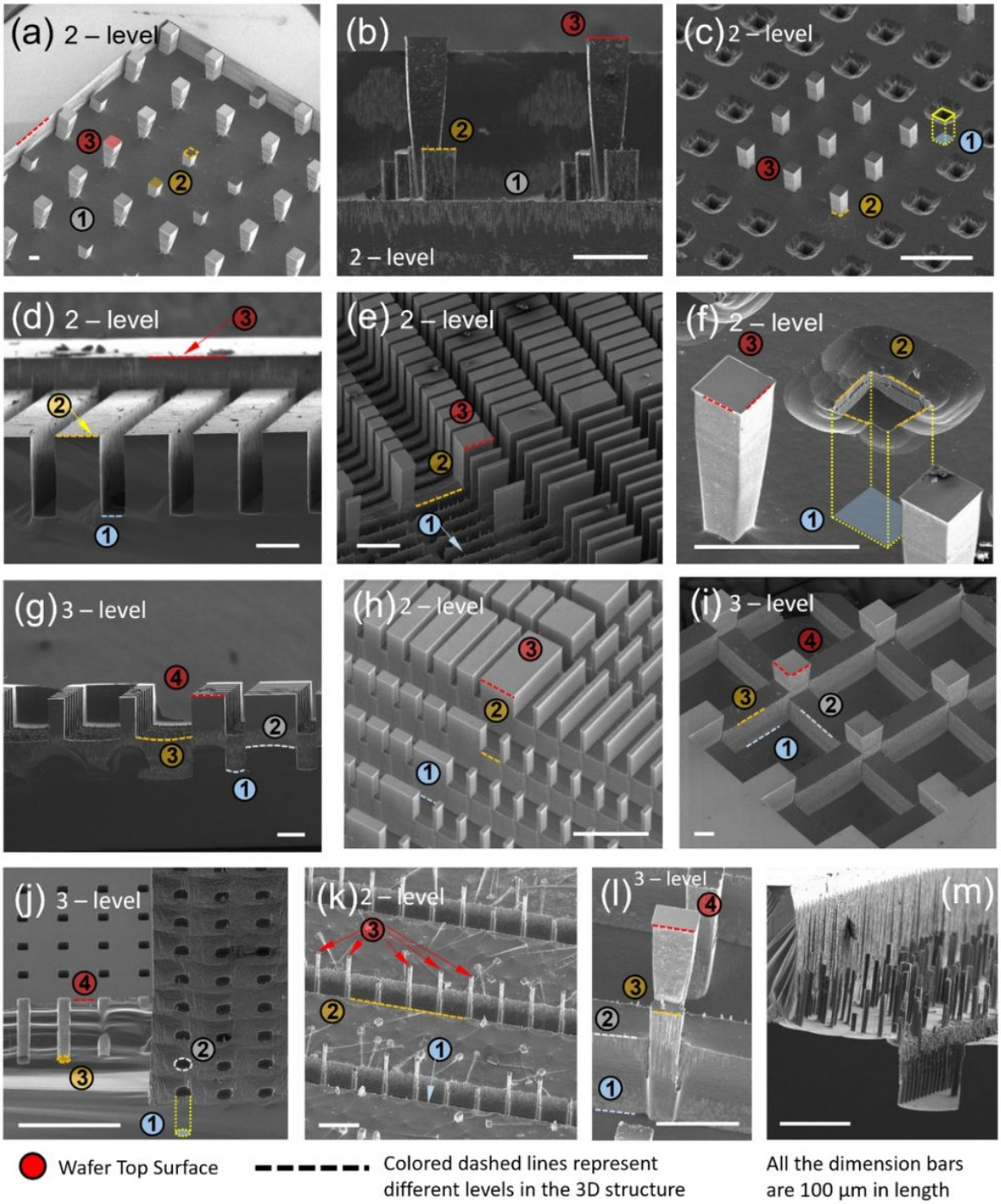

Figure 4

(a) Multi-level pin fin structures (isometric view), these types of structures cannot be made via conventional chip stacking or double sided etching techniques; (b) (Side view) multi-level pin fin array; (c) Pin fins and pin holes; (d) straight microchannels offset from wafer surface (the ability to make microstructure slightly offset from surface has immense potential to ease bonding, integration and packaging different components together especially for extreme heat flux cooling applications); (e) Serrated fin structures of different aspect ratios and spacing; (f) Zoomed image of pin-fin pin hole sample; (g) (Side view) Serrated Fin structure showing 4 distinct levels; (h) Isometric view of 2-level serrated fin; (i) Overlapping mask designs used to make 3-level serrated fins; (j) 3-level Channels with pin-holes made by overlapping 2 mask designs. These kind of smaller pin-fin or pin-hole type structures distributed on a larger underlying meso structure is an easy and viable way to improve thermal

performance of the active heat transfer zone in coolers; k) Pin fins protruding from channel base taller than the channel sidewall height (some fins got broken during wafer dicing); (l) 3-level “Chair” design made by overlapping square pattern mask designs on the side of channels; (m) Initial concept of pin fin array patterned on two-level channels suggests to our ability to make well-ordered surface enhanced structures as well.

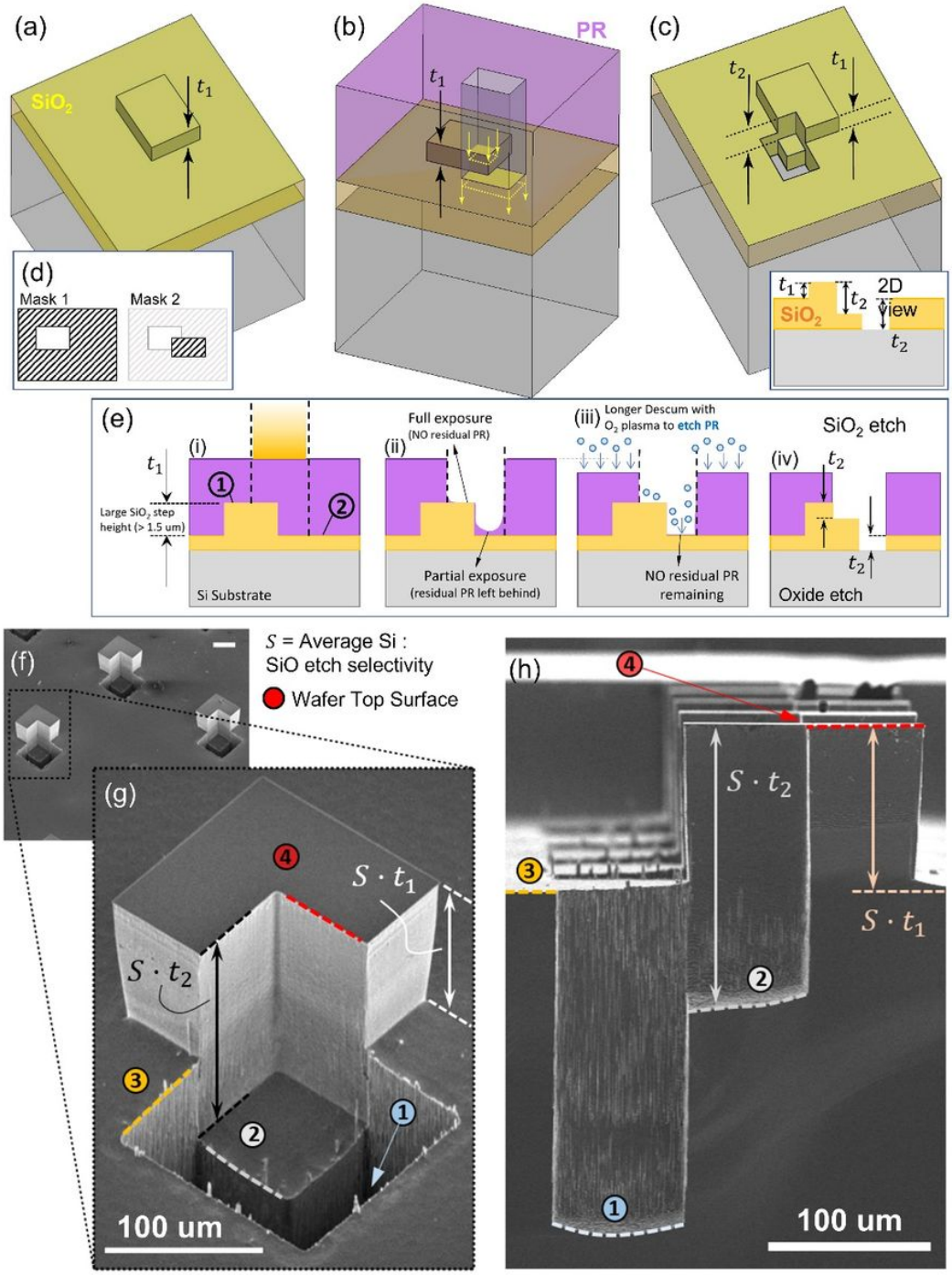

Figure 5

(a) First mask design (as shown in (d)) is exposed and SiO2 is etched by t_1 amount; (b) Second design overlaps partially on the step made in step (a) and (c) SiO2 etch is performed to obtain a 3-level 3D feature on the SiO2. A 2D counterpart of this 3-levels structure is shown in (e - iv) (d) The two masks for two rounds of (litho + SiO2 etch) are shown, image on the right shows how the masks overlap. (e) It has been verified that steps up to 1 μm in SiO2 do

not affect the exposure process. In case the step height is > 1.5 μm, there could arise differences in exposure quality between the two levels of SiO_2, 1 and 2 . In this situation the lower steps might be underexposed, with PR being left behind – a longer downstream descumming step (> 2 mins) fixes the issue, by removing all of this residual PR. (f) After DRIE, the structure is scaled vertically and transferred to the underlying Si, and the new 3-level pin-fin-hole combination arrays are shown; (g) zoomed view of the 3D structure; (h) side cross-sectional view. The numbers represent the different levels.

Supplementary Files

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