Reconfigurable Negative Bit Line Collapsed Supply Write Assist for 9T-ST SRAM Cell

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Research Article

Keywords: WM, WSNM, WTP, RNBLCS, CCS

Posted Date: April 11th, 2022

DOI: https://doi.org/10.21203/rs.3.rs-1516784/v1

Abstract

This paper presents a Reconfigurable Negative Bit Line Collapsed Supply (RNBLCS) write driver circuit for the 9T Schmitt Trigger-based SRAM Cell (9T-ST), significantly improving write performance for real-time memory applications. In deep sub-micron technology, increasing device parameter deviations significantly reduce SRAM cells' write-ability. The proposed RNBLCS write-assist driver for 9T-ST SRAM cell has 0.84×, 0.48×, 0.27× optimized write access delay and 1.05×, 1.08×, 1.19× improvement in Write Static Noise Margin (WSNM), 1.05×, 1.13×, and 1.39× improvement in Write Margin (WM), 0.96×, 0.89× and 0.72× minimum Write Trip-Point (WTP) from Transient-Negative Bit Line (Tran-NBL), capacitive Charge Sharing (CCS), and conventional write circuits respectively. The proposed RNBLCS is functionally verified using a Synopsys Custom compiler with a 16nm BSIM4 model card for bulk CMOS.

I. Introduction

For many years, energy-efficient and high-speed memory design have been a significant research focus in academia and industry. High energy efficiency and speed are required in a wide range of applications, including portable electronics and on-chip memories [1]–[4].

For example, capacitive charge sharing collapsed supply is a write-assist driver technique for lowering energy usage by altering the system operating voltage across a wide range based on performance requirements [5]. The SRAM cell is tested using cell characteristics and stability analysis in several operation modes. Using MC simulation, the properties of ST-inverters are discovered, and the importance of constructing durable memory cells is observed. A stability analysis reveals the constraints of a stable 10T-ST SRAM cell. As a result, this research offers a 9T-ST SRAM cell structure derived from the 10T-ST SRAM cell. This adjustment has improved read-stability and hold-stability by 13% and 15%, respectively. Over a temperature shift of more than 40^{o}C, read stability for 6T SRAM, and 10T SRAM deviates by 93% and 42%, respectively. The primary finding of the heat analysis for the proposed SRAM cell is that it can retain read stability while only exhibiting a 5% RSNM variance [6]. The write-ability improvement of memory cells is a significant concern in this paper, besides read and hold stability, which was improved by proper cell design. Write-ability can be enhanced by modifying the memory architecture with assist circuits [5], [7], [16]–[18], [8]–[15].

Predictive Technology Model (PTM) has released the latest multi-gate transistor model (PTM-MG). This RNBLCS is developed on a multi-gate device-specific model (BSIM-CMG) [19].

This paper is written in the following manner: Section II describes the Capacitive Charge Sharing (CCS) [5] and Tran-NBL circuits that assist [16] in increasing the write-ability. The proposed write-assist driver circuit design for the 9T-ST SRAM cell is presented in Section III. Section IV contains a statistical simulation-based analysis of the proposed work. Finally, section V concludes the paper by providing a summary.

Ii. Conventional Write-assist Circuits To Improve Write-ability

A. Capacitive Charge Sharing Write-assist Circuit (CCS)

As shown in Fig. 1(a), the Capacitive Charge Sharing write-assist circuit is designed to improve write-ability. Figure 1(b) shows that memory cells have enough cell stability at high voltage levels to hold cell data correctly when V_{CS} is kept at V_{DD} in Phase-1 for inactive WE. After WE assertion, P1 is turned off, and N1 is slightly conducted, so the charge across the source capacitor (C_S) is discharged to another capacitor (C_{BOOST}) through N1, as shown in Fig. 1(c); this collapsed voltage (V_{CS} fromV_{DD} to V_{COL}) can drive and reduce the memory cell's hold-stability as shown in Fig. 2.

As the supply voltage of the cell (V_{CS}) drops, cell stability degrades, as indicated by the "HSNM" stability parameter [5], [8]. For example, when V_{CS} is scaled down, the HSNM of the cell degrades, as shown in Fig. 2.

As shown in Fig. 3, the Q-node of the memory cell is tripped at a swept WL voltage range of 0.46V to 0.61V for a supply voltage (V_{DD}) of 1V. The mean Write Trip Points (WTP) levels are decreased with scaling the supply voltage, which indicates scaling the supply voltage makes the cell unstable and quickly accepts the changes in BIT and BITB lines. So the Q-node of a memory cell is tripped at a sweep WL voltage range of 0.33V to 0.39V for a scaled supply voltage (V_{DD}) of 0.6V. So Write-ability is improved by scaling the SRAM cell's supply voltage, which is done by the CCS write-assist circuit [5], [8], [20], [21].

The WTP voltage occurrence levels are plotted using Monte Carlo simulation, and it was observed that all strong cell samples with high V_{DD} occurred on the right side (at maximum Trip voltage levels). On the other hand, all weak cell samples with scaled V_{DD} occurred on the left side (at minimum Trip voltage levels), as shown in Fig. 4.

B. Tran-Negative BIT Line (T-NBL) Write-Assist Circuit

Tran-NBL write-assist circuit, shown in Fig. 5(c), can improve the write performance with the help of two charging capacitors C_{RBOOST} and C_{LBOOST}. One end of these capacitors is connected to the BIT line and write word line-B(WWLB) of the 9T SRAM cell, and the opposite end of the capacitors is connected to the control input 'BIT_EN' [11], [12], [16].

Figure 6 depicts the timing diagram for the circuit functioning. In a conventional write operation, the active NSEL signal turns both pass-transistors (N1/P1, N2/P2) 'ON' for the whole duration of the WL pulse and BIT, BITB is connected to ground and V_{DD}. Here, 'NSEL' is used for column selection. The NSEL and BIT EN signals are asserted together with the WL Pulse in Tran-NBL, but they are de-asserted halfway through the WL. The pass transistors (N1/P1 and N2/P2) are turned off, leaving BIT and BITB lines floating at the ground and V_{DD}, respectively. Due to capacitive coupling action via capacitors (C_{LBOOST} and C_{RBOOST}), as shown in Fig. 5(a) and Fig. 5(b), the negative transition of BIT_EN produces the bit-line under-

shoot (BIT or BITB). Because the floating BIT line at the '0' level generates a momentary negative sudden change voltage on the bit-lines (BIT or BITB). The timing diagram for the write-‘0' operation [6] is shown in Fig. 6. The Tran-NBL write driver circuit generates a negative voltage at the bit line to increase the strength of the accessing transistor (M_{AXR}) to improve the write access speed. The strength of the negative bit voltage depends on selecting boost capacitors C_{LBOOST} and C_{RBOOST} as shown in Fig. 6. Small range capacitors need a small silicon area to fabricate. Such a small range boost capacitor (C_{LBOOST}=110fF) can generate a small negative bit voltage of 110mV, observed in Fig. 6 [16]. The transient negative voltage causes a temporary rise in the access transistor's (MAXR) discharging current, making the Q-node voltage (V_Q) pull-down easier. The cross-coupled inverter pairs latch and settle with write data when V_Q falls below the trip-point.

During the write-‘1' operation, the column select control input word line-A (WWLA) remains "0", the driver circuit drives BL to "1", and the word line is enabled. As the WWLB is changed to "0" to disconnect the path from the V_{DD} power source by turning off M_{PDSL}, the Q-node storing data "0" is power-gated, which helps raise the voltage at Q-node.

Table I. Minimizing trip voltage levels using column select control voltage V_{WWLB}, which are observed from the voltage transfer characteristics of ST Inverter

V_{WWLB}	Feedback Strength	Strength of M_{FBR}	VTP
V_{DD}	Strong	Very weak	593mV
Ground	Very Weak	Strong	414mV
-ve	Zero	Very Strong	353mV

Furthermore, the ST inverter's trip voltage is lower than that of a conventional inverter because the ST inverter's feedback mechanism is decreased with negative VWLB voltage, as shown in Table I. The turned-on M_{AXR} drives the power-gated Q-node to "1", and the ST inverter is switched. After the data in Q_b-node is flipped, the column selects WWLB is reset to '1' [22].

Iii. Proposed Write-assist Circuit Design For 9t-st Sram Cell

A Reconfigurable Negative Bit Line Collapsed Supply (RNBLCS) write-assist circuit is proposed to improve the write performance (i.e., improve the write accessing speed, Write-ability) as shown in Fig. 7.

The write operation is carried out by the proposed assist circuit in three phases, (a) No-Assist phase. (b) Charge sharing or supply collapse phase. (c) Negative BIT line enable phase.

In the No-Assist phase, P1 is turned ON using control signals (Colgen, Boost1, Boost2). So conducting P1 can fully charge the source capacitor (Cs) to the maximum level of $V_{DD,}$ as shown in Fig. 10(a). Next, when the write mode of operation is initiated upon active write enable, the capacitive charge sharing

process is started from the source capacitor to the boost capacitor (C_{BOOST}) through conducting P2 in the second phase. So boost capacitor left plate (C_{BOOSTL}) is accumulated with a positive charge, as shown in Fig. 10(b). Finally, in the Negative BIT line enable phase as a third phase, the boost capacitor left plate is grounded by conducting N1suddenly by the boost2 signal. The capacitor does not allow sudden changes in voltage, so the right plate of the boost capacitor generates a negative voltage peak, which is directly transferred to the BIT/BITB line through N2/N3, as shown in Fig. 10(c).

The Reconfigurable Negative Bit Line Collapsed Supply (RNBLCS) write-assist circuit pulls supply voltage down (V_{DD} to V_{COL}) to reduce the stability of the memory cell. It also generates negative BIT/BITB line voltage to increase the strength of the access transistor (MAXR/MAXL). As a result, RNBLCS can outperform CCS and Tran-NBL assist circuits in terms of write-ability.

As shown in Fig. 9 (a), the boost capacitor is not adequately selected, so a write' 0' failure is observed. Write failure is overcome in the second case with the proper selection of boost capacitors during write '0'.

Iv. Results And Comparisons

A. **Write Accessing Delay**

As shown in Fig. 11, The conventional write driver circuit, existing write-assist circuit and proposed RNBLCS circuit simultaneously perform write-'1' operations to the 9T-ST SRAM cell. After WL is enabled, the write access time is calculated as the time it takes for one of the storage node voltages (initially at '0') to reach 90% of V_{DD} [15]. The maximum write delay for 1000 memory samples is plotted and compared. This comparison write delay of the proposed assist circuit is 0.84×,0.48×, 0.27× times lower than Tran-NBL, CCS, and conventional write operations.

B. **Write Static Noise Margin (WSNM)**

WSNM indicates the write-ability of the cell, which is used as a performance metric during write operations. WSNM is calculated through butterfly curves, a combination of read and write voltage transfer curves. The read VTC is a plot of Q_b-node voltage (V_{Qb}) versus Q_b-node voltage (V_{Qb}) with BL, BLB WL are biased at V_{DD}. The write VTC is obtained by sweeping the voltage at the storage Q-node with BL and WL biassed at $V_{DD,}$ and BLB biassed at the ground while plotting the node voltage at Q_b-node [2] [23],[4], [17], [23]–[26].

The width of the pull-up transistor is considered a Gaussian distribution function to perform Monte Carlo simulations to observe the effect of Write-ability due to the pull-up ratio (PR) variation. The maximum WSNM for 1000 memory samples is plotted and compared among conventional write driver circuits, existing write-assist circuits, and proposed RNBLCS circuits, as shown in Fig. 12 [14], [27], [28].

C. **Write Margin (WM) and Write Trip-Point-Voltage**

Write margin (WM) is a metric used to characterize Write-ability, and it can be measured using the word-line sweep method [15]. Data is applied to the bit lines to measure WM, and then the word line (WL) is swept from 0V to V_{DD} to simulate an actual write process. The voltage differential between V_{DD} and WL when memory nodes (Q and Q_b) update their data with write data during the write operation is known as the WM [29][5], [9], [15], [18], [30]–[32].

WM occurrence levels are plotted using a Monte Carlo simulation in Fig. 16. The observation from the plot is that all RNBLCS cell samples occurred on the right side (at maximum WM levels), while other cell samples with other assist techniques occurred on the left side (at minimum WM). The proposed assist circuit offers 1.05× and 1.13× higher write margins than Tran-NBL and CCS, respectively, which is evident from the mean of WM calculation in Fig. 13.

WTP is identified as the sweep voltage level of WL at which memory nodes (Q and Q_b) update their data with write data during the write operation. Figure 14 illustrates the Write Trip Point (WTP) of SRAM 10K cell samples with different write driver circuits under MC simulation and observed as the proposed Assist circuit offers 0.96× and 0.89× smaller write Trip voltage (WTP) from Tran-NBL and CCS.

D. **Write Power**

Average Write power (using write-‘0' and write-‘1' power) is calculated for write-assist circuits, and comparison results are shown in Fig. 15 [24]. The proposed 9T-ST SRAM with proposed RNBLCS, 20nm HP model, has 24%,13%, and 43% and 16nm HP model has 29%, 9%, and 36% Power saving than Tran-NBL, CCS, and conventional write circuits. Cell leakage during write operations is reduced because of the collapsed power supply in CCS and the proposed RNBLCS. The ST-based SRAM cell's characteristics, which feature dual-threshold, save write power even more.

V. Conclusion

The 9T SRAM cell configuration eliminates write half-select failures and read failures for robust subthreshold operation; write-ability improvement constraints are demonstrated in this paper. A significant improvement in write performance is observed with the 9T-ST SRAM Cell with Reconfigurable Negative Bit Line Collapsed Supply

Write-assist Technique. The proposed ST bit cell achieves a higher read SNM (1.56×) than the conventional 6T cell (V_{DD}=400mV). In addition, the proposed 'RNBLCS' completes a higher Write Margin (1.1×), WSNM (1.19×), and lower write delay(0.27×) compared to the convention write driver circuit. The proposed 'RNBLCS' also achieves lower write power (0.57× for 20nm) (0.64× for 16nm).

Declarations

Data Availability

The datasets generated during and analyzed during the current study are available from the corresponding author on reasonable request

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Figures

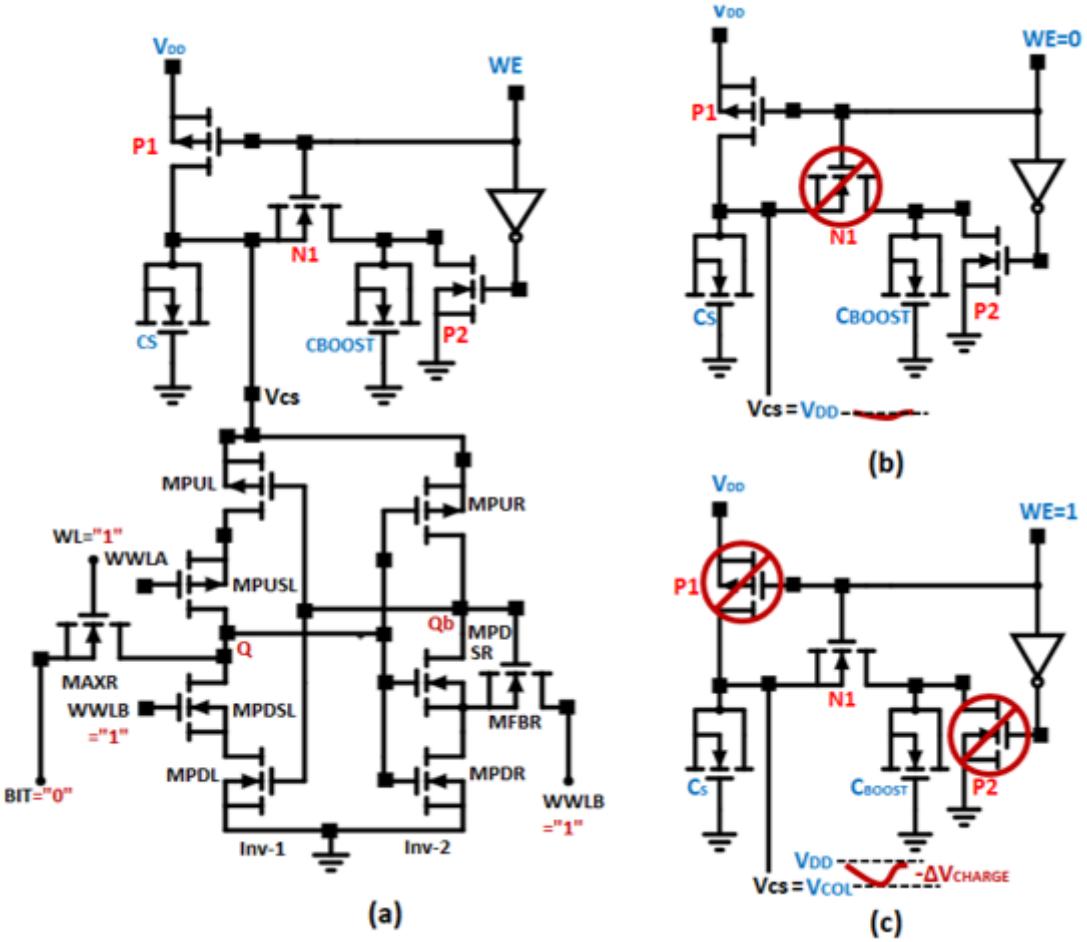

Figure 1

(a). CCS Write-Assist Circuit for fast write accessing. (b). Cell supply voltage in phase-1, when the write operation is not initiated. (C). Cell supply voltage down due to charge sharing in phase-2 when the writing process is initiated

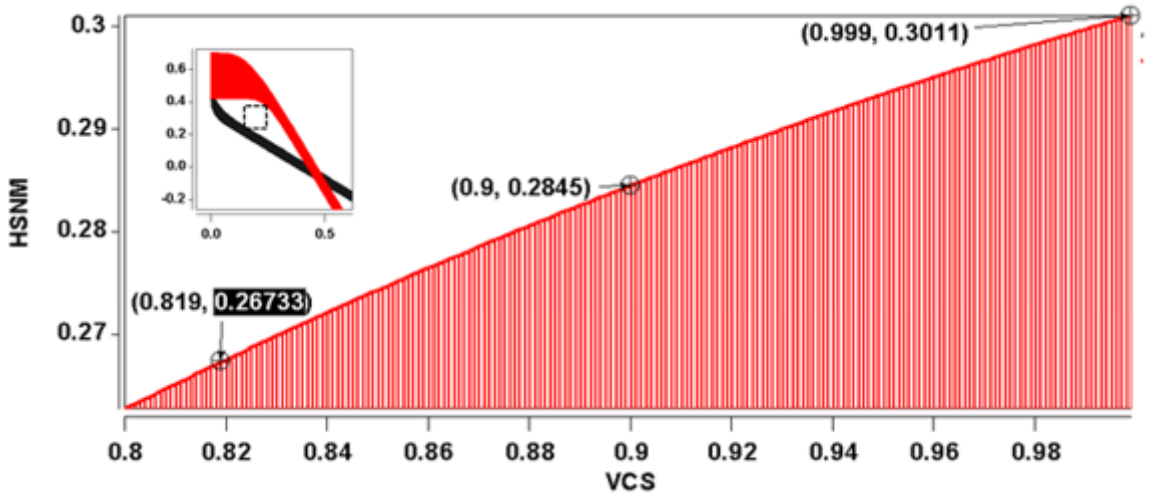

Figure 2

The plot of deteriorating hold stability for scaling the supply voltage (Vcs)

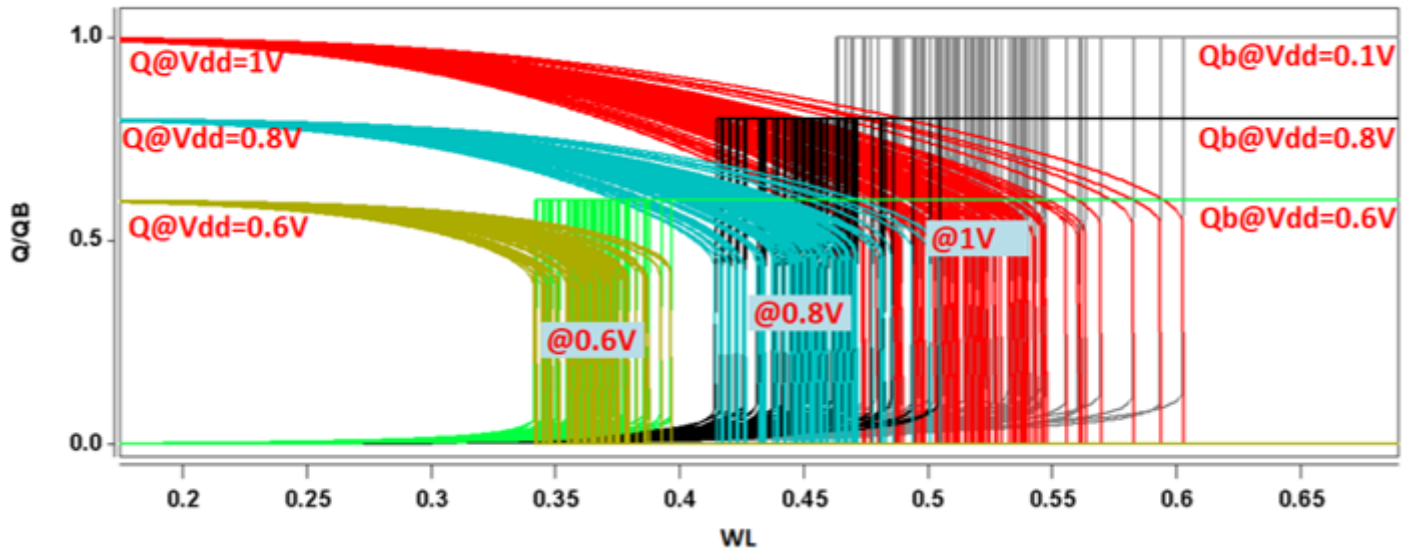

Figure 3

Write-0 into Q-node at VTP levels for different V_{CS}

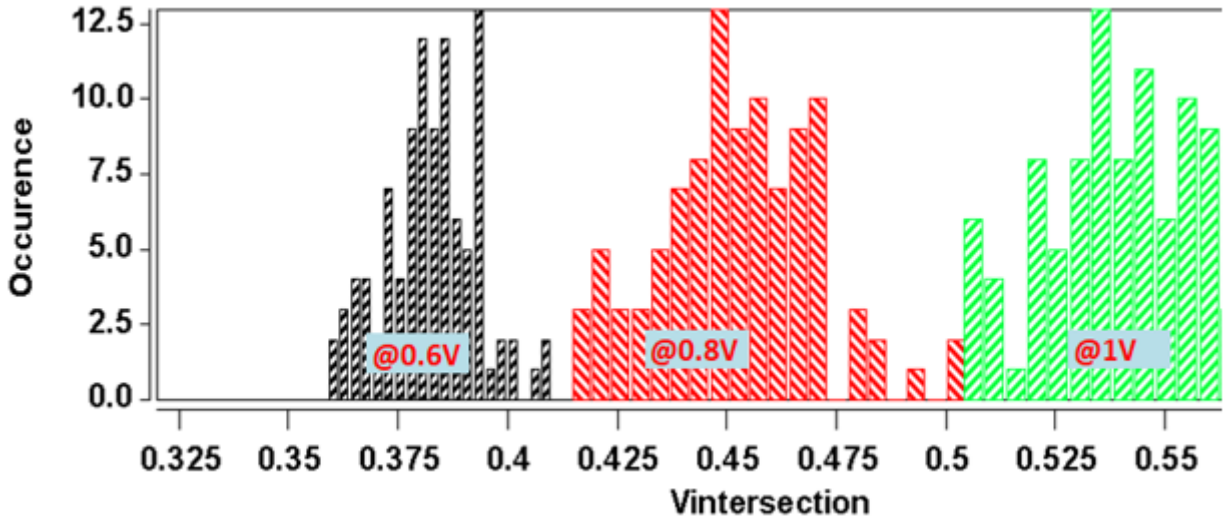

Figure 4

Write Trip Point levels occurrence for different supply voltages.

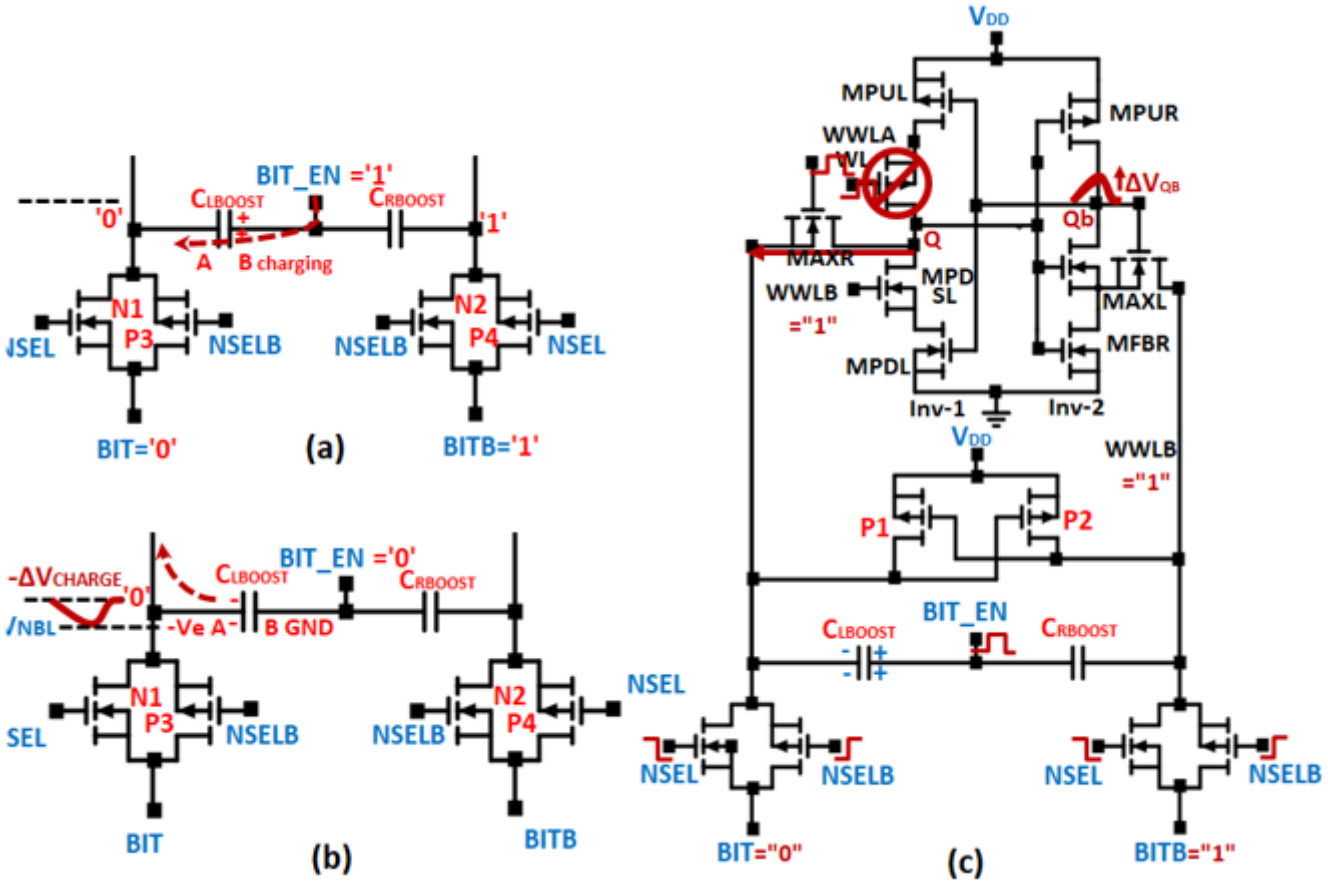

Figure 5

(a).capacitor charging mode through active BIT_EN. (b). Negative BIT enable mode upon inactive BIT_EN. (c)Tran-NBL write driver circuit for fast write accessing (Write-0).

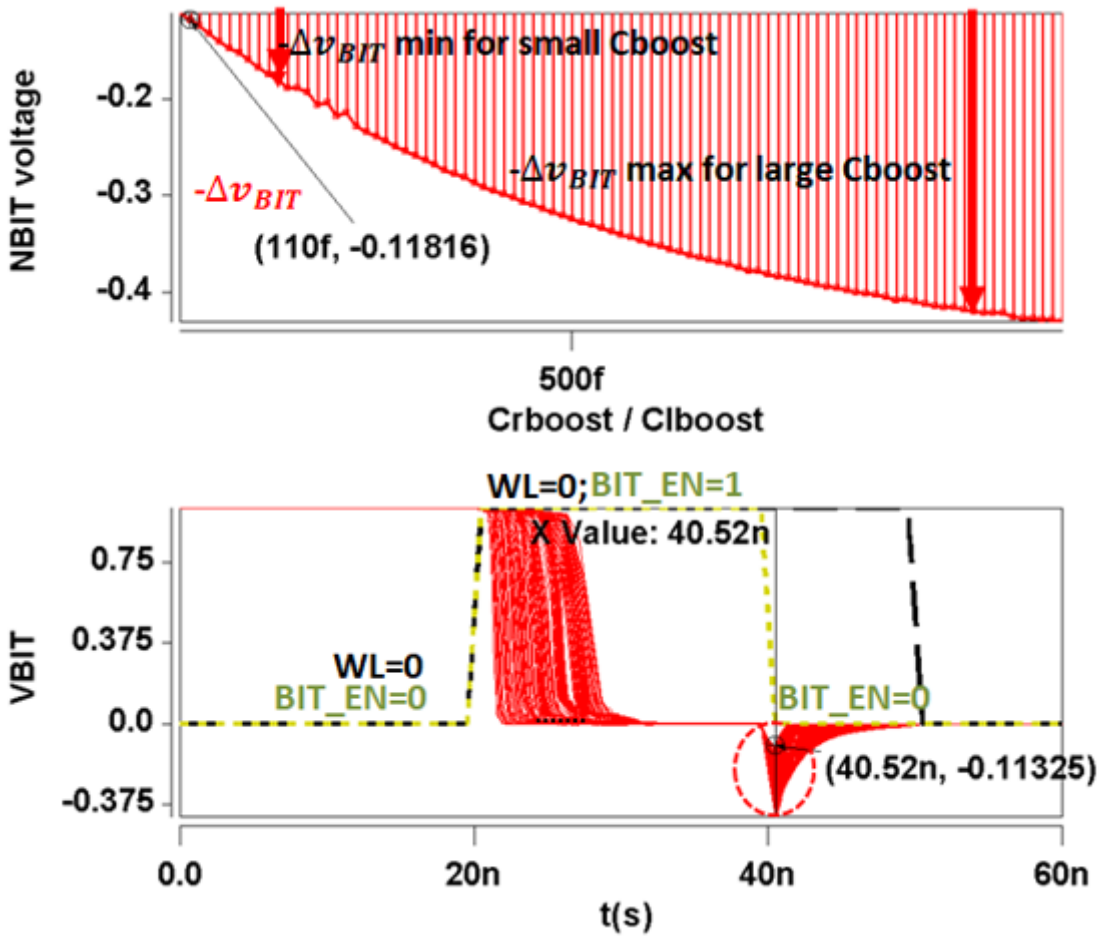

Figure 6

The timing diagram for the circuit operation of generating a Negative BIT line for the change of WL, BIT_EN

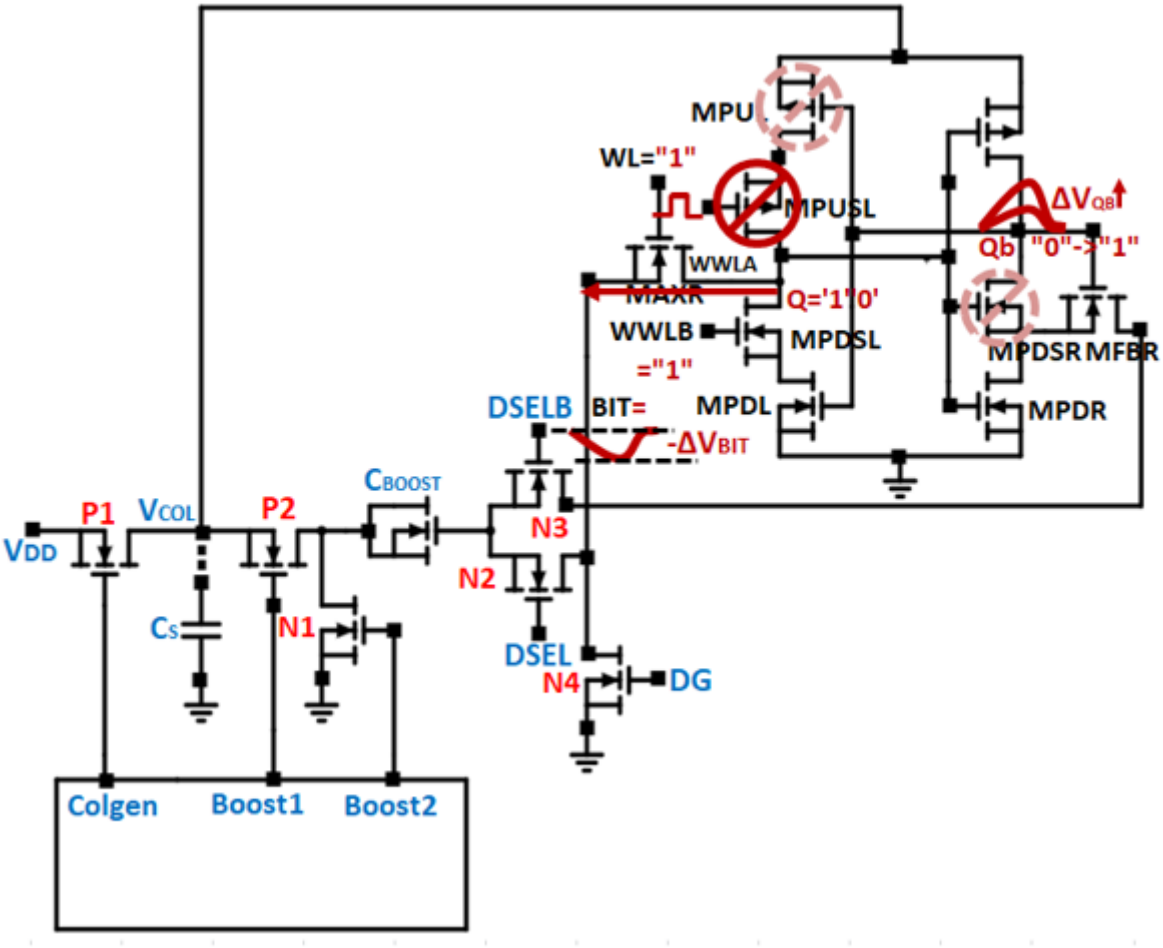

Figure 7

9T-ST SRAM cell with a proposed Reconfigurable Negative Bit Line Collapsed Supply (RNBLCS) write-assist circuit.

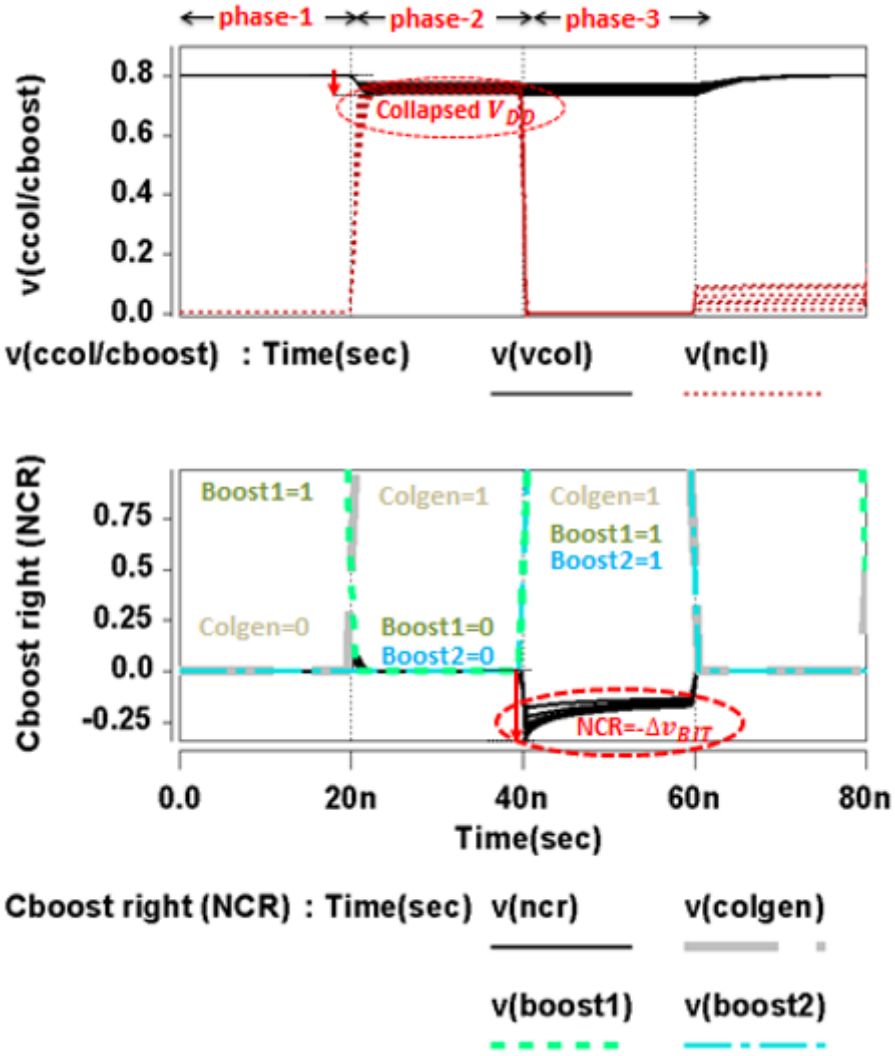

Figure 8

Negative BIT line voltage and collapsed supply voltage generation using 3 phase operation by proposed RNBLCS write-assist Scheme

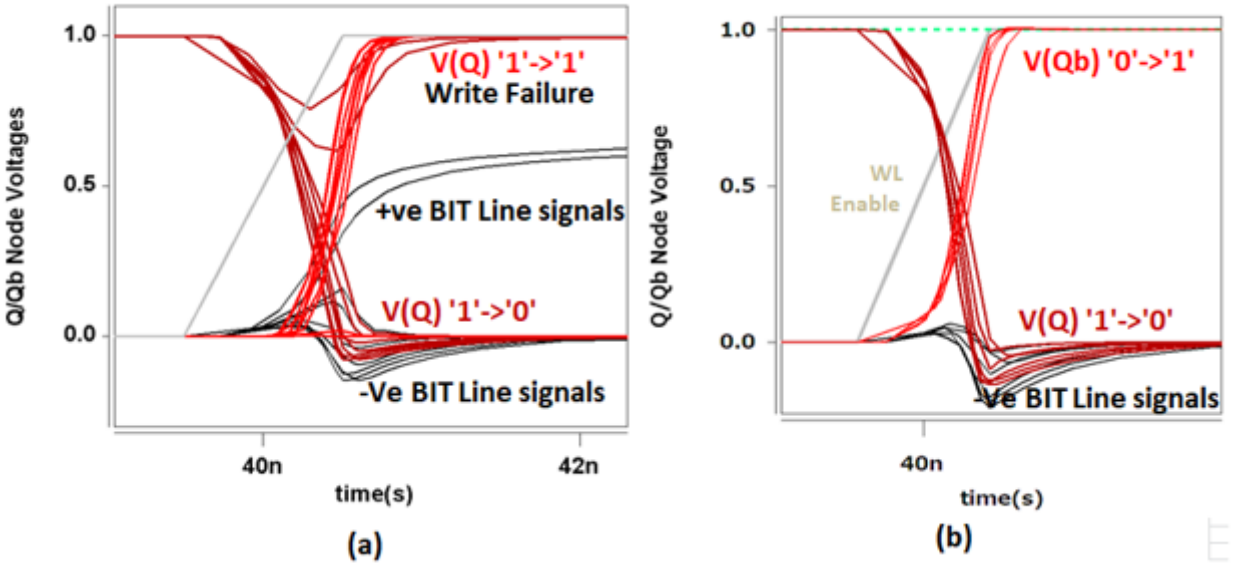

Figure 9

(a). Occurring write failure for assist circuit design with minimum Cboost selection (<23fF) (a). Proper assist circuit design with no write failure.

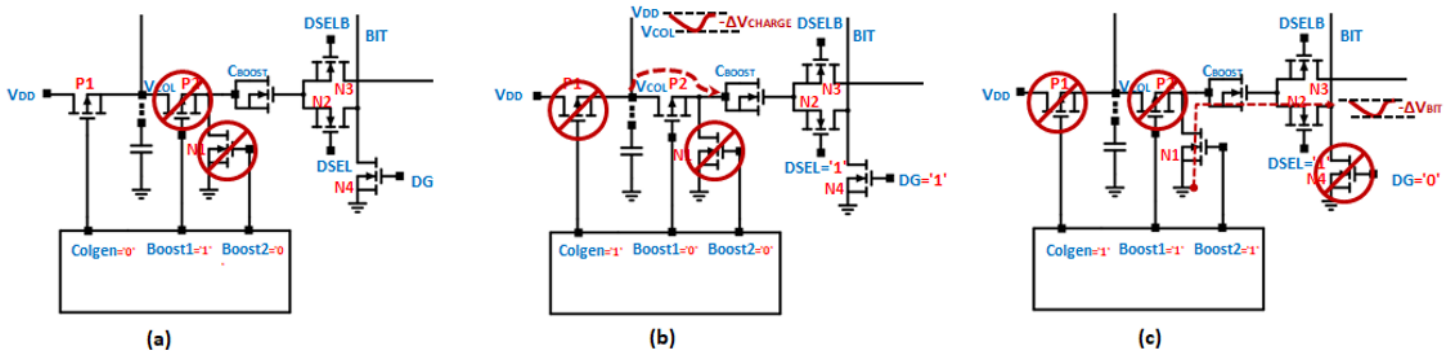

Figure 10

(a) Assist beginning phase. (b) Charge sharing or supply collapse phase. (c) A negative BIT line enable phase

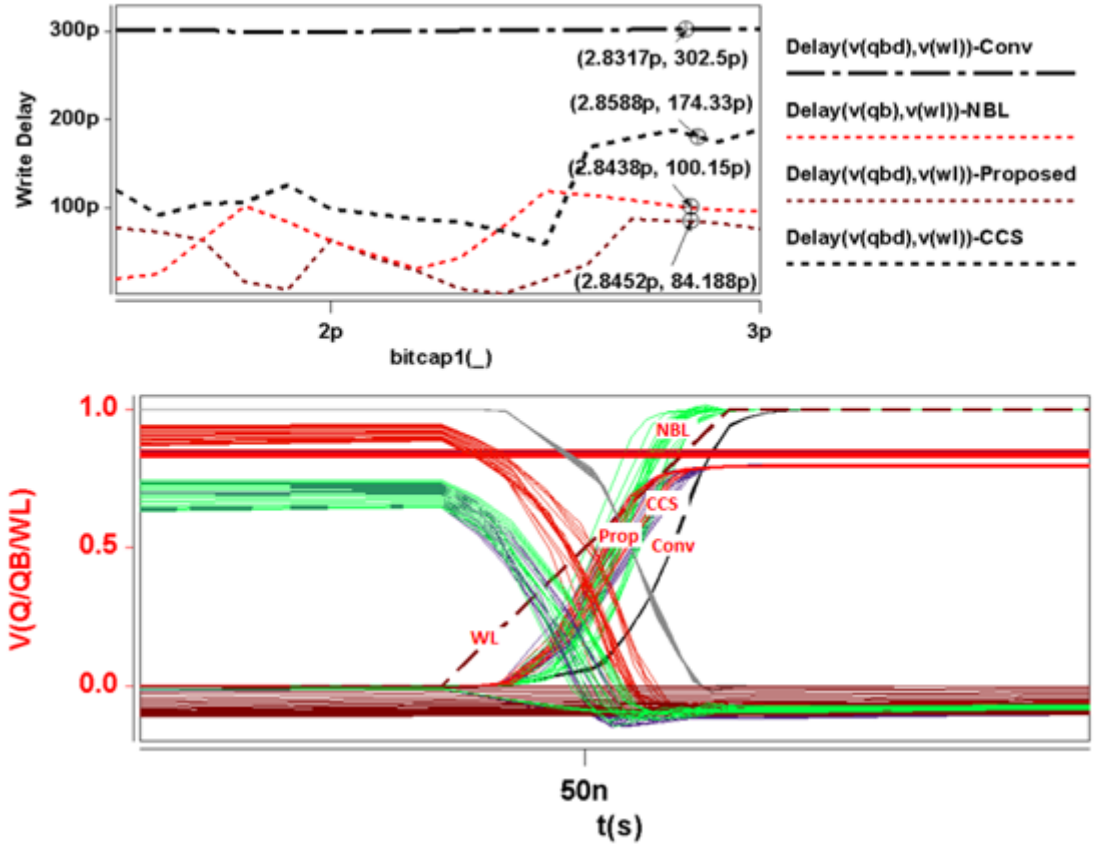

Figure 11

Write Accessing Delay calculation for Cboost capacitive sweep.

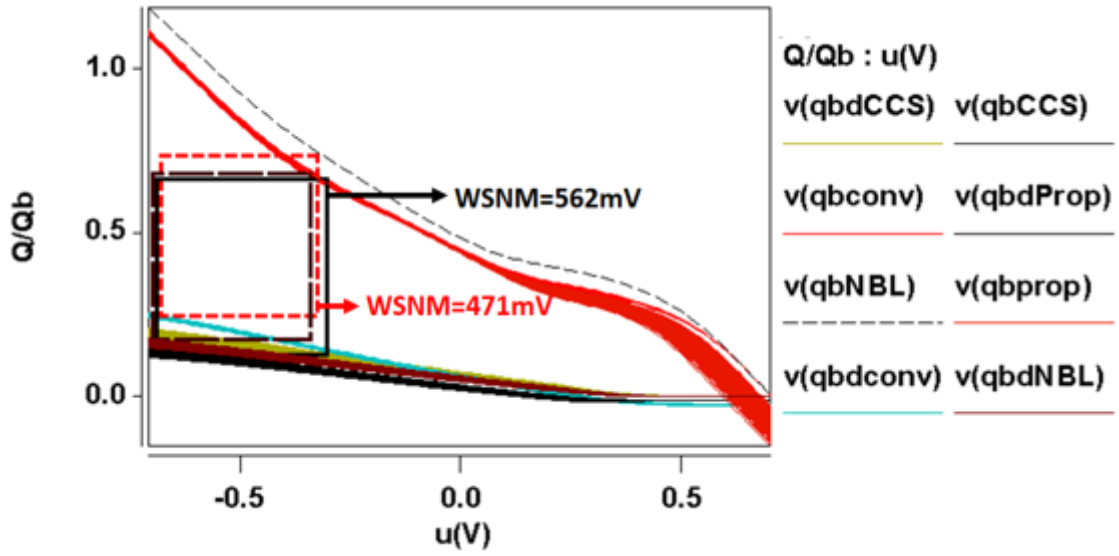

Figure 12

WSNM calculation through butterfly curves (DC transfer characteristics)

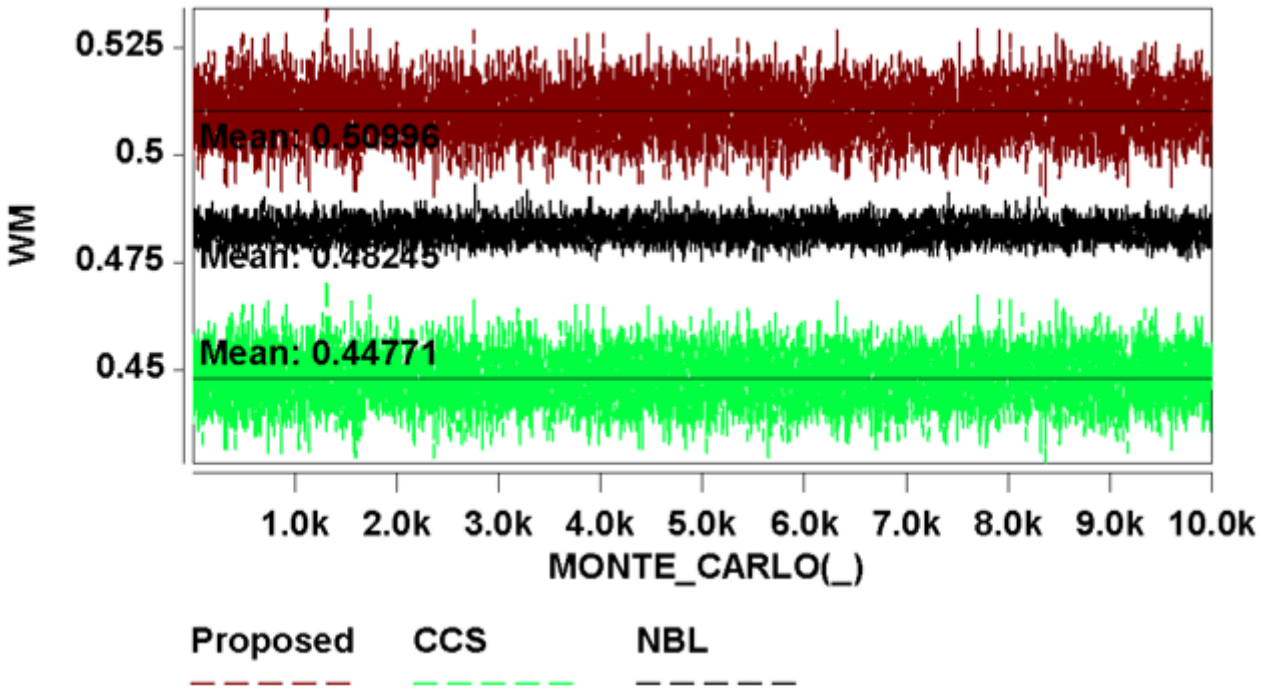

Figure 13

Under MC simulation, the WM of 10k samples of SRAM cells with different write driver circuits

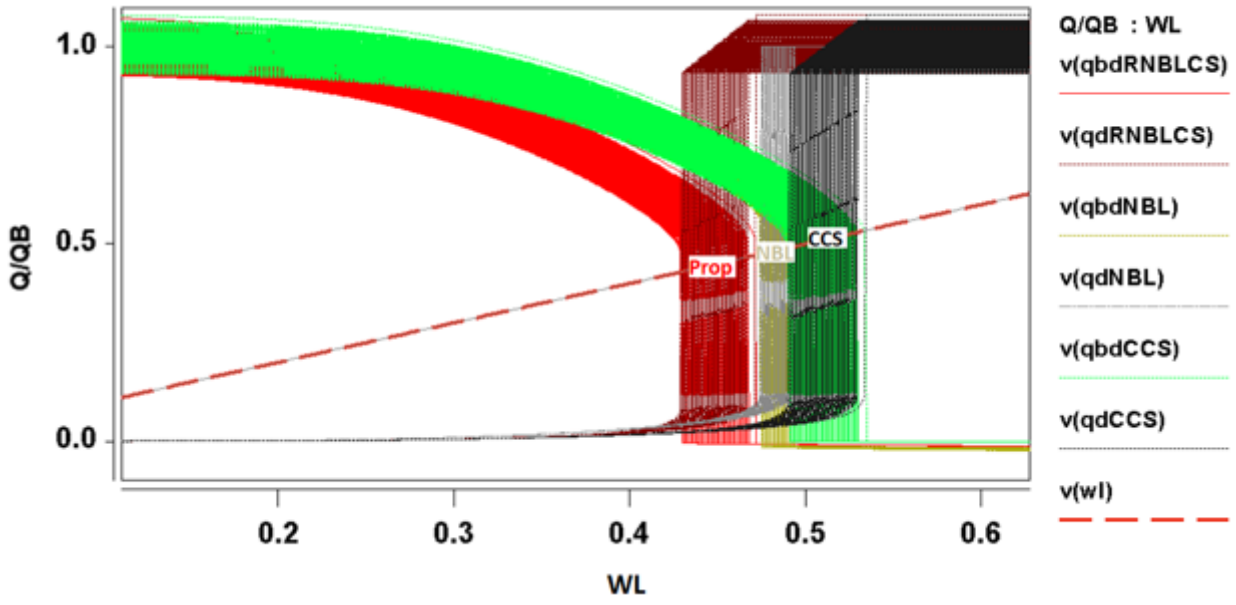

Figure 14

Write Trip Point (WTP) of 10000 samples of SRAM cells with different write driver circuits under MC simulation

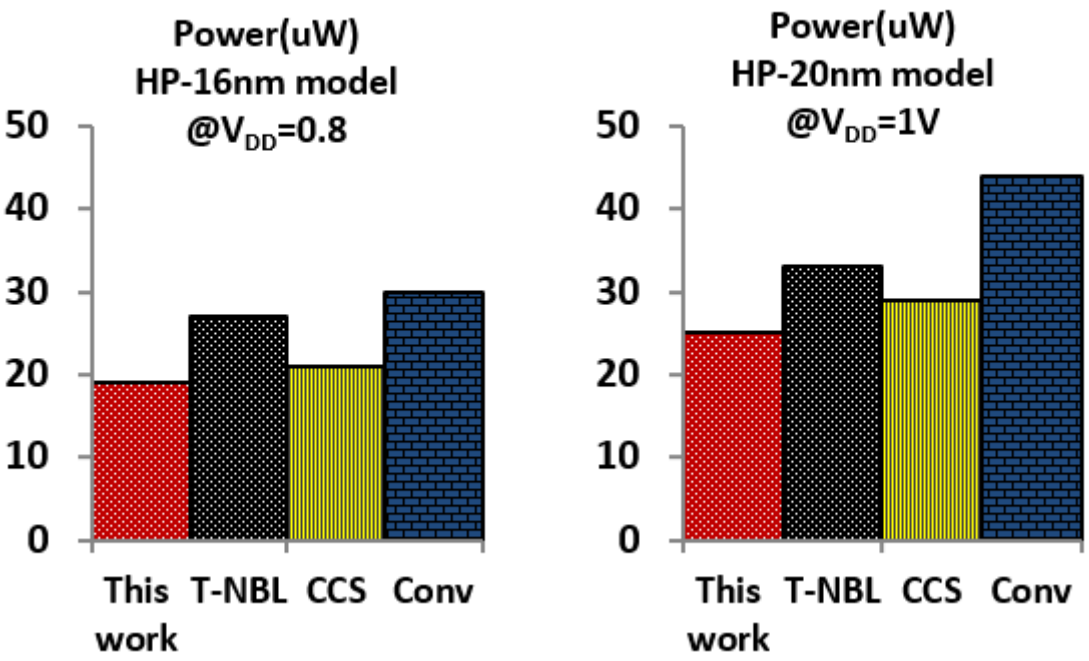

Figure 15

comparison of Write Power among assist circuits during a write operation

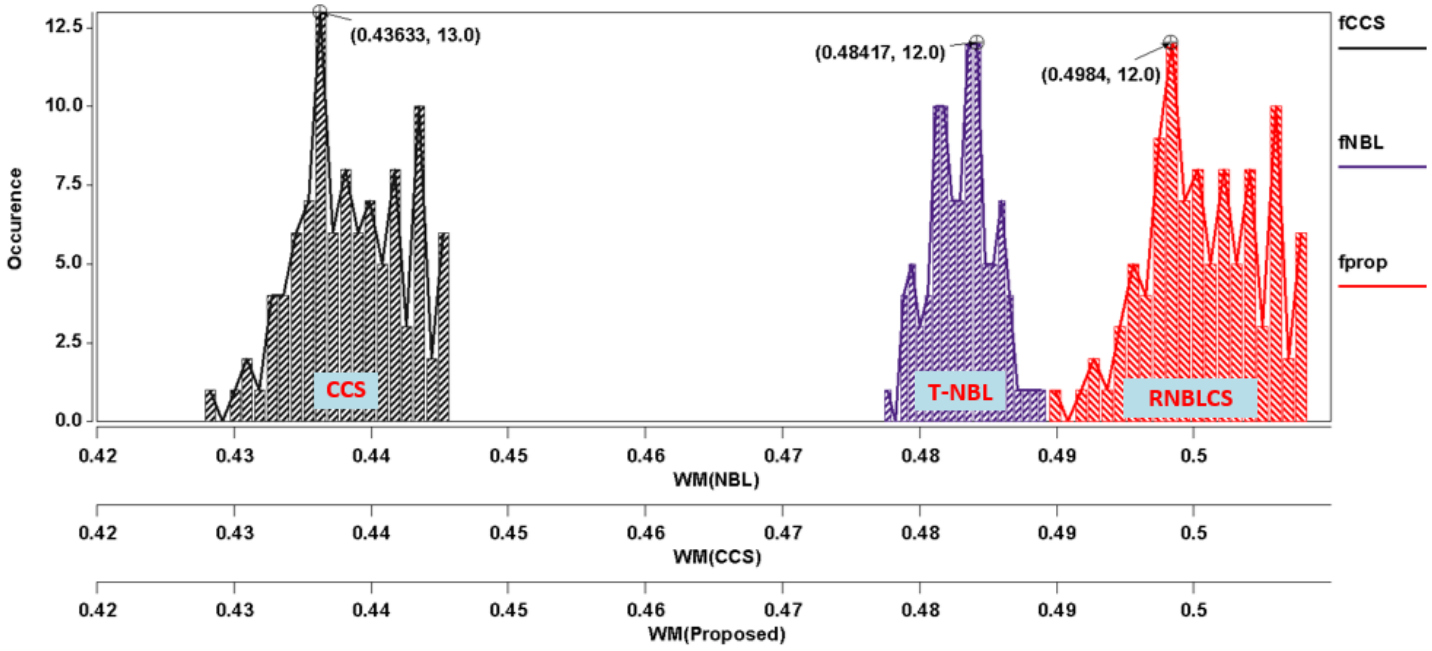

Figure 16

Histogram of 10K-point monte Carlo simulation for WM and comparison among assist schemes for 9T-ST SRAM Cell