A Capacitively Coupled Digital Isolator with CMTI of 162 kV/μs and Data Rate of 230 Mbps

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Abstract

This paper presents a small-size on-chip capacitively coupled digital isolator with superior Common Mode Transient Immunity (CMTI) and high operational speed performances. It employs a gate-cross-coupled common gate pre-amplifier with an active zero load and a high-pass filter before the pre-amplifier. By applying the proposed technique, the high-frequency gain retains to high value, while the low-frequency gain is greatly attenuated. The high-pass filter, which is designed based on the technology structure of the on-chip isolation capacitance, is applied to further cancel the influence of Common Mode Transient (CMT) and aid in the transmission of high-frequency signal. Furthermore, differential On-Off Keying (OOK) modulation is adopted to eliminate CMT noise. For the purpose of increasing the operation speed performances, the work utilizes the Voltage-Current high-speed comparator with fast feed-forward path as Schmitt trigger and level shift, and employs the envelop-comparator, integrator and filter as demodulator. Thus, it significantly reduces the propagation delay and speeds up the data rate. As a result, both high CMTI and operational speed performances are achieved simultaneously. Fabricated in a 0.18 μm isolated CMOS technology, the area of the isolation element, *i.e.*, the capacitor is 2×10^4 μm^2. The measurement results of a test chip are an over 162 kV/μs CMTI, a 230 Mbps data rate, a 6 ns propagation delay, a 1.5 mA dynamic current and 14 kV isolation breakdown voltage. The characteristics are superior to those of conventional digital isolators.

I. Introduction

Electrical isolators such as digital isolators are widely employed in electric vehicles, industrial automation, solar inverters and other applications that require the isolation of high-voltage and low-voltage areas [1-6]. Digital isolators with exceptional Common Mode Transient Immunity (CMTI), high operational speed performances, low power consumption and robust stability in the most noisy harsh environment are becoming increasingly significant. It means that the signal must be precisely transmitted while remaining immune to very quick Common Mode Transient (CMT). Furthermore, the isolator should have a low propagation delay and high-speed data rata under the condition of a low current power consumption. In addition, to safeguard the internal circuit, the isolation barrier must be able to withstand high V_{PK} surges.

In comparison to optocoupler isolators, transformer isolators [1, 2, 4, 7-17] and capacitive isolators [5, 6, 8-23] are the two types of usual isolation architectures because of their advantages of smaller size, faster speed, lower power consumption, and better CMTI.

Fig. 1 shows a polyimide-based digital isolator using on-chip inductor as transformer and OOK architecture in [1]. In which, the On-Off Keying (OOK) transmitter (TX) directly resonates with the transformer to generate a high frequency carrier signal. For high CMTI, the TX is designed based on the negative-*Gm* oscillator, which can contribute more *gm* to sustain the oscillation during the CMT event. Moreover, in front of the RX, an AC-coupled bias network is used to attenuate the CMT noise without impacting the carrier signal. Therefore, [1] can achieve 200 kV/μs CMTI. However, the data rate is

unavoidable to decrease due to the building time of the oscillator and comparing time contributed by the AC-coupled bias network. In addition, the diameter of micro-transformer is usually larger than 250 μm, occupying too much area and even need another die to put it [4]. For solving the problem of large occupied area of the transformer, [2] presents a SiO_2-based digital isolator using smaller transformers and pulse generation and detection scheme. However, with a transformer of 230 μm diameter, it requires a high-gain receivers to compensate for poor gain. Therefore, it has developed a GHz-band signal generation and detection technique with a 5 V CMOS technology, unavoidably, which degrades the CMT and noise immunity critical for isolators. In addition, pulse modulation, which is sensitive to signal edge, has extremely low static power consumption and high data rate, however, its anti-interference ability is inferior than OOK modulation. Hence, [2] achieves 1.6 mA power consumption and 250 Mbps data rate, however, but only provides 35 kV/μs CMTI due to the small transformer and the limited of pulse modulation. For both minimal isolation element area and high CMTI, [5] presents a SiO_2 based digital isolator using capacitors and OOK architecture. Using isolation capacitance, its isolation element area is 3.00×10^4 μm^2, which is about 1/5 that of traditional micro-transformer. However, capacitive isolators are limited to CMTI of 100 kV/μs even with the OOK data architecture [1, 5].

There is a trade-off between the area of isolation element and the accurate transmission with high-speed data rate when a fast CMT surges.

In this work, a SiO_2-based capacitively coupled digital isolator using OOK architecture with an active zero load pre-amplifier and a high-pass filter is presented that features high CMTI and operational speed performances. The pre-amplifier is designed into a gate-cross-coupled common gate amplifier. By applying the proposed active zero load, the high-frequency gain retains to high value, while the low-frequency gain is greatly attenuated. Besides, the high-pass filter before pre-amplifier, based on the technology structure, is applied to further cancel the influence of CMT. Finally, both high gain for high-frequency carrier signal and low gain for CMT and noise is achieved simultaneously.

For fast transient response, it utilizes the Voltage-Current high-speed comparator with fast feed-forward path as Schmitt trigger and level shift. Besides, it employs the envelop-comparator, integrator and filter as demodulator, which is beneficial to reduce the propagation delay and improve the transmission accuracy with extra boost of the CMTI. Finally, forming the core of the OOK modulation scheme, the oscilalator is designed as a fast start-up ring oscillator with frequency feedback for high accuracy to fulfill the demand of propagation delay and data rate.

This paper is organized as follows. Section II introduces the proposed architecture of the capacitively coupled digital isolator for providing high CMTI from transmitter and receiver. Section III describes the detailed circuit implementation of pre-amplifier, high-pass filter, demodulation and oscillator, all of which are designed for the improvement of CMTI and operational speed performances. Section IV presents the measurement results and finally a conclusion is given.

Ii. Isolator Architecture

Figure 2 shows the proposed SiO_2-based capacitively coupled digital isolator using OOK architecture. Four channels are integrated in a die, where transmitter and receiver are placed in die A and die B, respectively, using the dual-base island package. As Fig. 2 indicating, one channel consists of a transmitter (TX) and a receiver (RX). Each die shares one oscillator, bias circuit, etc. Furthermore, it should be noted that the work employs an isolation capacitance with “back to back configuration” to obtain a small area of isolation element while also withstanding high V_{PK} surges.

This work employs capacitive isolator with tiny area of isolation element, as a result, sacrificing data rate and propagation delay. For normal signal transmission, a high gain receiver is adopted, however, leading to the limitation of CMTI. Nevertheless, this work overcomes this limitation by adopting the OOK modulation and the optimized architecture. To reject noise and CMT, the fast start-up ring oscillator with frequency feedback provides high frequency carrier signal for the modulation. Then, the mixer enables the TX to keep generating the fully differential high frequency carrier signal during disturbances from very fast CMT. In addition, the receiver demodulates the received signal to the original signal, meanwhile, adopting pre-amplifier to suppress the interference of CMT.

Here, key nodes’ waveforms of the OOK modulator and demodulator are shown in Fig. 3. The TX modulates the digital input signal V_{in} into *cap_in_m* and *cap_in_p* and then transmits them through the isolation capacitor. The RX receives the *cap_out_m* and *cap_out_p* and then demodulates them into V_{out}. The waveform's thorough description will be handled in the transmitter and receiver sections, respectively.

A. Transmitter

The transmitter, consisting of a Schmitt trigger and a mixer, meets the demand to make the digital isolators robust, high operational speed performances and low power consumption in the most noisy harsh environment.

When a high frequency signal is input, the rising and falling edges of the signal may ring due to the parasitic impact on the PCB. As a result, the Schmitt trigger is critical in eliminating transient glitch by functioning as a noise filter. On the other hand, the voltage range of input signal from external is from 2.25 V to 5.5 V. Therefore, the Schmitt trigger operates as a level shift, allowing the wide range of voltage to adapt to the internal voltage, which is around 1.8 V supplied by the LDO, resulting in faster speed and less power disturbance. In addition, the delay generated by the Schmitt trigger itself should be as short as feasible, and it should consume as little static power consumption as possible. Here, this work employs a Voltage-Current high-speed Schmitt trigger, which comprises of a voltage hysteresis comparator and an operational current amplifier (OCA), for fast transient response. The voltage hysteresis comparator, which adopts the traditional push-pull output comparator with diode-connected load, has larger bandwidth. In addition, the input voltage is converted into a current signal through a high-pass circuit constituted of capacitor and resistor for the OCA. Compared with operational transconductance amplifier (OTA), the output swing of OCA is not limited by the bias current, but rather by the input current and the current gain of the current amplifier. Therefore, the OCA provides a fast feed-forward path to increase the speed of

transient response when the input changes. Meanwhile, it draws small current consumption when the input is maintained in quiescent mode. The proposed Schmitt trigger only generates 1 ns propagation delay, which is about half of that of the traditional voltage hysteresis comparator.

The OOK mixer, which using simple yet reliable digital logic circuit, mixes and transmits fully differential OOK signal. The OOK mixer combines the input signal with a high-frequency oscillation carrier signal for one input logic high. When one input logic is low, however, no energy is supplied across the barrier. Compared with OOK modulation in [1], the oscillator is working all of the time, consuming more power. Nevertheless, without extra start-up and die-down time optimized, this quite simple yet reliable scheme benefits high data speed and minimum propagation delay.

B. Receiver

The receiver, consisting of a pre-amplifier, an envelop-detection demodulator and a level shift, significantly reduces the propagation delay and increase the data rate dramatically.

This work employs a gate-cross-coupled common gate amplifier with an active zero load as pre-amplifier and a filter before pre-amplifier. Since the signal will be substantially attenuated after the isolation capacitor with the parasitic capacitance, the pre-amplifier amplifies the high-frequency carrier signal for the later demodulation. It means that a high-gain receiver is required to amplify the high-frequency carrier signal while suppressing the noise and CMT. Besides, the high-pass filter can further aid in the transmission of high-frequency signal. Here, the high-pass filter is actually formed by the isolation capacitance, the parasitic capacitance to substrate and the input impedance of pre-amplifier. In addition, the RX employs a envelop-detection, an integrator and a filter as the demodulator to detect and rebuild the high-frequency carrier signal. In which, V_{in+} and V_{in-} are differential input signals, while V_{th} is the demodulator's threshold voltage. According to the principle of OOK demodulation, the common-mode voltage of V_{in+} and V_{in-} is lower than Vth, and the peak of V_{in+} and V_{in-} is higher than V_{th}. Firstly, the comparator shapes V_{in+} and V_{in-} into steamed bread waves. When the input signal is higher than the threshold, the comparator's output becomes high. On the other hand, when the input is lower than the threshold, the comparator's output becomes low. Following that, if sufficient energy is discovered, the integrator produces a high-level output. Finally, the integrator's output glitch is filtered and shaped into a square wave by the filter. However, the design will encounter two potential issues: amplifier gain insufficiency and noise interference. Therefore, the threshold voltage and RC constant should be carefully designed for the compromise between propagation delay and the accuracy of demodulator.

The level shift makes the internal voltage from around 1.8 V to an external wide range voltage from 2.25 V to 5.5 V. Here, the level shift is designed for rendering decent transient response while maintaining low power consumption by using OCA to form a fast feed-forward path similar to Schmitt trigger. Similarly, the proposed level shift only causes 1 ns propagation delay, which is roughly half of that of the traditional level shift.

Iii. Circuit Implementation

Using the small isolation capacitance, a high-gain receiver is required to enhance to amplify the high-frequency carrier signal while blocking the noise and the CMT surging from one voltage domain to another. Since, the pre-amplifier is the key design for superior CMTI. Besides, aiming to improve CMTI without sacrificing data rate and propagation delay, the demodulator and oscillator should be designed for high operational speed performances. Therefore, the circuit implementation of pre-amplifier, demodulator and oscillator are also dscussed in following.

A. Pre-amplifier Design

Figure 4 gives the circuit implementation of the proposed pre-amplifier, which consists of gate-cross-coupled common gate amplifier, coupling capacitor for fast path, active zero load and a high-pass filter. The pre-amplifier is fully differential with symmetric layout to improve noise immunity. Here, the bias circuit is made up of an *IPTAP*, M_{N4} ~ M_{N2}, M_{N3} ~ M_{N1} and R_2, R_3. With the consistent bias circuit, it provides good common-mode rejection. Moreover, the gate-cross-coupled common gate amplifier doubles the differential-mode gain to double G_m, and cancels the common-mode gain for further common-mode rejection. In addition, the fast path through the coupling capacitor C_3, C_4 aids in enhancing the equivalent gain while maintaining the DC operation.

The common-mode transition with its harmonic overtones and parasitic oscillation has a frequency of less than tens megahertz [2] whereas the signal component flowing through the isolation capacitance consists of hundreds megahertz band. Therefore, it means that CMTI can be improved by a frequency selective circuit and a high-pass filter. Here, an active zero compensation circuit, composed of M_{P1}, R_1 and C_1, is designed as the load of the amplifier. The high-frequency high gain is preserved when the suggested active zero load is used, whereas the low-frequency gain is considerably reduced. Besides, the isolation capacitance C_5, the parasitic capacitance from lower plate to substrate C_6 and the input impedance of pre-amplifier, which is limited by the sampling resistance $R_{3,}$ operate as a high-pass filter, filtering the CMT and noise. As a result, the pre-amplifier can provide a high gain of 35 dB at high frequency of 500 MHz and a low gain of 10 dB under the frequency of 20 MHz.

The decent gain of the proposed pre-amplifier adapting active zero and high-pass filter is also verified. Eq. (1) describes the overall transfer function. Moreover, the G_{MN2} is double the g_{MN2} under this bias.

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} \approx \frac{\mathrm{sR_3C_5}}{\mathrm{sR_3C_6+sR_3C_5+1}} \times \frac{2\mathrm{g_{MN2}}(1+\mathrm{sRC_1})}{\mathrm{g_{MP1}+sC1+s^2RC_1C_2}}$$

1

B. High-pass Filter

The operation principle of the proposed high-pass filter is described from both qualitative and quantitative perspectives. From the qualitative aspect, the signal and the CMT are in separate frequency

domains, therefore, the high-pass filter can boost the CMT. Here, a displacement current is caused by a shift in potential at the capacitance. As a result, tiny R_{in} is employed to protect fragile pre-amplifiers while also making signal transmission resilient to high CMT. The bigger C_{iso} is, the larger current will surge across the isolation barrier from TX side when CMT occurs. For input impedance, the bigger R_{in} is, the more signal can be detected. However, it should not be constructed excessively large, which may accumulate a large voltage due to the current. Therefore, the RX will operate incorrectly, resulting in the wrong transmission. Moreover, it may even destroy devices on RX side. Thus, there is a trade-off between the performance of signal and CMTI. Scilicet, bigger C_{iso} and R_{in} leads to modest attenuation signal but a significant operation offset by the CMT.

From the quantitative aspect, the value of the isolation capacitance and the input impedance require matching design to improve CMTI. As can be seen from the blue shadow box and Eq. (2), $C_5/(C_5 + C_6)$ determines the peak value of response, and the R_3C_5 constant determines the time of discharge. The bigger the C_5 is, the better the signal in V_x at high-frequency, meanwhile, the smaller the C_6 is, the litter attenuation occurs in V_x. The capacitor C_6 can be reduced by making the lower plate of the isolation capacitance in the higher layer of the metal. It can increase the capacitor C_5 simultaneously while decreasing the isolation voltage of isolation capacitance.

$$\frac{\mathrm{V_x}}{\mathrm{V_{in}}} \approx \frac{\mathrm{sR_3C_5}}{\mathrm{sR_3C_6+sR_3C_5+1}}$$

2

Here, CMT is dominated by dV_{CMT}/dt. As shown in the Eq. (3), a shift of potential at the capacitance causes a displacement current. The bigger the C_5 is, the current caused by the CMT is larger. However, a 150 kV/μs CMT from TX side may cause 1 V *IR* drop on the R_3. The gain stage of the pre-amplifier is constructed over the sampling resistance R_3, resulting in the DC operation offset. The proposed high-pass filter absorbs and sources the current caused by CMT while having minimal impact on the operation of the pre-amplifier.

$$\mathrm{I_{CMT}} \approx \frac{\mathrm{C_5 dV_{CMT}}}{\mathrm{dt}}$$

3

C. Active Zero Circuit

The active zero is implemented to render decent gain at high-frequency while maintaining low power consumption. Figure 5 shows the gain plots of active zero circuit used in the pre-amplifier. Here, an active zero is implemented using a local feedback. In active zero circuit, the local feedback T_{AZC} is formed by R_1, C_1 and g_{MP1}. The feed-forward path through R_1 is essentially “open” and the impedance of the load at low-frequency is still approximates $1/g_{MP1}$. Since the R_1C_1 is large, the current through R_1 is gradually

increasing as frequency goes higher. Scilicet, the feedback reduces the impedance at V_{out} to $1/g_{MP1}$, and increases the impedance with the weakening of feedback gain at higher frequency. The gain from V_x to V_{out} increases when a zero occurs at $1/R_1C_1$ and flattens out when the first pole is met at g_{MP1}/C, which equals to the bandwidth of T_{AZC}. Besides, the gain from V_x to V_{out}, given by Eq. (4), indicates another pole at $1/RC_2$, where the gain begins to decrease. Due to this inductive load, the high frequency carrier signal can be amplified and low frequency noise can be filtered by the pre-amplifier. Meanwhile, occurring the same gain in the high frequency, the power consumption is much lower than that of amplifier with active zero load.

$$\frac{V_{out}}{V_x} \approx \frac{2g_{MN2}(1+sRC_1)}{g_{MP1}+sC1+s^2RC_1C_2} \quad (4)$$

D. Demodulator Design

Figure 6 gives the circuit implementation of the proposed demodulator, which consists of envelop-comparator, integrator and filter. This demodulator can improve the CMTI without sacrificing propagation time. Here, traditional three-input comparator works as envelop-comparator with V_{in+} and V_{in-} as differential input signals and V_{th} as the demodulator's threshold voltage. According to the OOK modulation and demodulation, the common-mode voltage of V_{in+} and V_{in-} is lower than V_{th}, while the peak of V_{in+} and V_{in-} is higher than V_{th}. Besides, the N_{bias} keep the voltage balance and cancel the offset of the comparator. When V_{comp} is high level, the gain plots of integrator circuits using in the demodulation is shown in Fig. 7. Importantly, after several input sine wave cycles the output of the following integrator with R_0C_0 constant produces a high-level output as illustrated in the Eq. (5). Hence, the R_0C_0 constant should be carefully designed for the compromise between propagation delay and demodulator's accuracy. In addition, R_1 is set to trim flip point of the integrator to improve the CMTI and be immune to the noise. Finally, the integrate output glitch is filtered and shaped into a square wave by the low-pass RC filter. Simultaneously, it can further provide a decent improvement in CMTI by canceling the glitch generated by the CMT while maintaining signal transmission. Moreover, due to the sampling digital logic circuit, there is no extra propagation delay generated by the filter.

$$\frac{V_{int}}{V_{comp}} \approx \frac{1+sR_0C_0\text{-}R_0\left(\frac{g_{MP1}}{(1+g_{MP1}R_2)}+\frac{g_{MN1}}{(1+g_{MN1}R_1)}\right)}{1+sR_0C_0}$$

5

E. Oscillator Design

The oscillator forms the core of the OOK modulation scheme, and its start-up time and frequency accuracy across PVT are major design factors. The work employs a fast start-up ring oscillator with

frequency feedback for high accuracy. As shown in Fig. 8, the M_{P1}~M_{P3} and the M_{N1}~M_{N3} forms the main part of the oscillation. In the start-up stage, the oscillator uses a high-pass filter C_2, R_2 to filter out low-frequency signals. Meanwhile, when the OSC is low-level, the M_{P4} will maintain open to supply a strong current to the ring oscillation for fast start-up speed. Besides, the blue shadow box describes the frequency feedback circuit. It transmits the signal to the frequency-voltage conversion network, realizing closed-loop control of the frequency, achieving high precision of the oscillation frequency. Compared with the traditional oscillator, the oscillator features a faster start-up speed and better frequency accuracy. It can deliver a precise 430 MHz high-frequency carrier oscillation, which is ideal for high data rate signal transmission. According to the Nyquist theorem, the frequency of oscillation is dominated at least twice the maximum date rate of the transmission signal.

Iv. Chip Fabrication And Experimental Results

Typical data rate and Common-mode transient noise rejection post-simulation is shown in Fig. 9. The amplitude of the surge impacting in the RX is almost proportional to the slew rate of the CMT. Moreover, this 600 mV voltage shifts prevent the receiver circuit from detecting an appropriate logic level. Nevertheless, the pre-amplifier can suppress the surge impact and provide enough gain for comparator to transmit right signal. As shown in the post-simulation result, it can accomplish 200 kV/μs CMTI and 250 Mbps data rate.

A. Chip Fabrication

The proposed capacitively coupled digital isolator was implemented and verified using a 0.18 μm isolated CMOS technology with no need of extra process. The structure of the isolation capacitance provided by the PDK is shown in Fig. 10. The TM1 metal is used as the lower plate of the capacitance, the SMT2 metal is used as the upper plate of the capacitance, and the 20 μm thick SiO_2 between the two layers is used as the insulation material. Obviously, the capacitance is not a standard device, but the parasitic capacitance between metal layers is used as the isolation capacitance. Besides, while considering the signal attention and the current caused by CMT, the parasitic capacitance between the lower plate and substrate must be attached.

According to the data from PDK, 20 μm thick SiO_2 of this isolated technology can provide 7,000 V isolation voltage. Moreover, with the “back to back configuration” that uses bonding wire to connect the isolation capacitances on both sides of the die, the capacitance provides twice the isolation breakdown voltage, which is 14 kV. At the same time, the capacitance becomes half that of a single side. In addition, the isolation element area is 2×10^4 μm^2, which is 1/10 – 1/2 that of transformer-based isolator and 2/3 that of other capacitively coupled isolator [2, 5].

As shown in Fig. 11 (a), there are two dies on one chip with four transmission channels, and each channel contains two isolation capacitances for differential transmission. Figure 11 (b) gives the single die photo of the prototype with area of around 1470×690 μm^2. The isolation element area of one channel is 2×10^4 μm^2, which is 1/2 that of [1], 1/10 that of traditional transformer-based isolator and 2/3 that of [5]. Here,

two dies are connected by a bonding wire through the isolation capacitances on both sides of the die. The prototype operates with an input voltage and output voltage from 2.25 V to 5.5 V, and generates an internal core circuit around 1.8 V. Besides, it can operate in a wide temperature range from − 55 ℃ to 125 ℃.

The test platform for the propagation function can measure the electrical parameters and dynamic characteristics of the isolator, consisting of propagation delay, maximum data rate, power consumption, and cross-talk coupling between multiple channels, etc. On the other hand, it requires a test platform for CMTI, however, the difficulty of the CMTI test is to generate a CMT with a controllable slope. Here, Fig. 12 shows a test platform test for the CMTI. CMT, confirmed by dV_{CMT}/dt, is generated by the slope generator chip and powered by a battery pack. Moreover, the peak voltage of the CMT is also important, which determining the duration of the CMT. Finally, the CMTI was calculated by detecting whether an incorrect transmission appeared in the output of RX. However, the testing platform can only produce voltage with maximum slope of 162 kV/μs and amplitude of 1,364 V, which is limited to the maximum CMTI of this work.

B. Experimental Results

Here, VCCI is the supply voltage for die A, while VCCO is the supply voltage for die B. DR1 and DR2 are the different input data rate for two channels, which can measure the cross-talk between these two channels. A low-speed operation is shown in Fig. 13 (a) (b), in which two channels transmit 10 Mbps and 4 Mbps signals, respectively. As Fig. 13 (a) given, the supply voltage in die A is 2.25 V, while the supply voltage in die B is 5 V. As Fig. 13 (b) given, the supply voltage in die A is 5 V, while the supply voltage in die B is 2.25 V. Signals can be conveyed normally, besides, there is no crosstalk in the output signals between the two channels. Figure 12 (c) (d) demonstrates a high-speed operation, where two channels transmit both 100 Mbps signals. As Fig. 13 (c) given, supply voltage in die A is 2.25 V, while the supply voltage in die B is 5 V. As Fig. 12 (d) given, supply voltage in die A is 5 V, while the supply voltage in die B is 2.25 V. The typical propagation delay from input to output is 6 ns, as shown in Fig. 13 (d), with a fluctuation of less than ± 1 ns depending on supply voltage and temperature. Furthermore, the consistency of signal transmission between different channels is solid. There is 1.5 mA power consumption per channel at 1 Mbps with 5 V supply and 15 pF load.

As shown in Fig. 14, the Shmoo measures the maximum data rate of the chip. As for Shmoo figure, the X axis represents the periods of signal, which range from 8 ns to 20 ns and can be converted into data rate. On the other hand, Y axis represents the sampling point, such as, 0.1 means that the sampling point is at the location of the 0.1×period. Moreover, it requires at least 2000 sampling points in each period for the accuracy. Besides, green indicates that the output value matches the expected value at this sampling point in this period, indicating that the signal can be transmitted normally. It shows that when the transmission period is 9 ns, that is, the data rate is 230 Mbps, Shmoo is passing at the sampling point of 0.55×period. According to the scanning by Shmoo, the maximum data rate is 230 Mbps.

Figure 15 shows the measured CMTI performance for positive CMT pulse under the typical operating conditions, that is, VCCI and VCCO are 5 V. In this test platform, the high voltage amplitude is 1,364 V and 162 kV/μs slew rate, and it is injected into the ground of die A. As can be seen, the yellow line represents the ground voltage in die A, whereas the green line depicts ringing induced by the parasitic capacitance of the PCB with rapid current when CMT but not by the transmission is incorrect. Here, it can be seen that the input is logic high, and the output is always high without the glitches due to incorrect transmission. The higher CMTI test is limited by the test platform. Nevertheless, it signifies that the CMTI can achieve at least 162 kV/μs.

Table I demonstrates the performance summary of the proposed work and the prior state-of-the-art. It can be inferred from the table that the proposed work achieved superior CMTI, fast speed of data rate, low propagation delay, small isolation element area and high isolation voltage.

TABLE I. Chip Specifications

	VLSI 2016 [1]	**JSSC 2012 [2]**	**ICICDT 2019 [4]**	**TI ISO77xx 2020 [5]**	**This Work**
Isolation Element	Transformer	Transformer	Transformer	Capacitor	Capacitor
Isolation Element Area Per Channel	Unknown	4.15×10^4 μm^2	5.00×10^4 μm^2	3.00×10^4 μm^2	2.00×10^4 μm^2
Isolation Material	Polyimide	SiO_2	Unknown	SiO_2	SiO_2
Modulation Architecture	OOK	Pulse	Pulse	OOK	OOK
Max Data Rate	Unknown	250 Mbps	500 Mbps	100 Mbps	230 Mbps
Propagation Delay	11 ns	5.5 ns	Unknown	10.7 ns	6 ns
CMTI	200 kV/μs	35 kV/μs	130 kV/μs (simulation)	100 kV/μs	162 kV/μs
Idd@5 V, 1 Mbps	2.8 mA	1.6 mA	1.16 mA	1.5 mA	1.5 mA
Isolation Voltage	20 kV	2 kV	1 kV	5 kV	14 kV
Supply Range	1.7 ~ 5.5 V	3.3 ~ 5.5 V	Unknown	2.25 ~ 5.5 V	2.25 ~ 5.5 V

V. Conclusion

In this paper, a small-size on-chip capacitively coupled digital isolator with high value of Common Mode Transient Immunity (CMTI) and operational speed performances is presented. Here, differential On-Off Keying (OOK) modulation is adopted to prevent CMT noise. In addition, the scheme employs a gate-cross-coupled common gate amplifier with an active zero load as pre-amplifier. Besides, a high-pass filter before pre-amplifier is applied to further cancel the effect of CMT and helps to transmit high-frequency signal. For high operational speed performances, the work utilizes the Voltage-Current high-speed comparator with fast feed-forward path as Schmitt trigger and level shift, and employs the envelop-comparator, integrator and filter as demodulator, thereby, significantly reducing the propagation delay and speeding up the data rate. Fabricated in a 0.18 μm isolated CMOS technology with no need of extra process, the isolation element is 2×10^4 μm^2, which is 1/10 − 1/2 that of transformer-based isolator and 2/3 that of other capacitively coupled isolator. Moreover, it can provide twice the isolation voltage by “back to back configuration”. The prototype operates with an input voltage and output voltage from 2.25 V to 5.5 V, and generates an internal core circuit about 1.8 V. Besides, it can operate in a wide temperature range from − 55 ℃ to 125 ℃. The prototype can achieve an over 162 kV/μs CMTI, a 230 Mbps data rate, a 6 ns small propagation delay, a 1.5 mA dynamic current and 14 kV isolation breakdown voltage.

Declarations

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Author Contributions Statement

Mr. Jingbo Zeng wrote the main manuscript and designed the main integrated circuit. Mr. Yuhao Yang assisted with thesis writing. Mr. Chenfei Jiang participated in designing integrated circuit and layout. Mr. Yifeng Peng assisted with chip experimental. Mr. Jianxiong Xi supervised the reasch of the integrated circuit and layout. Professor Lenian He supplied the research funding and research group and checked the manuscript with constructive discussions. All authors reviewed the manuscript.

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Figures

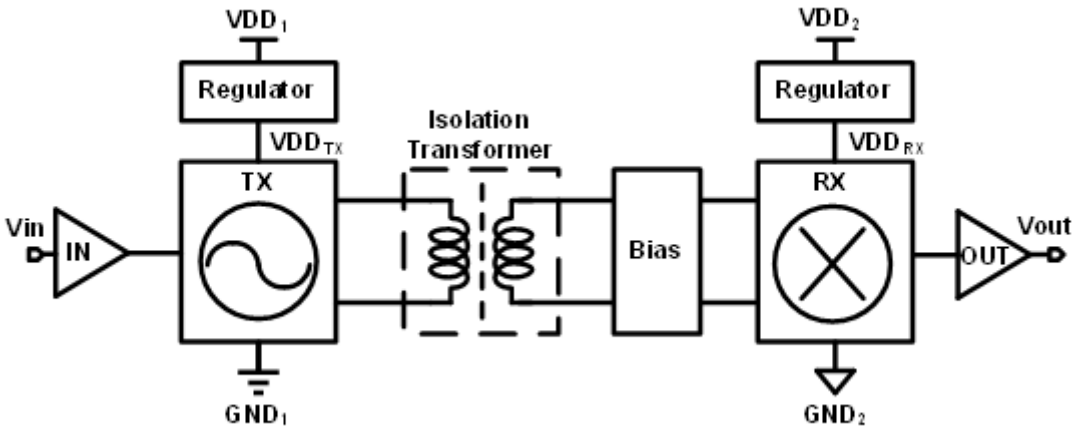


Figure 1

Block diagram of a transformer-based digital isolator architecture.

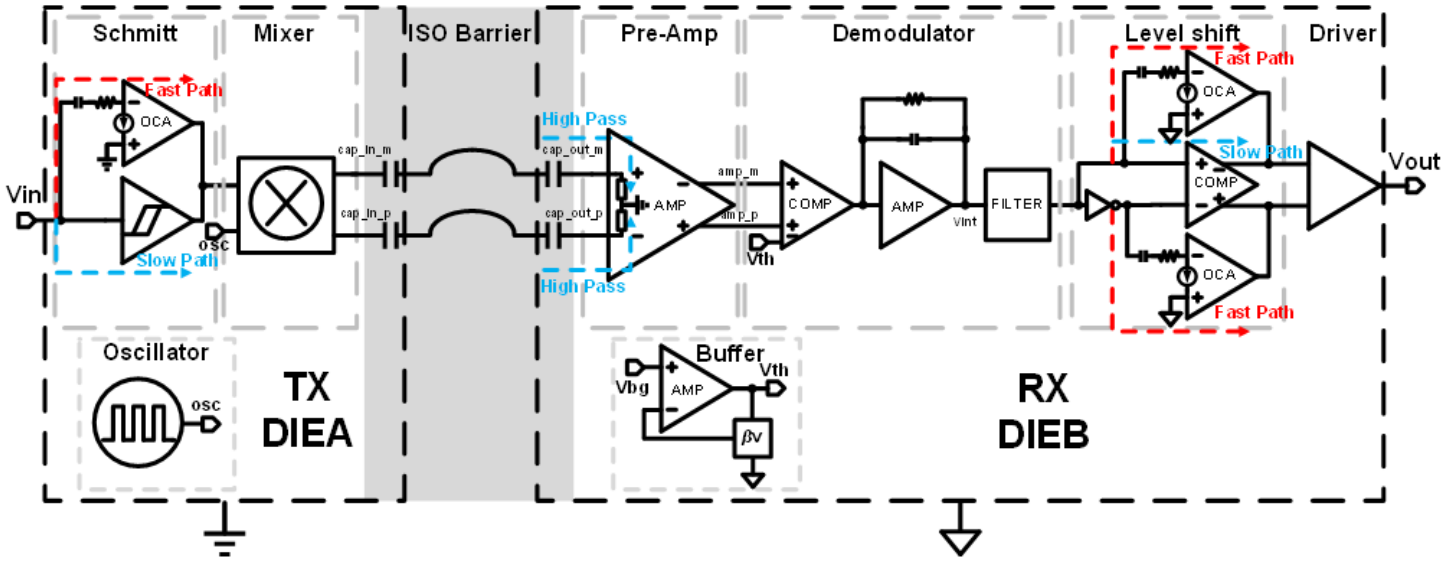


Figure 2

Block diagram of proposed capacitively digital isolator architecture with superior CMTI and operational speed performances.

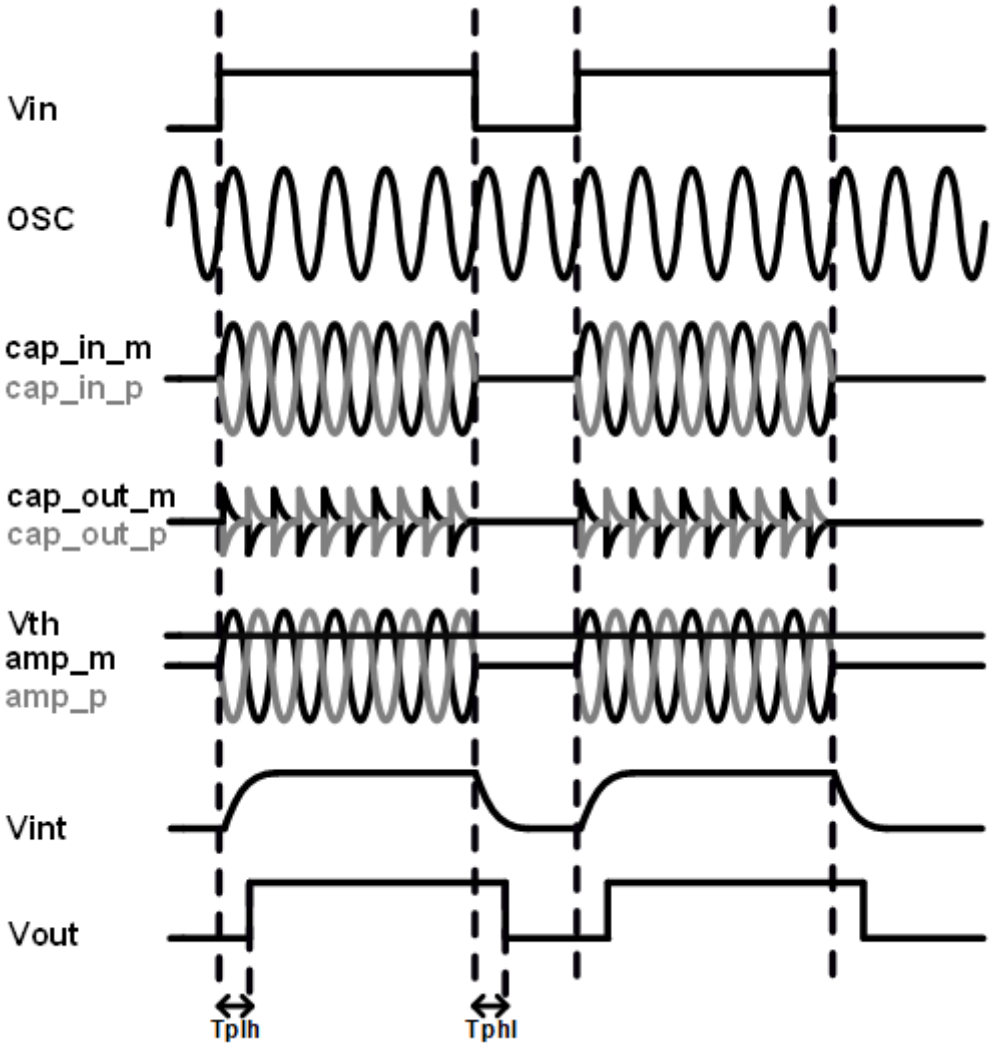


Figure 3

Modulator and demodulator operation waveform.

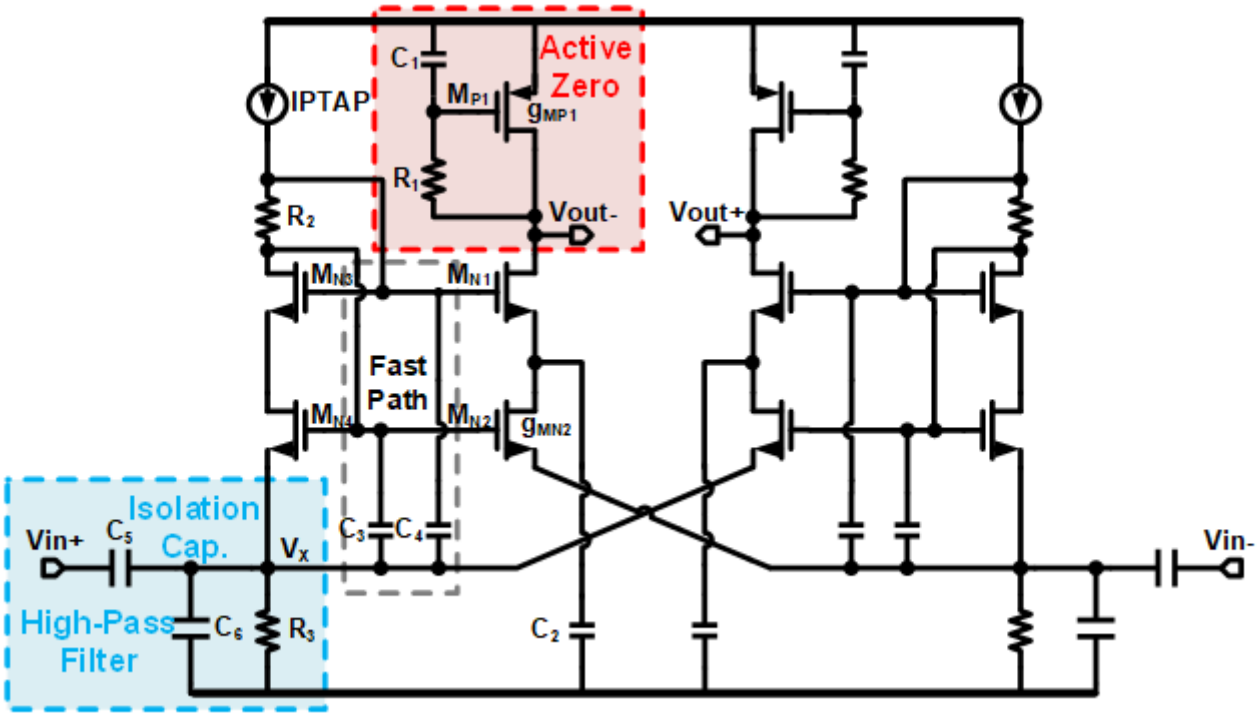


Figure 4

The proposed pre-amplifier with active zero load and high-pass filter.

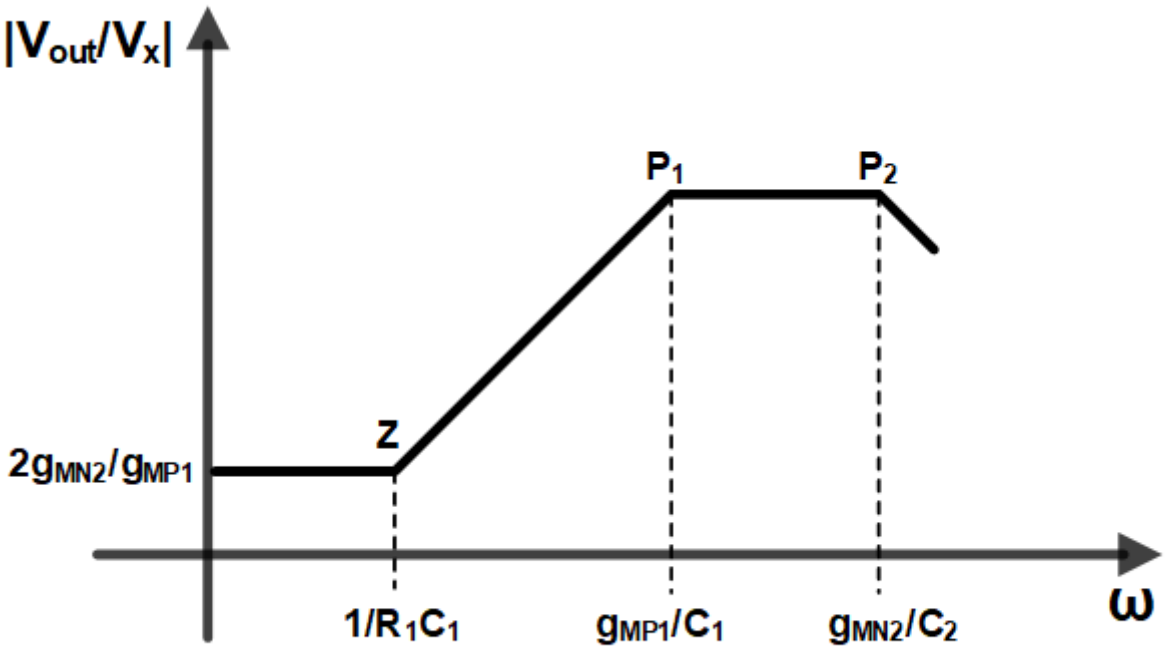


Figure 5

Gain plots of active zero circuits using in the pre-amplifier.

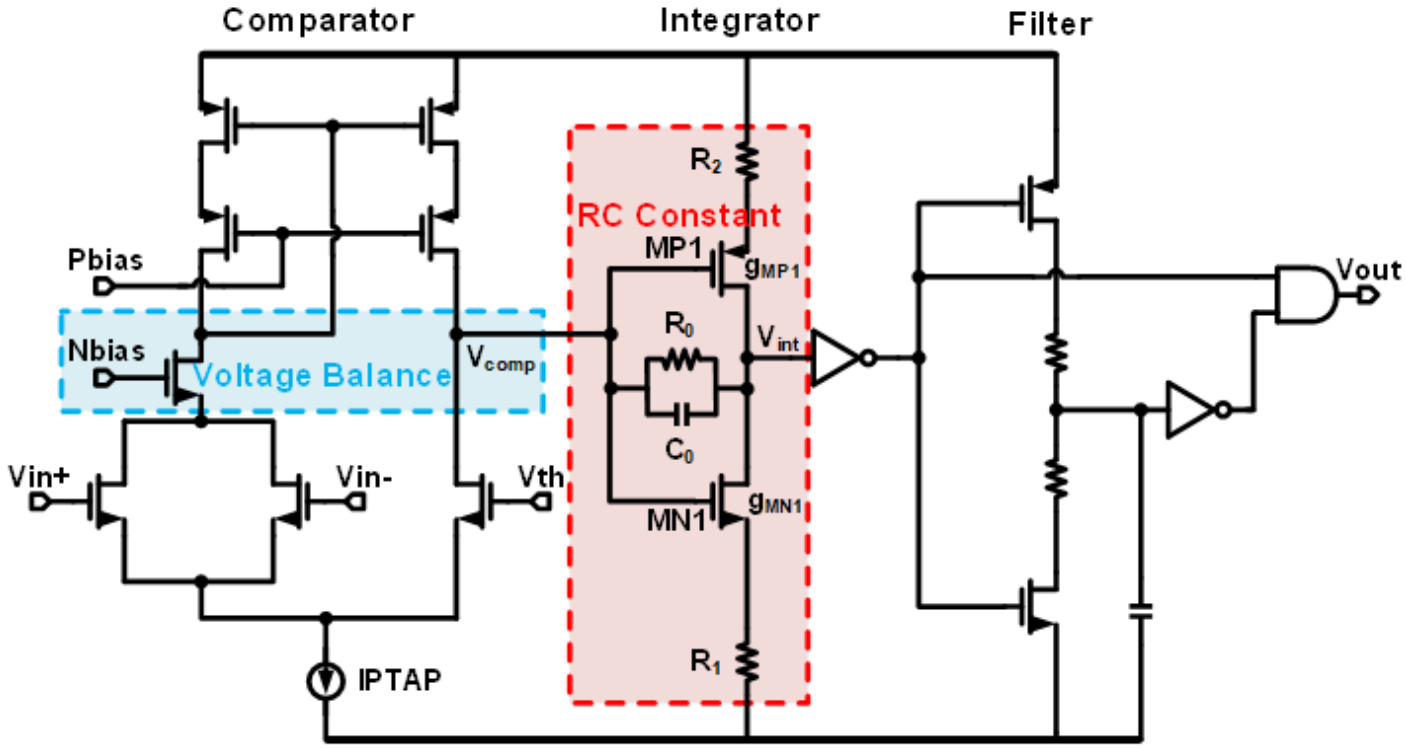


Figure 6

The proposed demodulator.

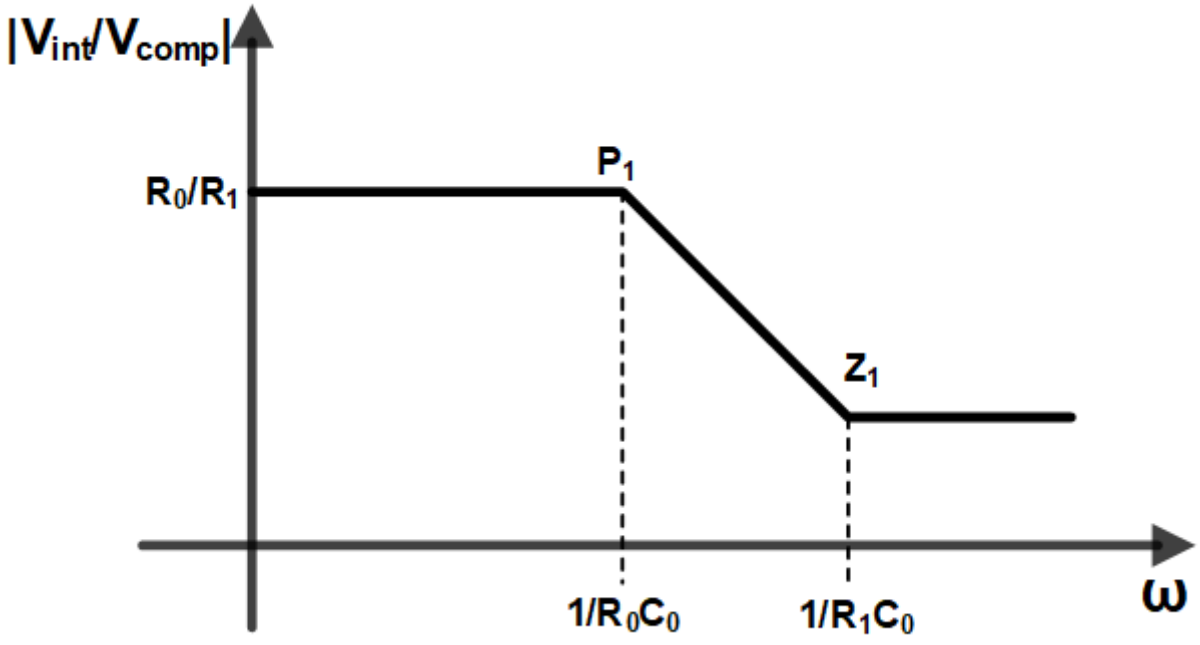


Figure 7

Gain plots of integrator circuits using in the demodulator.

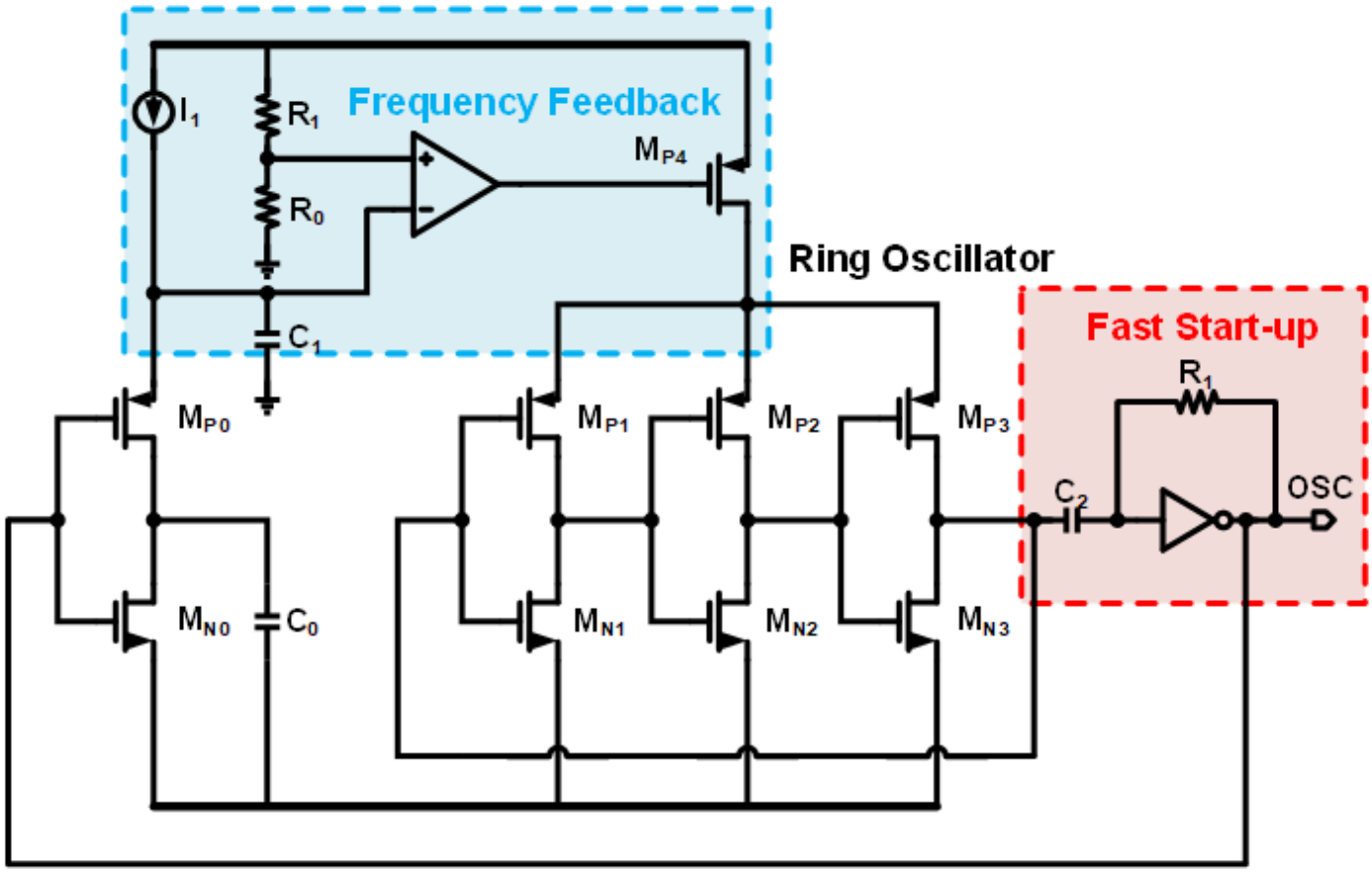


Figure 8

The proposed fast start-up high accuracy oscillation.

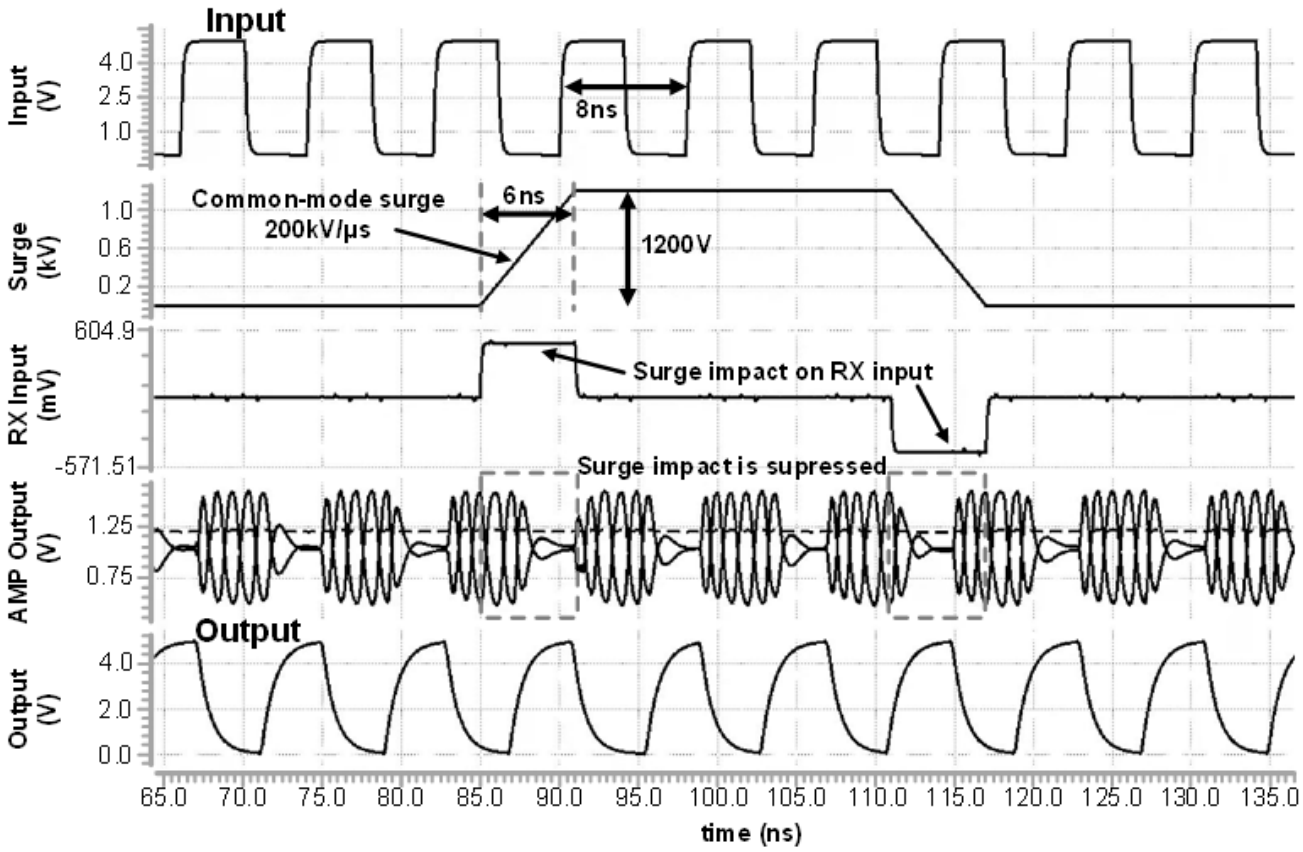


Figure 9

Post-simulation of operation under CMT: 250Mbps data rate, 200 kV/µs CMT, 5 V power supply, 15 pF load, 25 °C.

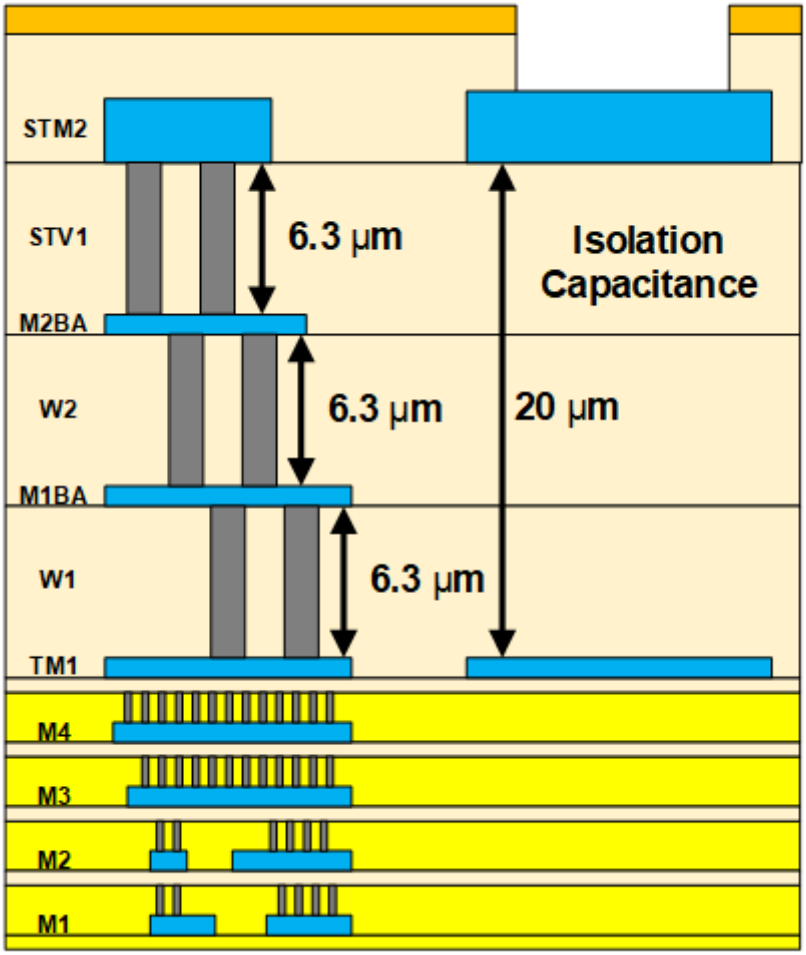
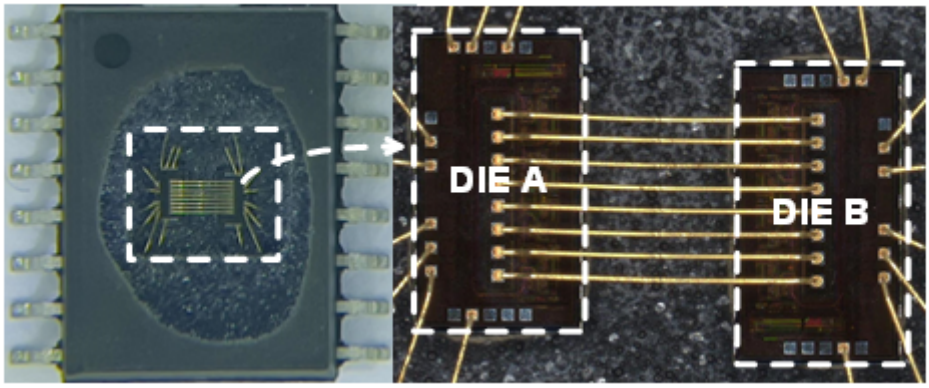
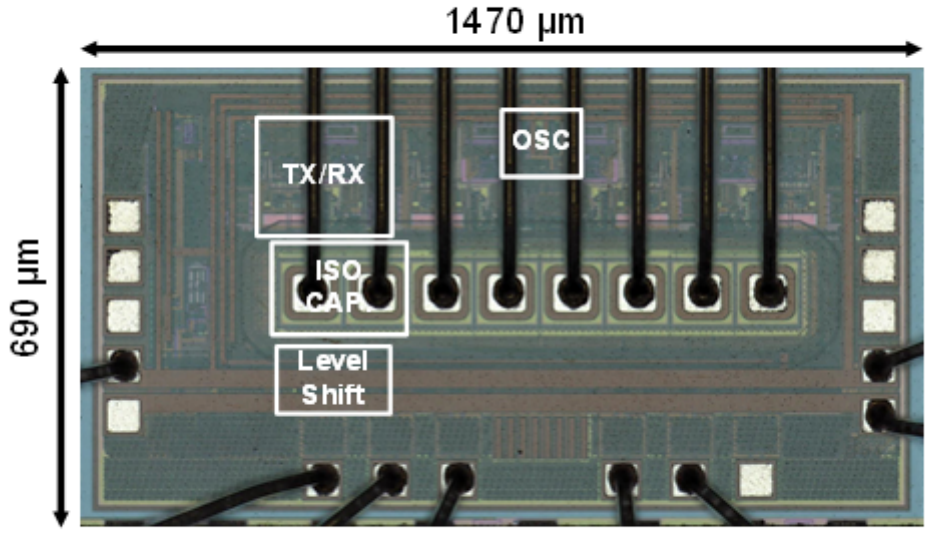


Figure 10

Structure of isolation capacitance.



(a)



(b)

Figure 11

Micrograph of the (a) chip, (b) single die.

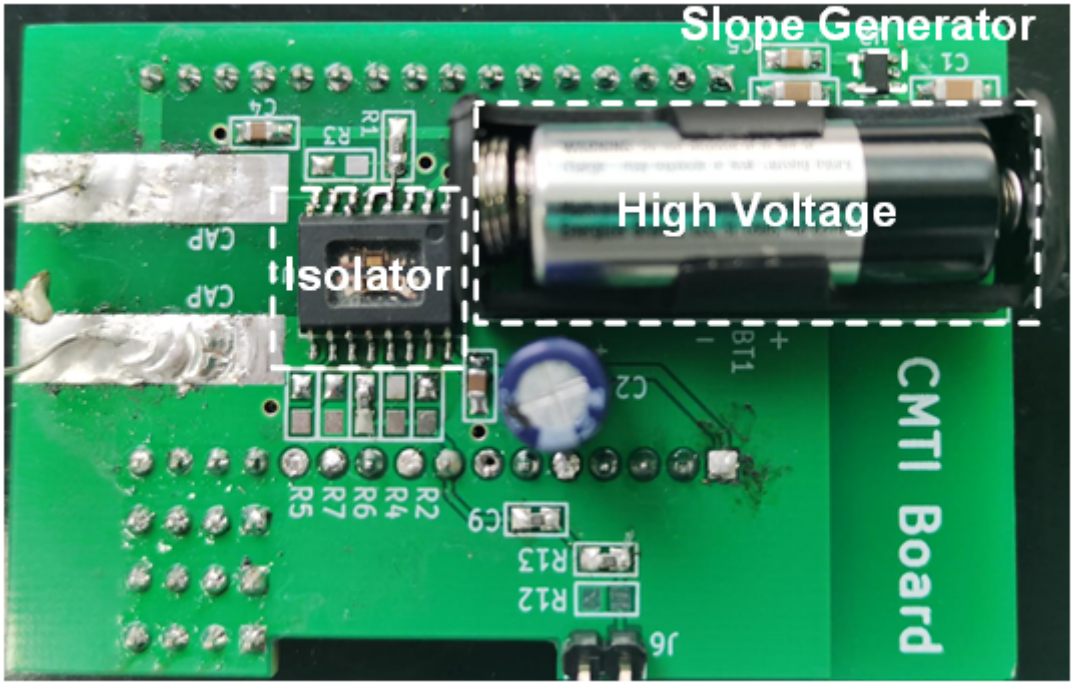


Figure 12

Testing platform of CMTI.

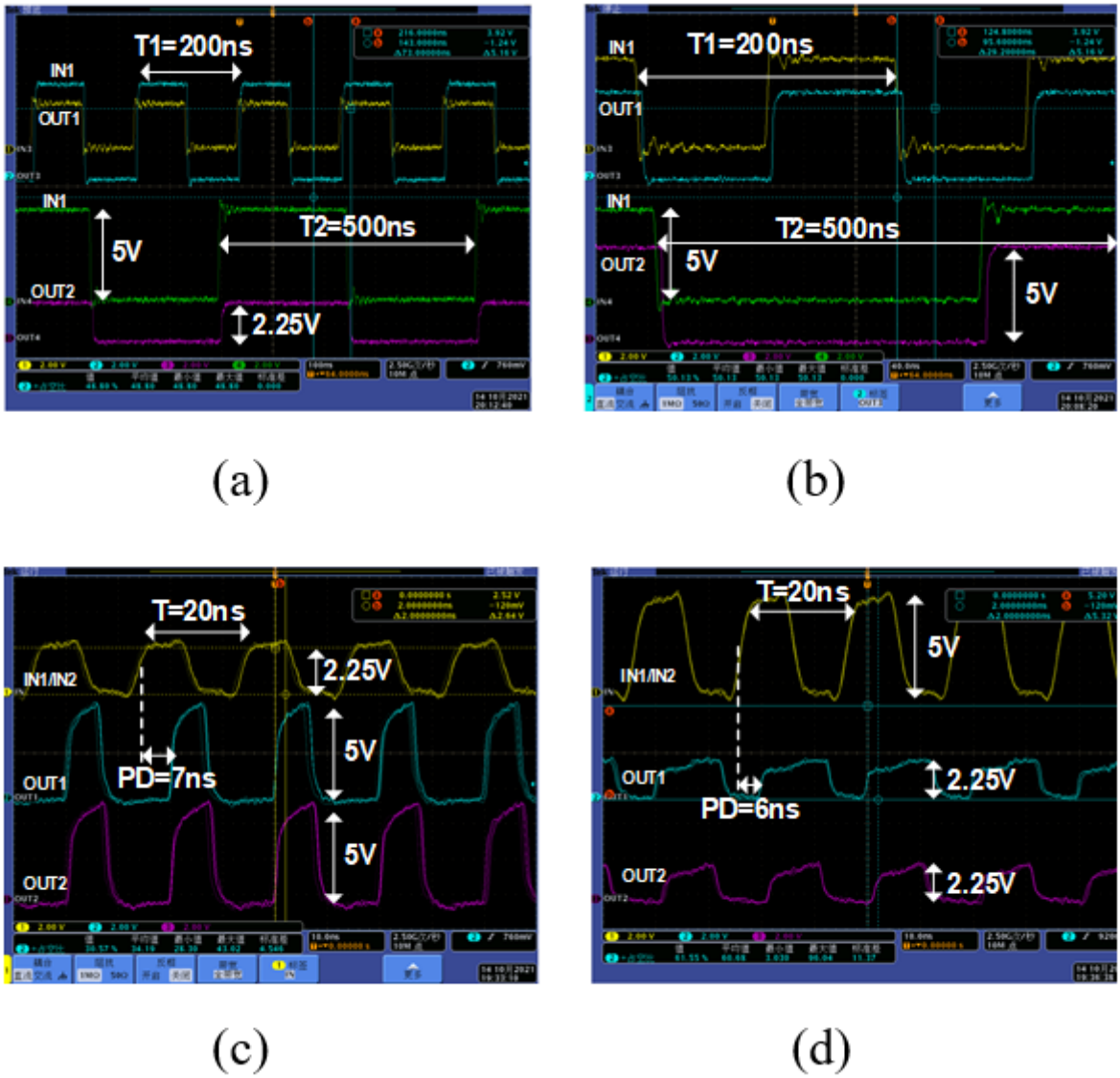


Figure 13

Propagation test: (a) VCCI=2.25 V, VCCO=5 V, DR1=10 Mbps, DR2=4 Mbps, (b) VCCI=5 V, VCCO=5 V, DR1=10 Mbps, DR2=4 Mbps, (c) VCCI=2.25 V, VCCO=5 V, DR=100 Mbps, (d) VCCI=5 V, VCCO=2.25 V, DR=100 Mbps.

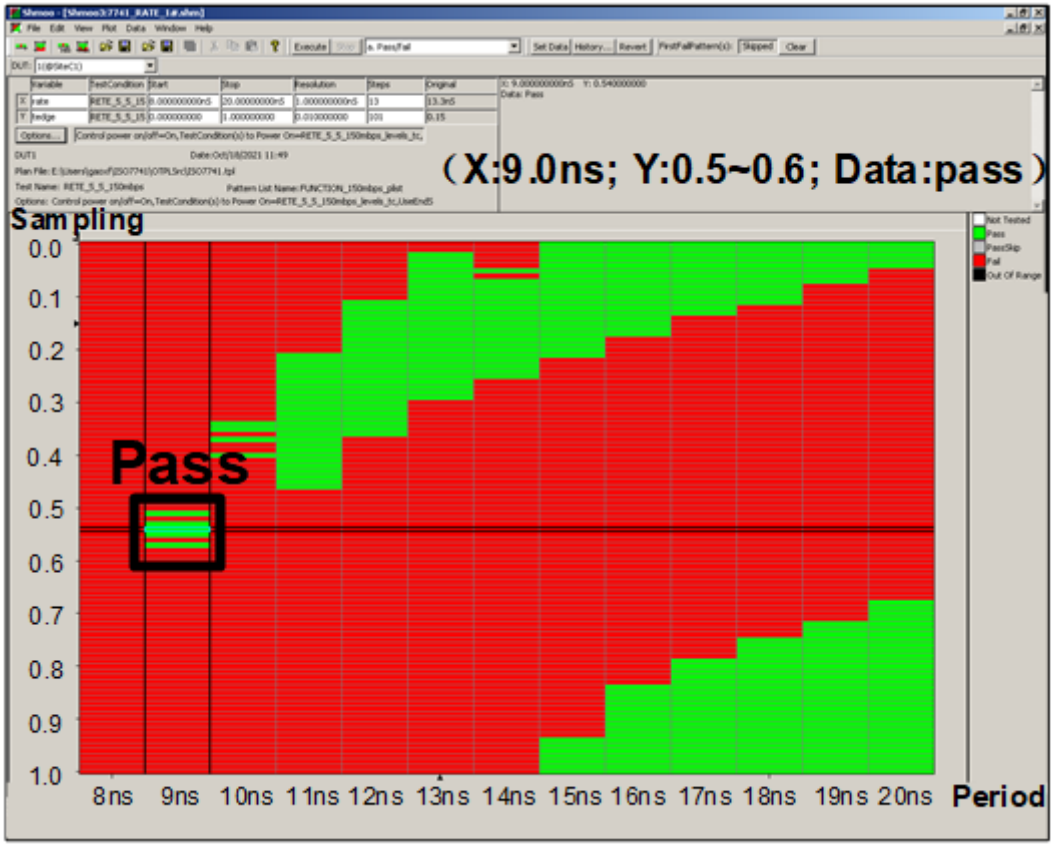


Figure 14

Shmoo of the maximum data rate by shmoo scanning.

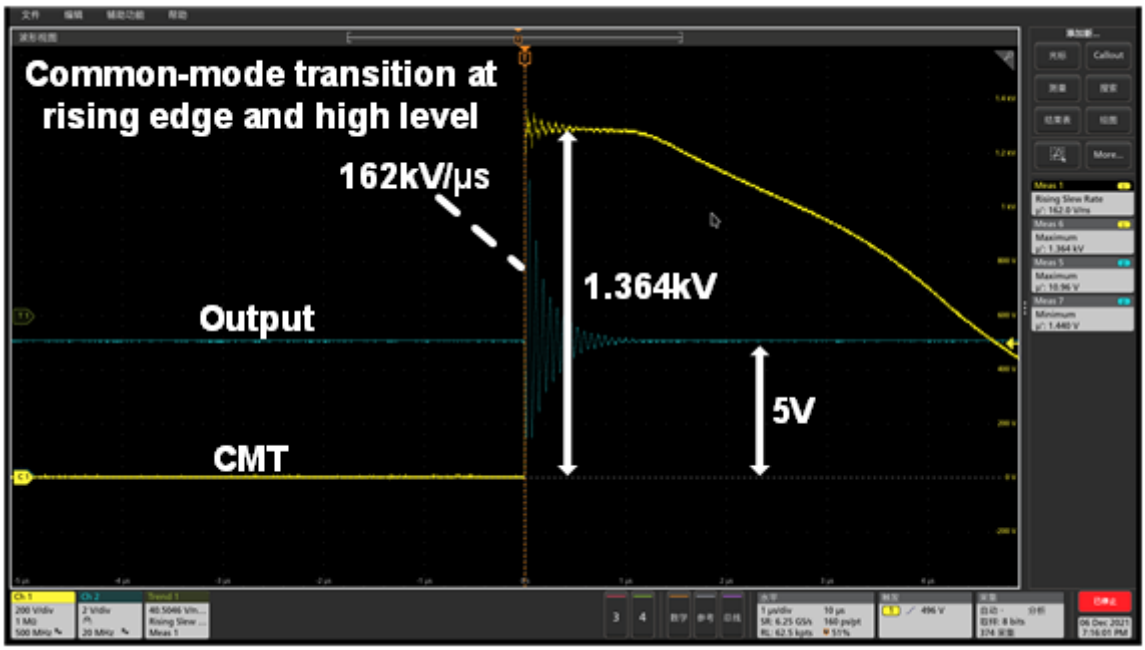


Figure 15

CMTI test with 162 kV/µs, 1,364 V amplitude.