Architecture for at Speed Testing of Crosstalk Faults in Through Silicon Vias in Three Dimensional Integrated Circuits

PRAVEEN KUMAR REDDY K (kpkreddy_99@yahoo.co.in)
RMD Engineering College https://orcid.org/0000-0002-1275-573X
C.Bennila Thangammal
RMD Engineering College
Rangarajan Parthasarathy
Larsen and Toubro Limited

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ARCHITECTURE FOR AT SPEED TESTING OF CROSSTALK FAULTS IN THROUGH SILICON VIAS IN THREE DIMENSIONAL INTEGRATED CIRCUITS

*K.Praveen Kumar Reddy, **C.Bennila Thangammal, ***P.Rangarajan

*Assistant professor, EEE Department, RMD Engineering College, Chennai, India. Email: kpkreddy_99@yahoo.co.in
**Associate Professor, Department of Computer Science Engineering, RMD Engineering College. Email: cbt.it@rmd.ac.in
*** SME, L&T Head Quarters, Chennai, India. Email: rangarajan69@gmail.com

Abstract: A parallel test Algorithm and design for built in self test (BIST) architecture to test the crosstalk faults in clustered arrays of TSVs (through silicon via) in 3DICs (Three dimensional Integrated Circuits) is discussed in this paper. Design of Modified Flexible Boundary scan cells to transfer the outputs to the functional cores or to the Output response analyzers (ORA) or signature analysers is proposed. Algorithm state machine (ASM) based design of BIST controller to generate the control and timing signals for launch and capture of test patterns is discussed. Parallel outputs capturing and signature generation mechanism is designed to reduce the time complexity.
Keywords: BIST, TSV, Crosstalk, modified boundary scan cell, maximum aggressor fault model, IEEEP1838, parallel test output capture.

INTRODUCTION:

Three dimensional integrated circuits (3DIC) is a promising technology to keep Moore's law alive, to integrate more and more components in the given area specifications of IC. 3DICs use the basic idea of vertical integration of components by stacking the dies one on each other, interconnect them by using vertical interconnects called as through silicon vias (TSV) and establish a communication between different dies. But, Testing of Three dimensional Integrated circuits is a major challenge for over years. Recently IEEEP1838 standard [1][2][3] was released focusing the test methodology of 3DIC. This standard focused on reusing the conventional methods of testing like JTAG IEEE1149.1 [4] and IEEE 1500 [5] standards, where serial transmission of test data input is passed through boundary scan registers or die wrapper registers on a die, and also introduced a new design of Flexible parallel ports (FPP) [3] which are used to elevate the serial test data to the upper/lower (primary and secondary) layers of stacked dies. This serial test access uses the mechanism such as INTEST & EXTEST to test functional cores and interconnects between two cores on the same die or between two dies, was designed to test the basic faults such as stuck at and bridge faults only. As the number of interconnects are increasing rapidly in the latest technologies such as High Bandwidth Memory (HBM), The time complexity of serial transmission of test patterns is high. It may not be suitable to implement the test mechanism to find the faults like crosstalk and delay faults, where test pattern transitions are to be applied on neighbouring interconnects simultaneously at the same time. Here in this paper we propose a test access mechanism and architectural implementation of BIST mechanism to test the crosstalk faults in the TSV interconnects. TSVs are usually placed as structured two dimensional arrays [6][11] and are prone to these

Crosstalk and delay faults. There are various research papers in the literature [6][7][8][9][10] addressing the issue, discussed about the distance range of aggressor TSVs to be considered from the victim TSV, while testing for crosstalk faults and also the different approaches of BIST architectures to detect them. But the design and implementation of these architectures was not discussed clearly in this literature. Implementation of test architectures is discussed in this paper. The paper is organized as follows

1. Procedure of Grouping TSV arrays
2. Design of test pattern generator & BIST Controller
3. Design of modified boundary scan cells (launch and capture cells)
4. Illustration of BIST Mechanism
5. Output response analyzer/ Signature analysis

GROUPING A LARGE ARRAY OF TSVS:

In order to test the large array of TSVs, a parallel test algorithm is proposed which tests the entire array in four steps, by grouping the entire array of TSVs in to four sets as shown in fig.1, and applying the test patterns to a set at a step. TSVs shown in red colour are victim group and the aggressors are shown in green colour. Here we considered the aggressors as the nearest neighbours from the victim TSV to be tested, i.e. 1st order aggressors only chosen here as per the terminology mentioned in [6][7].

To select the particular set of TSVS which are considered as victims at each step, a 4-bit shift register is re used as proposed in [7], illustrated in fig.2 & fig.10. A Logic 1 shifts through the shift register and the corresponding outputs of shift registers are connected to selection lines of multiplexer which are dedicated to select any one of the four sets of victims at a particular instant of test. The illustration is shown in fig.10. Shift register is loaded with a binary number '1000' at the first step, so that multiplexer (coloured in red) which broadcasts the victim test patterns V to set 1 of victims is selected, and other Multiplexers (coloured in blue, orange and violet for illustration) are selected with selection input as 0, so that aggressor test pattern transition from the TPG are broadcasted accordingly to the remaining TSVs.

	J	J+1	J+2	J+3	J+4	J+5
I	⊗	⊗	⊗	⊗	⊗	⊗
I+1	⊗	⊗	⊗	⊗	⊗	⊗
I+2	⊗	⊗	⊗	⊗	⊗	⊗
I+3	⊗	⊗	⊗	⊗	⊗	⊗

Step1: Victim set = (I + P, J + P) where P=0, 2, 4...

	J	J+1	J+2	J+3	J+4	J+5
I	⊗	⊗	⊗	⊗	⊗	⊗
I+1	⊗	⊗	⊗	⊗	⊗	⊗
I+2	⊗	⊗	⊗	⊗	⊗	⊗
I+3	⊗	⊗	⊗	⊗	⊗	⊗

Step2: Victim set= [(I+1) +P, (J +P)] where P=0, 2, 4.

	J	J+1	J+2	J+3	J+4	J+5
I	⊗	⊗	⊗	⊗	⊗	⊗
I+1	⊗	⊗	⊗	⊗	⊗	⊗
I+2	⊗	⊗	⊗	⊗	⊗	⊗
I+3	⊗	⊗	⊗	⊗	⊗	⊗

Step3: Victim set= [I+P, (J+1) +P] where P=0, 2, 4…

	J	J+1	J+2	J+3	J+4	J+5
I	⊗	⊗	⊗	⊗	⊗	⊗
I+1	⊗	⊗	⊗	⊗	⊗	⊗
I+2	⊗	⊗	⊗	⊗	⊗	⊗
I+3	⊗	⊗	⊗	⊗	⊗	⊗

Step4: Victim set = [(I+1) +P, (J+1) +P] where P=0, 2, 4…

Fig1: Grouping of TSVs into four sets

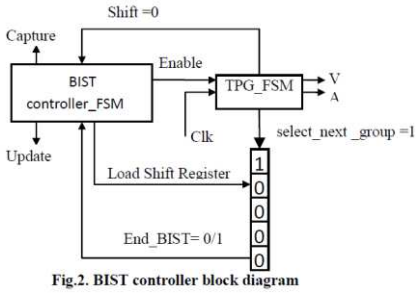

Fig.2. BIST controller block diagram

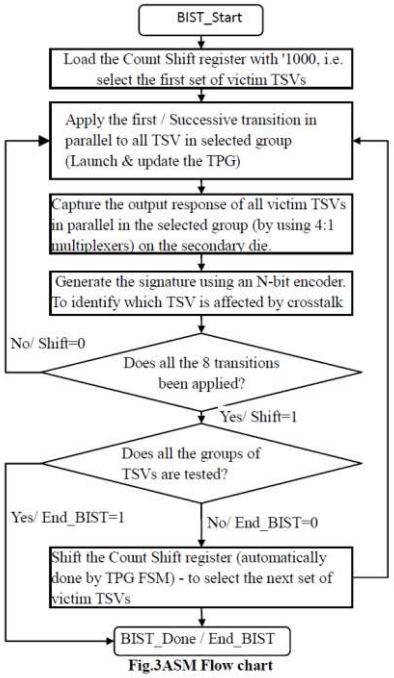

Fig.3ASM Flow chart

DESIGN OF TEST PATTERN GENERATOR:

The deterministic Maximum aggressor model based sequential test pattern generation is adopted in this design. maximum aggressor model assumes the selected victim TSVs in the possible logical states of '0' or '1' and applies the possible 0->1 or 1->0 transitions in the surrounding aggressor TSVs, to observe the glitches (positive or negative) on the victim interconnect. And also this model applies the transitions occurring both on victim TSVs and aggressor TSVs simultaneously at the same time in order to detect the crosstalk coupling faults. The table below shows the various state transitions to be applied on victim (V) and aggressor (A) TSVs to detect different types of crosstalk faults such as glitches and transition delays.

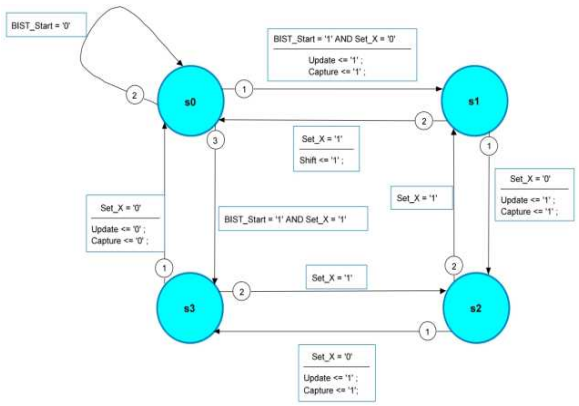

Fig.4. Finite state machine of Test pattern Generator& simulation

Set X	Present input		Next input		Fault detected
	V	A	V+	A+	
Set X=0	0	0	0	1	Positive glitch on victim
	0	1	1	0	Rise time delay
	1	0	1	1	Positive glitch
	1	1	0	0	Delayed arrival
Set X=1	0	0	1	1	Delayed arrival
	1	1	1	0	Negative glitch
	1	0	0	1	Fall time delay
	0	1	0	0	Negative glitch

Table1: Test pattern transitions to be applied

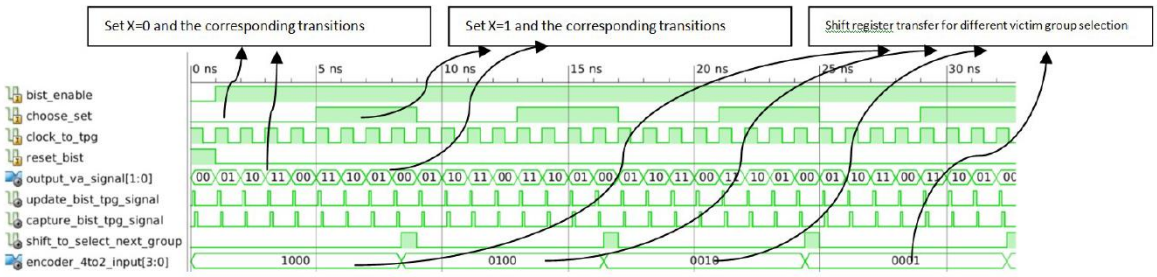

Fig.5. Simulation results of BIST and TPG shown in fig.2.

TPG will start applying the patterns after enabled by the BIST controller. By receiving the launch/update signal from the controller TPG applies the test pattern transitions sequentially at each clock cycle until the enable signal high. BIST controller broadcasts the test patterns to all the LBSCs (Launching Boundary scan cells) on primary die by broadcasting the Update control signal commonly to all LBSC cells, and captures the responses of all TSVs on secondary die by broadcasting a capture control signal to all CBSC (Receiving/Capturing Boundary scan cells) cells, as illustrated in fig.8. Later, at the receiving end on the secondary die only the outputs of Victim TSVs in the chosen group are selected in parallel by the 4:1 multiplexers, for further analysis, as illustrated in fig.12. As per our knowledge, this capturing the outputs in parallel is a novel technique proposed in this paper.

The captured outputs will be all '0's if no fault is occurred. When there is crosstalk fault in any of the selected victim TSVs the corresponding output will be '1' as the XOR output in CBSC will be '1'. A signature of these captured outputs is generated by using an encoder discussed and illustrated in fig.11, whose output indicates the location of faulty TSV in the selected group. After applying the eight transitions to the first group of victim and aggressor TSVs, the next group of TSVs have to select for applying the similar transitions to the next group.

MODIFICATION OF BOUNDARY SCAN CELL:

TSV Interconnect has to carry different signal in different functional/ Test modes

1. Functional inputs in normal functioning mode
2. Serial test data from JTAG TDI input in EXTEST Mode.
3. Test pattern inputs generated from BIST test pattern generator.

Conventional boundary scan cells or die wrapper cells which were originally designed only to switch between functional mode and serial scan mode is modified for this application, where the third mode of broadcasting the BIST-TPG Generated test patterns to the corresponding TSVs At-speed is included . Conventional IEEE 1149.1

based boundary scan cells/ IEEE 1500 based Die wrapper cells are the elements used as switch boxes, designed to carry the functional inputs in normal mode(from Die input pins into the cores on the die or out from the cores to the Die output pins) and also used to switch to test mode to serially transport the test input data (which comes from external ATE through TDI pin) serially through their scan in and scan out pins, to apply the test patterns in INTEST mode for core functional test or EXTEST mode to test the interconnects. Modification of these cells is required in order to carry the third input test patterns generated by the proposed BIST. Modified Boundary scan cell for launching the test patterns and capturing the responses named as LBSC (Launch Boundary Scan Cell) & CBSC (Capture/Receive Boundary Scan Cell) is shown in fig.6, fig.7 and the simulation outputs of these cell responses in shown in Fig 8 & Fig.9 respectively.

LBSC: Launch Boundary Scan Cell:

LBSC contains one extra multiplexer to select between serial scan inputs or inputs generated from TPG, to be launched by the Update register. Selection line of multiplexer X_select can be enabled from instruction control registers. X_select='1' defines the At-speed test mode and transmits the test patterns generated from the TPGThe designer can also use these LBSCs connected in conventional scan in-scan out serial test pattern transmission as required in EXTEST mode by selecting the X_Select signal to '0'

CBSC: Capture Boundary Scan Cell

Simillarly the other side , to observe the response on the layer2, compare the output signals with the actual test patterns applied, a similar test pattern generator has to be located in layer 2, which generates the test patterns in synchronism with the test pattern generator on layer 1. (Illustrated in fig.10). To Capture the responses, Boundary scan cells are required to compare outputs with expected patterns, capture and store them for further analysis. Boundary scan cell with compare and capture capability is shown in fig.8. The expected test patterns (generated by TPG) are compared to the actual test patterns travelled through TSV from the primary die, by using a XOR comparator as shown in the figure 7. Whenever there is a mismatch in the expected logic pattern and the actual logi c level arrived, the XOR gate output is logic 1, which is captured by the D flip flop in CBSC

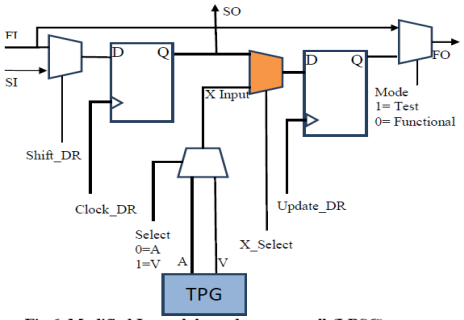

Fig.6. Modified Launch boundary scan cell (LBSC)

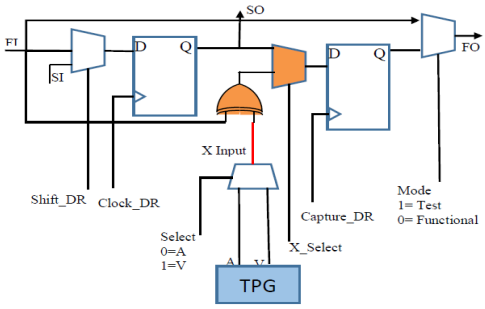

Fig.7. Modified Capture/Recieve boundary scan cell (CBSC)

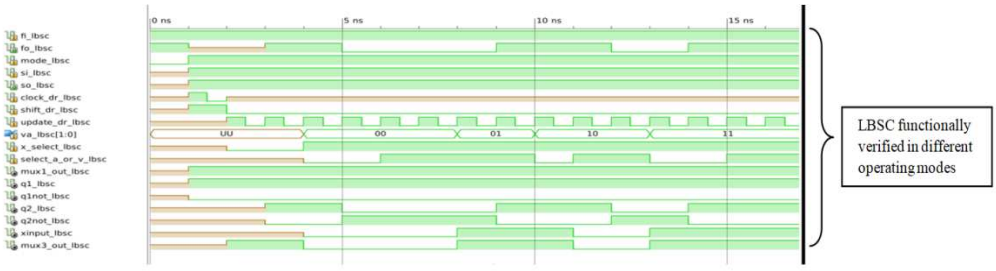

Fig.8. Simulation results of Launch boundary scan cell in functional mode and test mode

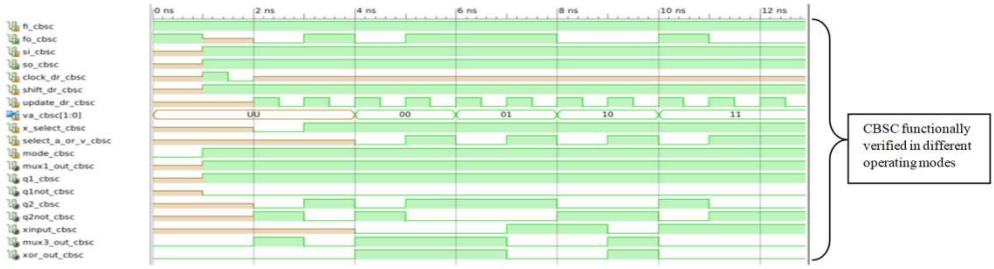

Fig.9. Simulation results of Capture boundary scan cell (CBSC) in functional mode and test mode.

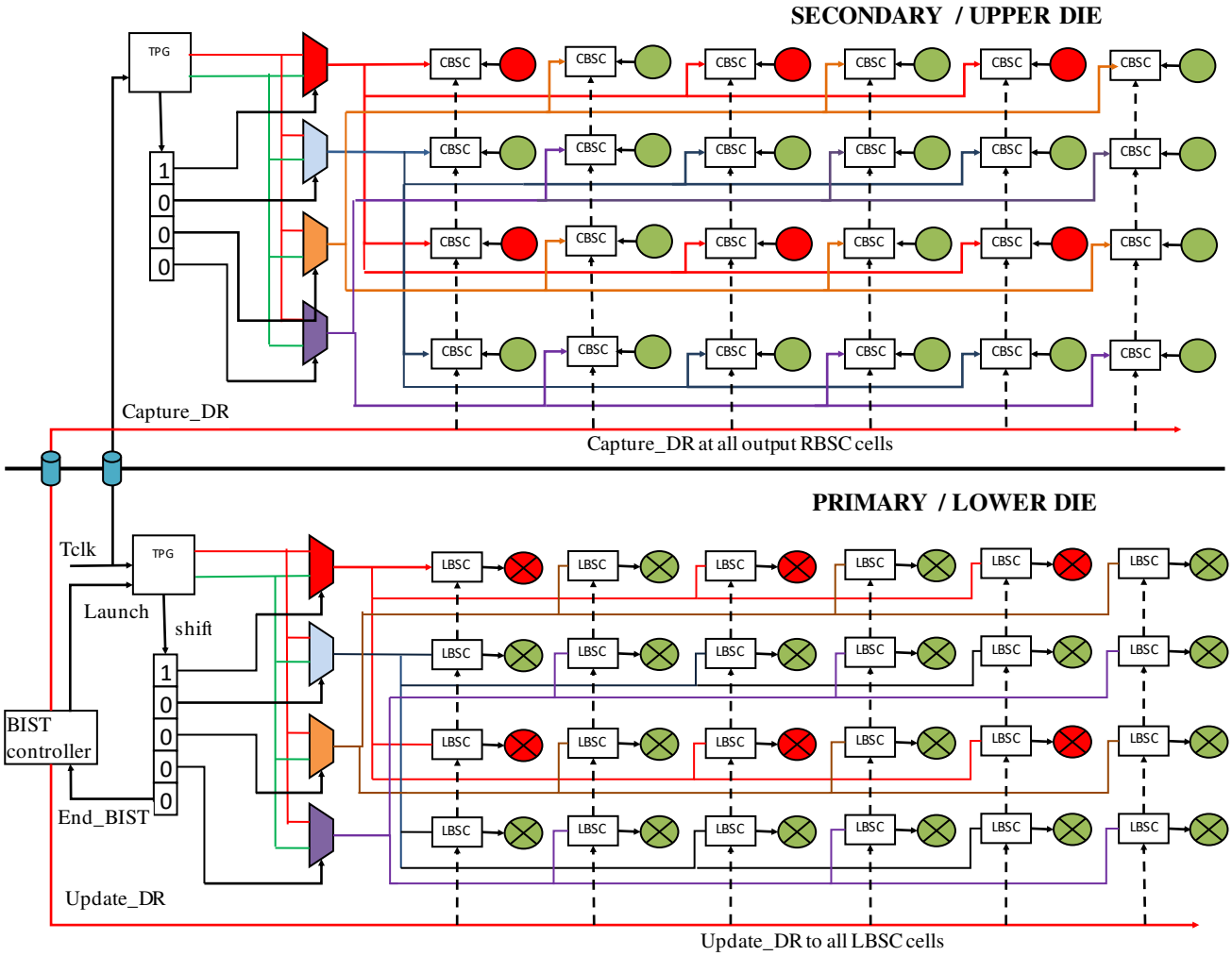

Fig.10. Illustration of parallel test pattern transition launch and capture in primary and secondary dies

OUTPUT RESPONSE ANALYSIS:

In order to achieve the parallelism in observing and capturing the response, 4 input multiplexer is used to select the particular set of Victim TSVs under test, by sending the selection signals on its selection lines. A 4:1 multiplexer used to select the outputs from four different sets of victims at four stages of test, illustrated in fig.1 and fig.11. A separate selection logic circuit (4:2 Encoder) is designed to give the inputs to 2 bit selection lines of 4:1 Multiplexer. The circuitry to generate the inputs to the selection lines of the 4:1 multiplexer is obtained by a simple combinational logic circuit (Encoder) designed from the truth table given below.

Inputs (from shift register)				Outputs		
A	B	C	D	S1	S0	
1	0	0	0	0	0	Select victim set1
0	1	0	0	0	1	Select victim set2
0	0	1	0	1	0	Select victim set3
0	0	0	1	1	1	Select victim set4

S1 = A'B' (C XOR D) **S0= A'C' (B XOR D)**

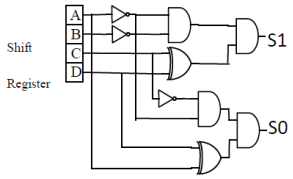

Fig.11. Combinational circuit for generating the selection inputs of 4:1 Mux

Binary value present in shift register shown in fig.2., is used to identify which set of victim outputs to be selected by the multiplexer. The Boolean equations and combinational logic circuit block (CLB) for the ab ove truth table is as shown below The outputs of the 4:1 multiplexer can be captured by the encoder to generate the signature or to identify the faulty TSV

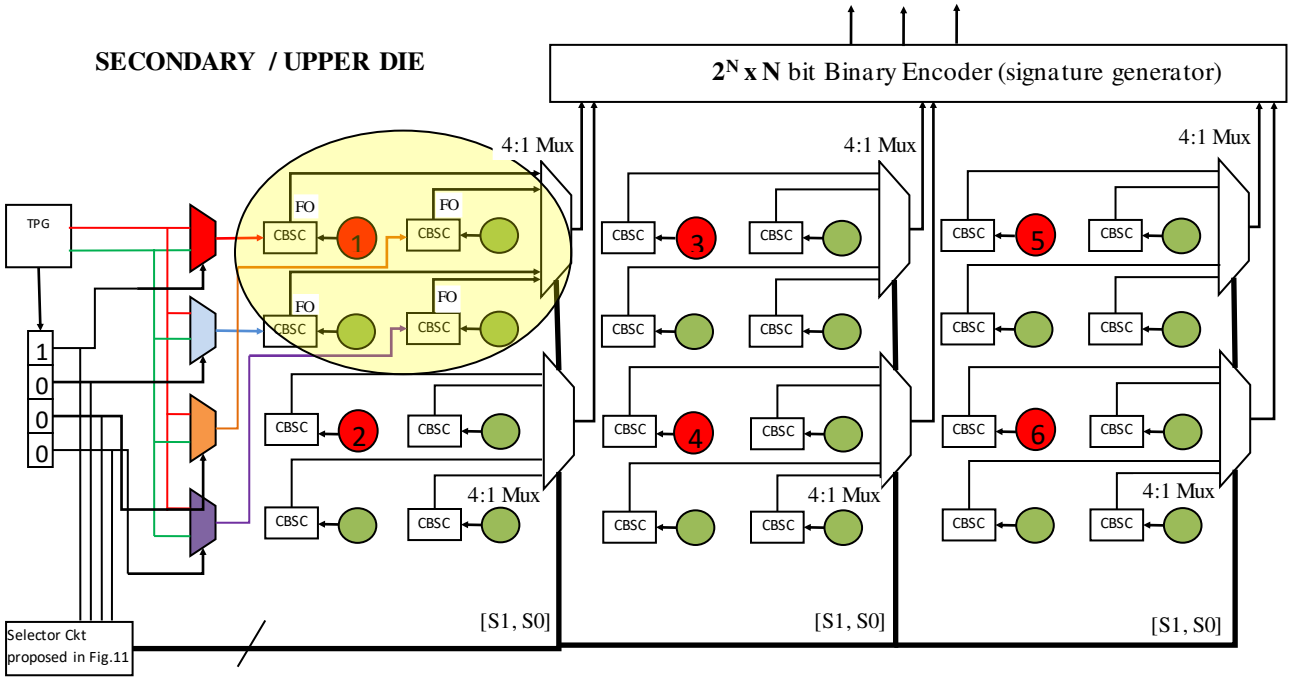

Fig.12. at speed parallel capturing mechanism of output response of group of TSVs

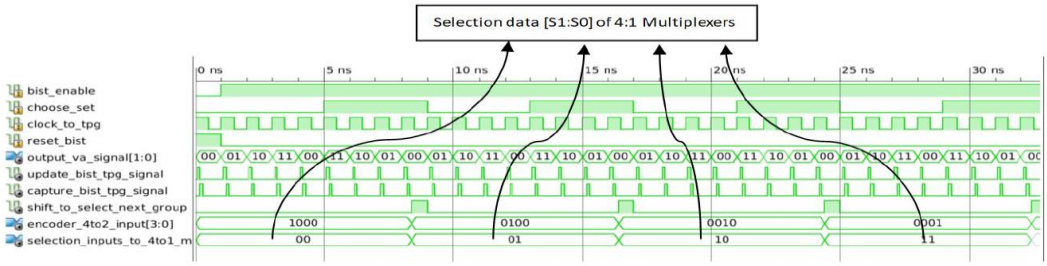

Fig.13. Over all BIST signals generated through simulations Using Xilinx simulation tools.

2^N – N BIT ENCODER AS OUTPUT RESPONSE ANALYSER / SIGNATURE GENERATOR:

The outputs of the 4:1 multiplexer can be captured by the encoder to generate the signature or to identify the faulty TSV As shown in fig 12. Outputs of selected Victim TSVs are given as inputs to the 2^N x N bit Encoder/Signature Generator which will give the exact location as TSV number which is faulty or affected by crosstalk. It is illustrated in the table 2.

The signature generated by the Encoder can be stored on the secondary die, temporarily by using a RAM and further processed for analysis, or serially shifted out through the TDO pin in the conventional manner.

Inputs								Output	Faulty TSV
0	0	0	0	0	0	0	0	000	No fault
1	0	0	0	0	0	0	0	001	TSV1
0	1	0	0	0	0	0	0	010	TSV2
0	0	1	0	0	0	0	0	011	TSV3
0	0	0	1	0	0	0	0	100	TSV4
0	0	0	0	1	0	0	0	101	TSV5
0	0	0	0	0	1	0	0	110	TSV6
0	0	0	0	0	0	1	0	111	TSV7

Table 2. Truth table 2^N – N bit Encoder

CONCLUSION:

HDL simulation of the proposed TPG, LBSC, and CBSC is done and port mapped as the flow discussed. Algorithm based BIST controller as proposed was designed to generate the control signals and port mapped to the corresponding control signals of components as proposed in the design. The proposed boundary scan cells require just two extra Multiplexers in LBSC and one Multiplexer and a XOR gate in CBSC, slight area overhead will be there due to these components. But Time complexity of parallel test is very low, as it requires 8 different transitions (8 clock cycles) per a group, and 8 x 4= 32 clock cycles to test the four different group of victims as shown in fig.1

Future work: Validation of the proposed Logic by applying the test patterns to Equivalent circuits of TSVs in SPICE Simulation tools or AMS (Analog and Mixed signal) Tools such as VHDL-AMS tools

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