A Charge Balanced Vertical Power MOSFET With Record High Balliga's Figure of Merit: Design and Investigation

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A Charge Balanced Vertical Power MOSFET With Record High Balliga's Figure of Merit: Design and Investigation

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ABSTRACT: In this work, we design and simulate a high-performance vertical power MOSFET with a charge balanced drift layer, which modulates the RON-BV relation from super quadratic to linear. The proposed device is designed with a super junction drift layer which modulates the R_{ON}-BV relation from super quadratic to linear. The proposed device has the source and channel regions isolated from the super junction drift layer. This results in a significant improvement in the performance of the proposed device in comparison to the other conventional devices, in terms of Balliga's figure of merit. A 2D TCAD simulation study reveals that the proposed device with an epitaxial layer thickness of 50μm shows an ON resistance of 3.84mΩ.cm^2 for a break down voltage of 833V, which is the lowest among the resistances reported in the previous literature at this breakdown voltage. Further, the study of charge imbalances and the capacitance analyses including the calculation of gate charge has also been done. The values of Balliga's figure of merit (FOM) calculated for all the drift thicknesses of the proposed structures are significantly outperforming the conventional super junction structures reported so far.

INDEX TERMS Power MOSFET, Balliga's figure of merit, Super junction MOS, Specific ON resistance, charge balance

I. INTRODUCTION

Power devices find applications in almost all domains with power consumption of a few watts (mobile phones and portable devices) to tens or hundreds of watts (computer) to kilo Watt (KW) or megawatt (MW) applications, such as traction for cars and trains etc [1]. The lateral configuration of power MOSFETs has reduced charging time, however, has poor packing density [2]. The trench MOSFET configuration is more popular with reduced ON resistance (Ron) and high packing density [3]. Furthermore, the most important issue with the power semiconductor devices is to improve the BV-Ron tradeoff and to overcome the silicon limit [Ron α BV2.5]. The concept of super junction formation inside a power MOSFET is reported to have the potential to break the silicon limit enabling the device to withstand high breakdown voltage simultaneously with large On-state conduction [4-8]. The super junction MOSFET or Cool MOSFET replaces the uniformly doped drift region by alternate stacks of P and N type doped regions [9]. The depletion region is formed across these thin alternate vertical pillars along with the vertical base-drift junction. In OFF state with zero gate bias, a drain bias causes the junctions to spread, causing complete depletion of P and N pillars before breakdown [10][11]. The doping and width of the p and n regions are chosen such that Wn.Nn=Wp.Np, providing charge balance among the p and n layer [12]. The triangular electric field curve due to the single junction in the conventional power MOSFET becomes flat in the super junction structure [11]. This breaks the conventional silicon limit and makes the On-state resistance a linear function of breakdown voltage. The P pillars do not contribute to the On-state conduction and the conduction current flows through the N pillar only. As the area for conduction reduces for super junction structure; it will provide a high conduction resistance compared to the structure with uniform drift doping. However, as the charge between p and n pillars is balanced in off state, the doping densities of these pillars can be increased maintaining the charge balance, which eventually will provide reduced ON resistance of the drift region without considerable breakdown voltage reduction

[13]. Various vertical trench gate structures with super junction drift layer have been reported in the literature which can sustain a high reverse voltage, but they lack considerable reduction in their specific on resistances simultaneously with the breakdown voltage, due to their high base resistance [14]-[16]. These devices are limited by the parasitic activation issue when the doping density of the base region is altered to reduce the base resistance, resulting in the decay in their breakdown performances and hence in their Balliga's figure of merit.

In this work, a novel vertical power MOSFET structure with charge balance drift region is proposed showing reduced ON resistance and a good immunity of breakdown voltage towards p-body doping variations. The simulation results have shown that the breakdown performance of the proposed device does not differ, when the p-body doping is reduced to reduce the ON resistance. This indicates that the parasitic activity is suppressed in the device (even when the doping densities of the device are customized with the highly doped drift region together with the lightly doped p-body region), resulting in a highly improved performance of the device in terms of Balliga's figure of merit.

This paper has been divided into IV sections. Section II describes the design procedure for the SJ drift layer. The novelty of the device is explained in section III, along with the other simulation results. Section IV concludes the work.

II. DESIGN PROCEDURE FOR SUPER JUNCTION DRIFT LAYER

The vertical power devices carrying voltage sustaining layer encounters a prominent limitation between its breakdown voltage and ON state resistance, which is defined by the relation [15]

$$R_{ON} = 27\ VB^2/8\mu\ \epsilon_{si}\ Ec^2$$

The electric field and mobility are not independent quantities, and their relation with the breakdown voltage is given by [8], With

$$Ec = 8.2\times10^5\ VB^{-1/5}\ (V/cm)$$
$$\mu = 710\ VB^{1/10}\ (cm^2/VS)$$
$$\epsilon_{si} = 11.7\ \epsilon$$

R_{ON} is given as,

$$R_{ON} = 8.3 \times 10^{-9}\ VB^{5/2} \quad (\Omega.cm^2)$$

The above relation shows that the ON resistance does not vary linearly with the breakdown voltage, rather with a power of 2.5. This relation is commonly known as the silicon limit.[11] The silicon limit considers the drift resistance to be the only component of ON resistance, and hence the actual resistance at a particular breakdown voltage is higher than the ideal silicon limit at that voltage. One of the solutions to reduce the ON resistance of a device below the silicon limit is the use of super junction structures. In a super junction structure, two junctions are formed. One junction is formed in vertical direction between p-base and n drift region. The other one is formed in lateral direction between the N and P pillars of the drift region. The drift region charge is balanced by oppositely doped p and n pillars of same width and doping. When a reverse voltage is applied at the drain end in OFF state, the reverse bias across the p/n pillars allows the depletion region to extend laterally till they merge together. Hence, in the OFF state, a uniform depletion region is formed in the entire drift region. The vertical p-base / n-drift junction thus faces a uniform depletion region for the entire drift region thickness, with all of the drift region charge being balanced in one direction only(x-direction). According to Poisson's equation [8]

$$\delta Ex/\delta x + \delta Ey/\delta y = \rho/\varepsilon$$

The super junction allows the junction charge to be spread in one dimension only, making the electric field gradient in the other direction ideally equal to zero. i.e.,

$$\delta Ex/\delta x = \rho/\varepsilon \text{ and } \delta Ey/\delta y = 0$$

Zero field gradient means the electric field is constant throughout the Y direction. This reduces the electric field peak at the vertical junction and hence the junction can sustain a higher reverse voltage before reaching the critical electric field and the breakdown of the device.

In this section, an analytical method for the design of a super junction power MOSFET is given. The cross section of the proposed BGP-SJMOS is given in figure1. Out of the possible variations in the design of a simple super junction structure, Figure 1 summarizes a general design rule given by [14]. The flow chart in Figure 1 gives the relationship among the dimensions, doping concentration and the resistance of the drift region of a super junction MOSFET, assuming a uniform doping of both the n and p pillars of the drift region. The flow chart shows the steps for the design of a super junction drift region in two possible ways. In the first condition where the device dimensions are to be calculated for a desired breakdown voltage, the designer also has to assume a certain value for f (geometric factor). f is a constant which is proportional to the ratio of cell pitch and epitaxial thickness. The value of f can be approximated to the equation of step3 with a condition if tepi/2Cp > 1[14]. The value of f is desired to be much less than one, preferably below 0.3, while a major deviation in the simulated results is observed as f reaches unity [15]. Therefore, for a particular f, the design will

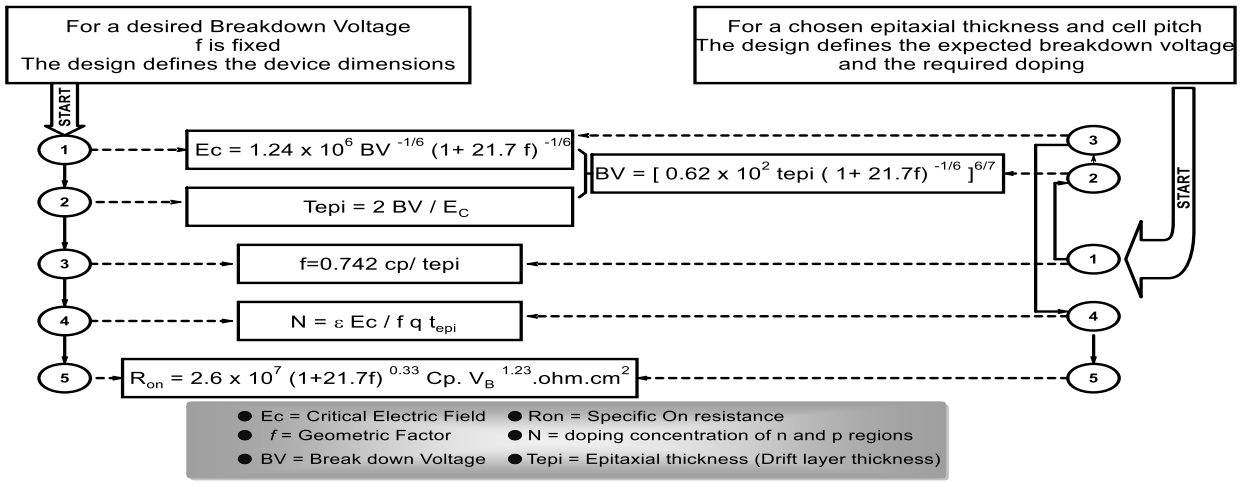

Figure 1: Flow chart for the design of super junction drift layer for different design conditions.

start by calculating the critical electric field corresponding to the desired breakdown voltage followed by the calculation of required epitaxial thickness and cell pitch given by step 2 and 3. The uniform doping required for the n and p pillars of the drift region can then be calculated using 4. Finally, the expected specific ON resistance corresponding to the desired breakdown can be calculated using 5. The second design condition in which the device dimensions i.e. the cell pitch and epitaxial thickness is fixed, and it is required to calculate the expected breakdown voltage and its corresponding specific ON resistance. In that case, the design starts by calculating the value of f, followed by the expected breakdown voltage and then the corresponding critical eclectic field. This will be followed by finding the desired doping and Ron of the device.

Figure 2 shows the cross section of the proposed dual buried gates super junction power MOSFET called BGP-SJMOS structure. The thickness of the drift layer labeled as tepi is large compared to the other regions of the device and is varied during the simulations. Considering the design procedure discussed in figure1, a simple procedure for the design of BGP-SJMOS has been adapted, for four different drift regions and with the same cell pitch of 3 µm. The values for the critical electric field, Specific On resistance and break down voltage corresponding to a specific drift thickness have been calculated analytically and are reported in table1. The doping of p and n pillars related to particular device geometry are also set during the simulations and are also mentioned in the table1.

Table1 :SJ layer used for BGP-SJMOS

A= Analytical Result S= Simulated Result

Tepi µm	**f**	**Breakdown Voltage (Volts)** A	S	**Ron (m.Ω.cm²)** A	S	**Ec (V/cm) X 10⁵**	**N (/ cm³) X 10¹⁶**
20	**0.055**	**400.65**	**366.5**	**0.8036**	**1.51**	**4.0076**	**2.354**
30	**0.037**	**590.33**	**524**	**1.213**	**2.26**	**3.88**	**1.2133**
40	**0.0278**	**766.35**	**676.5**	**2.62**	**3.06**	**3.788**	**2.2**
50	**0.022**	**929.78**	**833**	**1.98**	**3.84**	**3.719**	**2.185**

III. SIMULATION RESULTS AND DISCUSSION

In this work, we design and simulate a high performance dual buried gates super junction MOSFET (BGP-SJMOS), as shown in Figure 2. The proposed device uses two laterally aligned poly silicon buried gates, along with the super junction drift layer consisting of a single n-type doped silicon column sandwiched between two P doped silicon columns each with a width equal to the half of the n column width. The drift region in the proposed structure is located below the gates while the source and channel regions are located above the gates. The gap between the

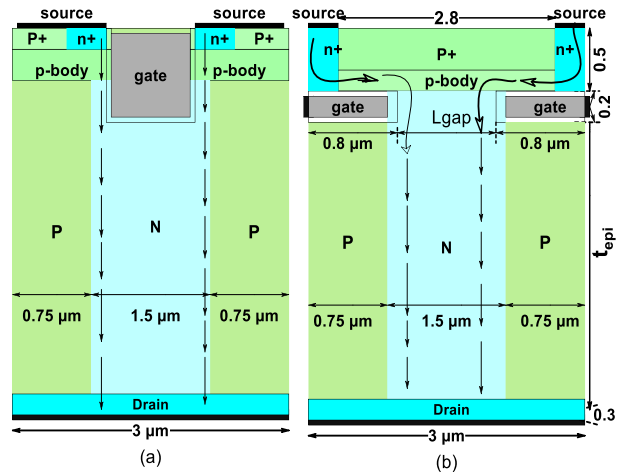

Figure 2: cross section of the (a) conventional trench gate super junction MOSFET and (b) proposed dual buried gates super junction structure (BGP-SJMOS), with same cell pitch. All the dimensions of the figure are in micrometer with the black arrows showing the current conduction path.

two gates is the only open area that connects the upper region of the structure with the drift region. The junction that is formed at the p-body / n-drift interface plays a very

important role in the working of the device. The doping concentration of the p-body region requires to be low so as to get a low ON resistance. But, if the channel region is in direct contact with the drift region, as is present in the conventional trench gate super junction structure, a low channel doping will extend the depletion region more inside the channel region that may disturb its threshold voltage. Besides, an even more dangerous situation occurs in reverse biased condition, where this depletion region extends and get merged with the source region in the conventional structure. This causes a premature breakdown of the device at lower reverse voltages. The risk of parasitic n-p-n activation also becomes significant. As the junctions formed at the source-body and the drift-body interfaces are in different directions in the proposed device, they will not merge by doping variations, causing a sharp and better breakdown performance.

To prove this, we have simulated the conventional trench gate super junction MOSFET also along with the proposed SBGP-SJMOS device. We have shown the breakdown voltage variations with the variation in p-body doping concentration. It can be seen in figure 3(a) that there is a sudden declination in the breakdown strength of the conventional device when the p-body doping is reduced below 5e15 /cm^3. This is because of the junction extension and the parasitic BJT activation effect stated above. The variation of breakdown voltage with p-body doping concentration for the conventional and the proposed devices are shown in figure 3(a). The graph shows that the p body doping variation does not degrade the breakdown performance of the proposed device, as the source body and drift body junctions are in different directions giving a reduced parasitic n-p-n effect. Whereas the conventional

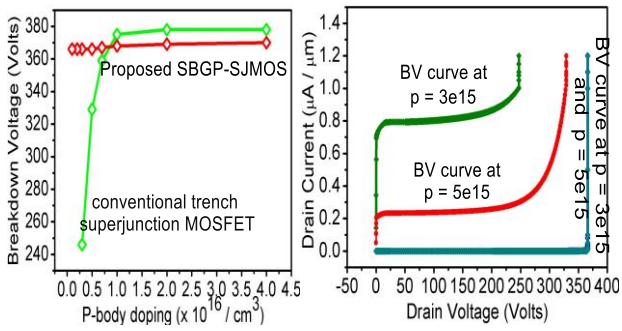

Figure3(a): variation of the breakdown voltage with the variation in P-body doping in the conventional and the proposed super junction devices. (b) breakdown voltage curves for two different p-body doping concentrations at which the BJT activation occurs, resulting in the reduction of breakdown voltage. The curved breakdown characteristics of the conventional device in contrast to the sharp breakdown characteristics of the proposed device can also be seen.

device shows a sharp performance decay. The breakdown curves for two different values of p-body doping concentration, where the performance decreases sharply are also shown in figure3(b). It can clearly be seen from the breakdown curves that the proposed device provides a sharp breakdown curve (indicating breakdown of the p-body / n- drift junction only), while a curved breakdown characteristic indicating premature breakdown can be seen for the conventional device, marked red and green in fig 3(b).

The proposed BGP-SJMOS has been designed for four different values of breakdown voltages, showing very low values of specific ON resistances, which are also quite close to the expected analytical values at those breakdown voltages. The simulation results show that the proposed device has as low as 1.51m.Ω.cm^2 resistance at a breakdown voltage of 367V, making the Balliga's figure of merit to be 88.89MW/cm^2. The values of Balliga's figure of merit (FOM) calculated for all the four drift thicknesses of the proposed BGP-SJMOS structures are very high outperforming the other reported super junction structures as well as recently reported SBGPMOS [16] also. The same performance analysis has been benchmarked along with the silicon limit line in this paper. In addition, the proposed device also shows reduced gate charge in comparison to the conventional trench super junction structure, indicating better switching performance. Two dimensional (2D) simulations of the proposed SBGP-SJMOS have been performed using Atlas Device simulator. Different models incorporated during the simulations include the field dependent mobility (FLDMOB), impact ionization model (IMPACT SELB), the concentration dependent mobility (CONMOB) model, Auger recombination (AUGER) model, bandgap narrowing (BGN) and concentration dependent lifetime model (CONSRH).

A. Input, Output and Breakdown Voltage Characteristics

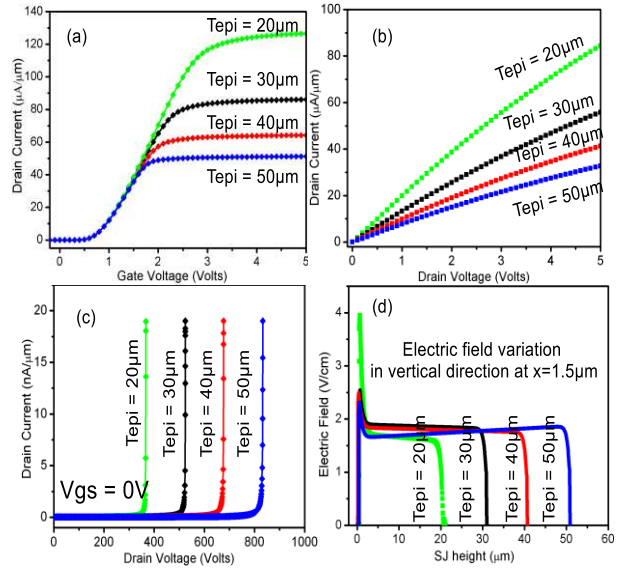

Figure4: (a) I-V characteristics of the proposed super junction structure for different values of drift thickness. (b). output characteristics for varying drift thickness at Vgs=0V, (c) corresponding breakdown curves. (d). Electric field profile for increasing values of drift layer thickness

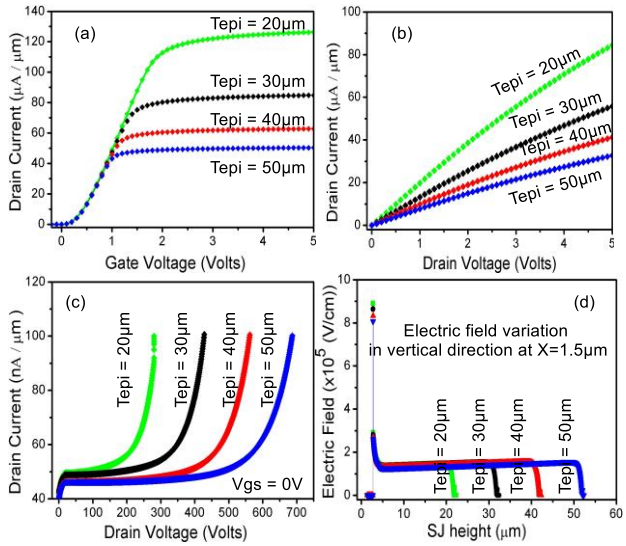

Figure5: (a) I-V characteristics of the conventional trench gate super junction structure for different values of drift thickness. (b). output characteristics for varying drift thickness at Vgs=0V, (c) corresponding breakdown curves. (d). Electric field profile for increasing values of drift layer thickness

The transfer characteristic of the proposed buried gate super junction MOSFET (BGP-SJMOS) with varying epitaxial thickness is shown in figure 4a. The graph shows a reduction in ON current with increasing epitaxial thickness owing to the corresponding increase in current conduction path. Figure 4b shows the output characteristic curves for increasing values of epitaxial thickness. All the curves are taken for Vgs=10V. In OFF state (Vgs=0), the reverse voltage applied at the drain end causes the two-dimensional depletion of the drift layer which lowers the field peak at drift/base junction, thus achieving a high breakdown strength of the proposed BGP-SMOS. The breakdown voltage thus becomes a function of drift layer thickness which increases if the thickness is increased. Figure 4c shows the breakdown characteristic of the device for increasing values of epitaxial thickness. The electric field profile corresponding to different epitaxial thickness is shown in figure4d, which is taken by drawing a vertical cutline at X=1.5µm. The graph shows a uniform electric field throughout the drift region, for each value of drift thickness, which eventually resulted in reduced field peaks at one junction. It can also be seen from the graph that the magnitude of uniform electric field is same for all the values of drift thickness, concluding that the breakdown voltage is proportional to the epitaxial thickness. Figure 5 shows the similar performance curves of the conventional trench gate power MOSFET structure for comparison with the proposed device. By comparing the curves of figure 4 and fig 5, it can be seen that both the proposed and the conventional structures possess the same amount of ON current and resistance in the ON state, but differ widely in the OFF-state performance, as shown in figure 4c and 5c.

The ON current of both the structures is same because of the same source, drift and drain doping and drift thickness. But, as the effect of parasitic npn transistor is low in the proposed device, it can sustain a higher reverse voltage without breakdown. On the other hand, the breakdown curves of figure 5(c) show the occurrence of premature breakdown where the breakdown occurs before the desired value because the drift-base junction reaches the source end at lower voltages. As the drift-body junction formed in the proposed device is not aligned with the source region, the depletion region will never reach the source region and hence the possibility of premature breakdown is eliminated, which is clearly visible in the breakdown characteristic curves of the proposed device. A huge improvement in the breakdown voltages is achieved over the conventional one for all the drift layer thickness. The values of the breakdown voltages and specific ON resistances extracted from the curves of figure4 are also listed in table1. It can be observed from table1 that there is a difference between the analytical and simulated values of ON resistance of the proposed super junction device. This is due to the fact that the design of the super junction drift layer gives the value of the drift region resistance only, while the one extracted from the simulations is the total resistance of the device. Hence the ON resistance values extracted from the simulations are higher than the analytical values.

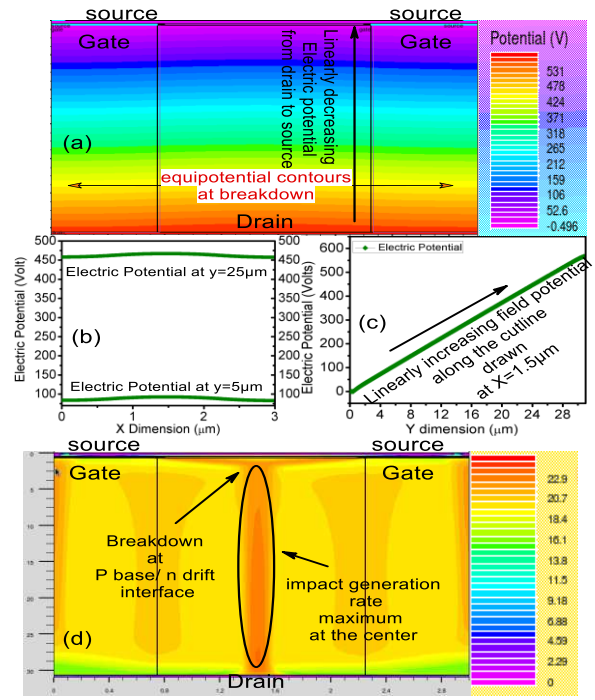

Figure 6: (a) Uniform distribution of potential contours in the super junction drift region, (b) Uniform distribution of electric potential lines laterally in the drift region which is taken by drawing a lateral cut line at y=5µm and y=25µm respectively (c) vertical variation of electric potential inside the drift region taken at x=1.5µm, (d) the distribution of impact generation rate inside the super junction drift region before breakdown.

Figure 6a shows the uniform distribution of potential contours in the drift region of the device at breakdown. This indicates that the device holds a uniform electric potential before breakdown which is highest in magnitude at the drain end. This occurs because of the fact that the reverse bias is applied at the drain end, which will provide a gradual reduction of electric potential from drain to source. A horizontal cutline drawn at y=5µm and y=25µm shows the potential lines which are almost linear in the lateral direction with different magnitudes as shown in fig 6b. A vertical cutline is also drawn at the center of the two buried gates that shows linearly varying field potential in the vertical direction as shown in figure6c. The linear variation of electric potential in the vertical direction is because of the uniform electric field in the same direction at the time the drift region is in complete depletion, with the n pillar charge being balanced by the p pillars. Figure 6d shows the 2D image of the impact ionization rate in the device at breakdown.

B. CHARGE IMBALANCE

In the design of a super junction drift region, the doping of both the pillars is taken to be of same magnitude. However, it is a tedious task to achieve a perfectly equal doping of both the pillars during fabrication, resulting in charge imbalance between the pillars, and thus a reduction in the expected breakdown voltage of the device [17]. It is expected that the doping can be controlled within a deviation range of±10% from the nominal value [18]. For that reason, the simulations are also performed for the charge imbalance situation. The charge imbalance is calculated as (N-P/N) x100% [19]. Where 'N' is the nominal value of the doping concentration.

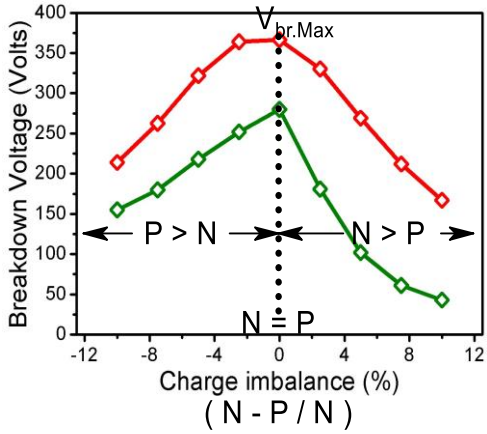

Figure 7: sensitivity of breakdown voltage for unequal n and p pillar charges. The red curve shows variations of the proposed device while the green one is for the conventional device.

A positive value of charge imbalance indicates N region charge in excess of the P region whereas the negative value indicates P region charge in excess of N. Figure7 shows the variation of breakdown voltage for unequal doping conditions with the charge imbalance varying from -10% to +10%. The breakdown voltage is maximum with equal doping condition and is denoted as Vbr.max in the graph. The value of breakdown voltage declines for both the unequal doping conditions. The breakdown sensitivity with unequal p/n doping for the conventional device is also shown in figure 7. It can be seen that the proposed device marked red shows a lesser decay with unequal doping as compared to the conventional device marked green. Further, the graph shows a greater reduction of breakdown voltage for positive charge imbalance values. A detailed study of the drift layer of BGP-SJMOS under the two charge imbalance conditions is discussed below.

For a p-n junction with equal p and n doping, the depletion region formed will be of equal width on both sides of the junction. The electric field developed will have a peak at the junction which reduces gradually till the junction terminates. The field peak increases if the doping of any one of the regions or of both the regions increases. In the proposed super junction BGP-SJMOS, three junctions are formed inside the structure. One junction is formed at the P base/ n drift interface, second at the p pillar /n pillar interface and the third at the n+ drain/p pillar interface. For equal doping of p and n pillars, a uniform depletion region is formed between these pillars which increase with the increase in reverse bias resulting in the complete depletion of both the pillars. This complete (and equal) depletion reduces the electric field peaks at the p-n pillar junction. At this point, the base drift junction encounters a uniform depletion region throughout the drift layer, which allows higher reverse voltage to be applied before breakdown. The breakdown voltage will be maximum in this case and is denoted as VBR.max. Consider the case when the doping of n pillar is higher than the p pillar (n>p). Since

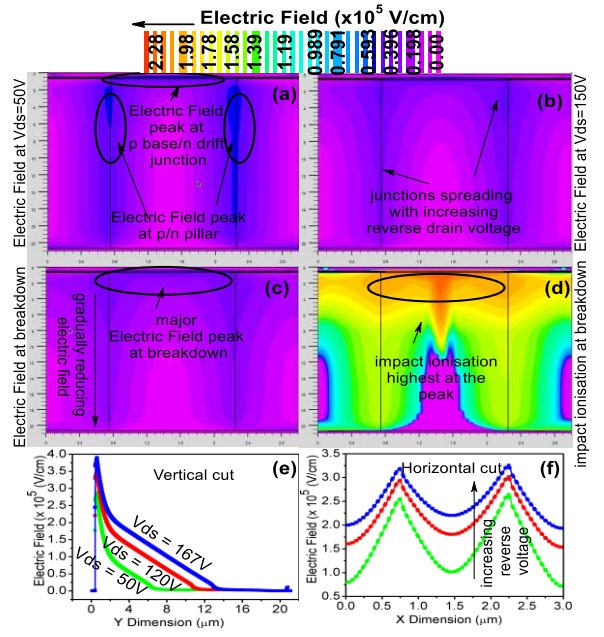

Figure8: (a)(b)(c) Electric field contours at different values of reverse drain voltage for the condition when N>P. (d) impact ionization contours at breakdown. (e)The electric field profile which is taken by drawing a vertical cutline in the middle of the drift layer at x=1.5µm.(f) The lateral electric field profile taken by drawing a cutline at y=15µm.

the doping is not equal, the junction formed between pillars will not have equal depletion widths in both the pillars. This will cause a larger junction width on p side and lesser on the n side. Unequal doping also slightly increases the field peak at the junction. One junction at the drift base side will also form unequal junction width with lesser on the n side and more on the p side. This vertical junction along with the lateral n/p pillar junction forms the wider depletion region near the gate. The field peak is also maximum at the drift base junction because of high n doping. The increase in reverse voltage will then cause the junction to extend towards the drain. Figure8 shows the electric field contour at different values of reverse drain voltages. For lower drain values, the figure shows dense electric field contours which gradually spreads in the downward direction and reaches the drain end before breakdown. Once the junction reaches the drain end, further application of reverse voltage increases the drift velocity of minority carriers inside the junction, which in turn causes an increase in kinetic energy of the carriers and hence in impact generation rate, which finally causes the breakdown of P base/n drift junction. As the n region doping is more than the p region doping, there will be some undoped region remain in the middle of the n layer. The reverse drain voltage at which the breakdown occurs is lesser than VBR.max because of the increased electric field peak at base/drift junction which reaches the critical field at early reverse voltage.

On the other hand, consider the case when the doping of p pillar is higher than the n pillar (P>N). In this condition, an unequal depletion region is formed which is wider on the n

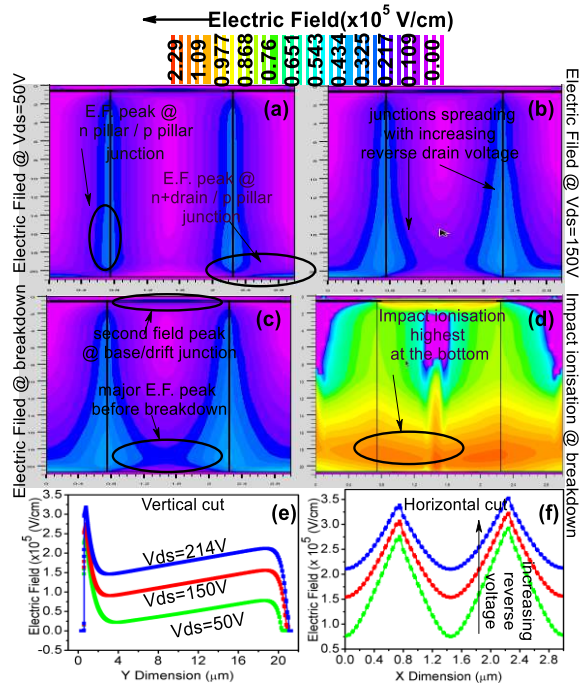

Figure9: (a)(b)(c) Electric field contours at different values of reverse drain voltage for the condition when P>N. (d) impact ionization contours at breakdown. (e) The electric field profile which is taken by drawing a vertical cutline in the middle of the drift layer at x=1.5µm. (f) The lateral electric field profile taken by drawing a cutline at y=15µm.

pillar side, having peak electric field at the junction (see Figure 9). The wider undepleted p pillar region will form another junction at the n+ drain/p pillar interface with field peak higher than the one for n>p case. These two junctions form a wider depletion region near the drain end at lower drain voltages. An increase in reverse voltage will cause the two depletion regions to merge, which then spreads in the upward direction before reaching the upper end of the drift region. It can be seen from the figure that the merging of junctions near the drain end at higher drain voltages forms an electric field peak at the bottom of the drift region. This accounts for high impact generation rate to occur at lower side of the drift region resulting in breakdown of the junction. The impact generation rate higher at the drain end can also be seen in figure 9d. It can also be seen from the graph in figure 9e, that the critical field in this case is lower than the one with N>P situation, thus providing a lesser reduction in breakdown voltage from VBR.max.

C. BENCHMARKING

Owing to the BV-Ron trade-off that exists in power MOSFETs, it is favorable to compare their performances

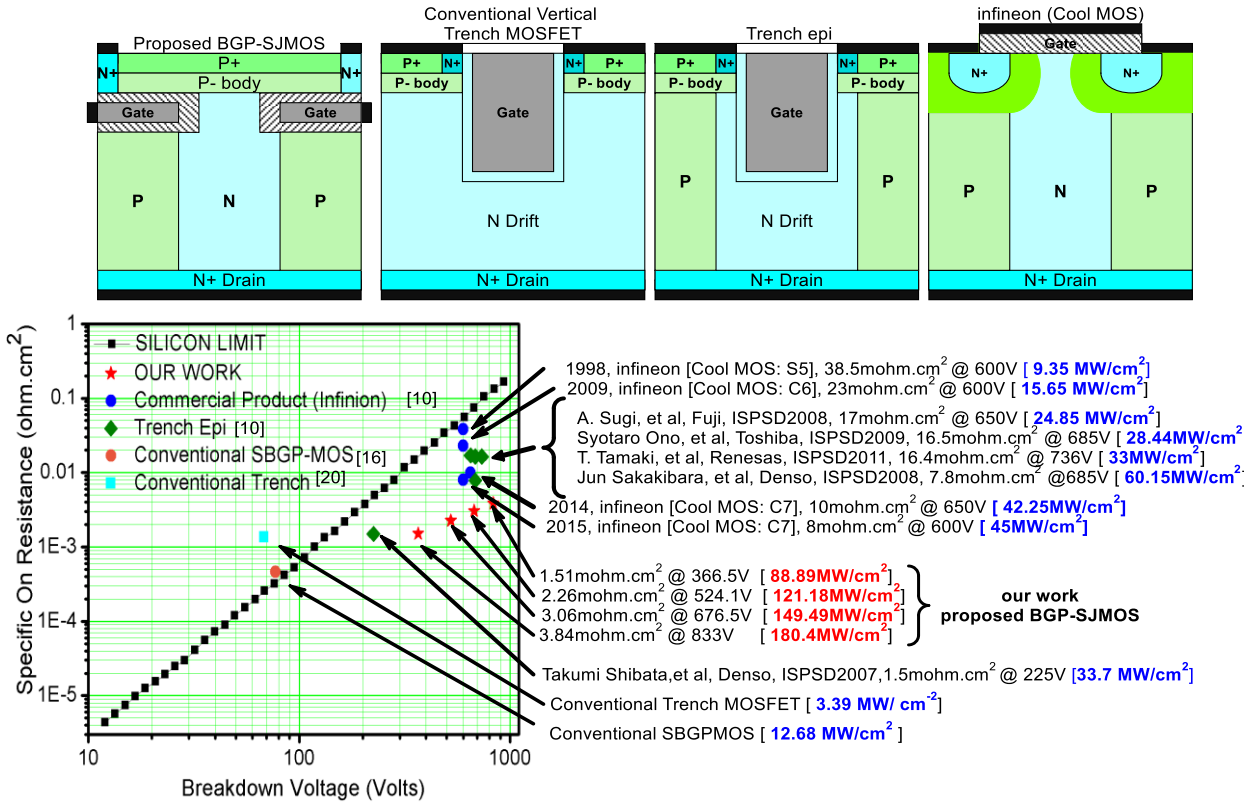

Figure 10: Specific ON resistance versus BV with the ideal silicon limit line, the reported structures in the literature [10],and the proposed super junction structure with different breakdown voltages

on the basis of Balliga's figure of merits (FOM) rather than comparing them separately. Thus, in Figure 10, we have compared the performance of the proposed BGP-SJMOS in terms of Balliga's figure of merit, with some of the results reported in the literature [10]. All the values are also plotted against the silicon limit line. The corresponding values of Balliga's figure of merit are also mentioned against each data. In the present work, the proposed structure is designed for four different values of breakdown voltages that are 367V, 524V, 676V and 833V. The corresponding values of specific on resistances are 1.51, 2.26, 3.06 and 3.84mΩ.cm^2 respectively. The graph shows that the proposed device offers the lowest ON resistances as compared to the other devices in the literature, at all of these breakdown voltages. The graph also indicates that the proposed device offers the FOM value as high as 180.4MW/cm^2 for a breakdown voltage of 833V, which is almost three times the value achieved by the other reported values in the graph.

D. CAPACITANCE ANALYSIS

Figure 11 shows the variations of gate to source capacitance (Cgs), gate to drain capacitance (Cgd) and drain to source capacitance (Cds) as a function of drain to source voltage (Vds). All the three variations are taken at zero gate to source voltage. The graph shows that the depletion regions and hence the capacitance associated with the p/n pillars of a super junction structure are highly sensitive to Vds, especially in its lower range. This is due to the fact that for lower values of Vds, both, the small depletion regions formed across the p/n pillars and the larger undepleted surface separating them, will provide higher output capacitance. The depletion regions extend laterally with Vds resulting in reduction of output capacitances (Cgd and Cds) till the complete depletion of drift region. Further increase in reverse voltage will have no impact on the output capacitances. In addition to that, the capacitance variation of the conventional super junction trench MOSFET is also performed and is plotted in the graph for comparison. The graph shows reduced gate drain capacitance of the proposed SBGP-SJMOS because of the increased distance between gate and drain. The graph also shows a huge reduction in parasitic Cds of the proposed device. This is due to the fact that the proposed device carries source and drain on opposite sides of the gate thus minimizing the coupling effect, and a great reduction in Cds of the proposed structure is achieved. In addition to this, the gate charge of the proposed BGP-SJMOS is also calculated using its gate charging curve shown in figure 12. The gate charge of a power device indicates the amount of drive power ((Pg) required at some specific frequency [21]

$$P_g = Q_g . V_{gs} . f_{sw}$$

The values of the total gate charge Qg for the conventional SBGPMOS and proposed BGP-SJMOS extracted from the graph are 106pc and 83pc respectively and are shown in the figure 12.

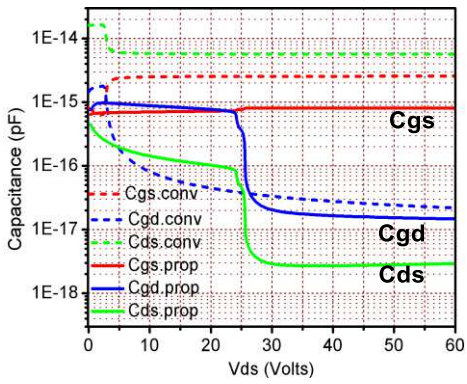

Figure 11: Comparison of Cgd, Cgs and Cds of the proposed GBP-SMOS and the conventional superjunction trench MOSFET, with increasing drain to source voltage (Vds).

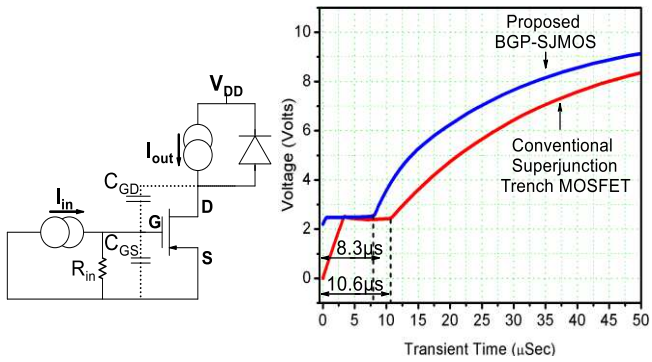

Figure 12: Gate charging transient curve for the proposed super junction MOSFET device with the circuit used to simulate the same

IV. PROPOSED FABRICATION FLOW

A process flow for the fabrication of the proposed device is given in Figure 13. We believe that the device is not easy to fabricate, but the device dimensions are optimized with values which are already reported in the previous fabricated devices.

The first step can be the epitaxial growth of a lightly doped n-region on a highly doped substrate, as shown in Figure 13(a). A thermal oxide can then be patterned for the hard mask to mark the trenches, followed by selective etching as shown in Figure 13(b)[22]. Trenches are filled with P-type epitaxial layers followed by chemical mechanical polishing to flatten the surface as shown in figure 13(c). This way a super junction drift region gets created [22][23]. The fabrication of buried gates over the drift layer includes the oxide and the polysilicon growth. A possible set of steps to form the buried gates is mentioned, which includes the growth of oxide layer over the super junction drift layer [24] followed by the growth of 100nm polysilicon layer over it using LPCVD [25], as shown in figure 13(d). Selective patterning and etching can then be done to create a trench window, as shown in figure 2(e). A 50nm oxide layer can then be grown over the polysilicon layer and the inner walls of the trench using thermal oxidation., as has been done in [26][27][28], as illustrated in figure 2(f). A similar fabricated structure with as low as 10nm oxide layer on top of the 50nm polysilicon layer is already reported in the literature [25]. Selective oxide etching can then be done to remove the bottom oxide which will open a seed window, figure 13(g), for further epitaxial growth of silicon over oxide, as shown in figure 13(h) [29]. Finally, the n+ source, p and p+ implantation can be done as done in [26]-[27], as shown in figure 13(i). The contacts from side gate can be formed similar to the gate electrodes reported in the fabrication given by [27]. This way, there is a possibility that the proposed device can be fabricated.

V. CONCLUSION

A new dual buried gate super junction power MOSFET has been designed and analyzed. The drift region of the proposed device is composed of alternate p and n type doped regions, commonly known as the super junction drift region. The design procedure of a super junction drift layer is also mentioned with two different conditions. For four different values of drift region thickness, the analytical values of the breakdown voltage and ON resistance have been calculated and are compared with the values obtained from the results obtained by simulating the super junction dual gate structure with varying drift thickness. The performance of the proposed structure has been further compared with the structures reported in the literature in terms of their figure of merits and are plotted on the silicon limit line. Further, a detailed analysis of the effect of charge imbalances on the breakdown of the proposed BGP-SJMOS has been performed. Moreover, the transient analysis of the proposed super junction device in terms of gate charge is also performed.

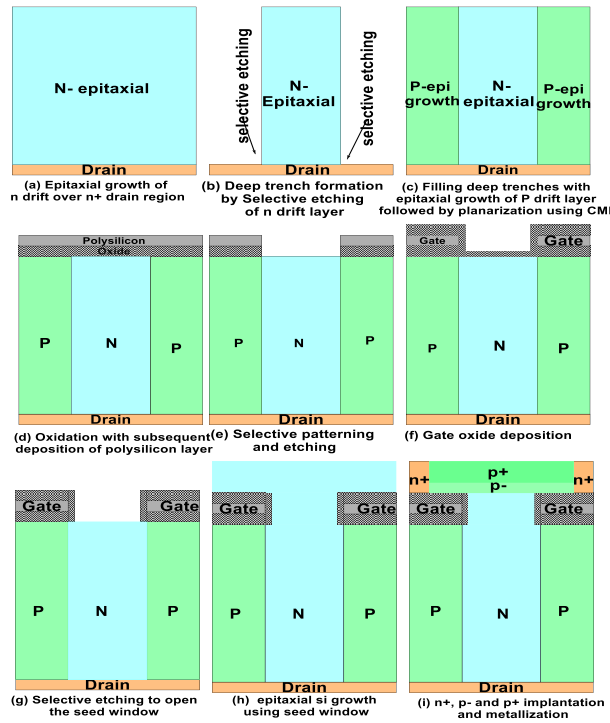

Figure 13: Process flow for the proposed device

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Consent to participate: NA
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Figures

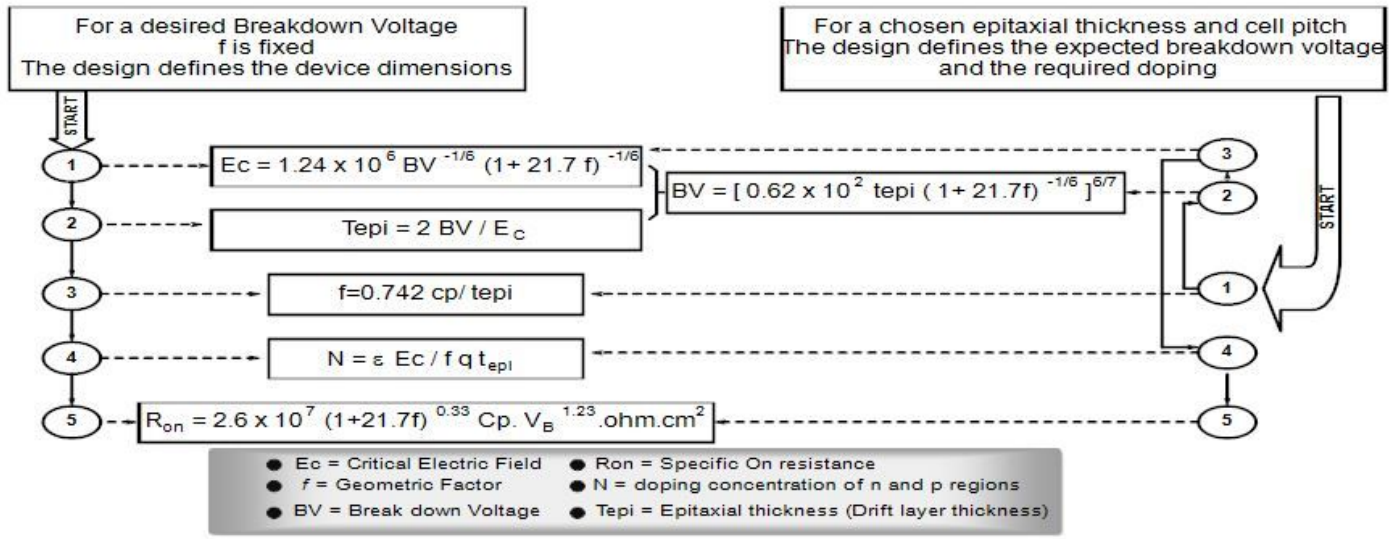

Figure 1

Flow chart for the design of super junction drift layer for different design conditions.

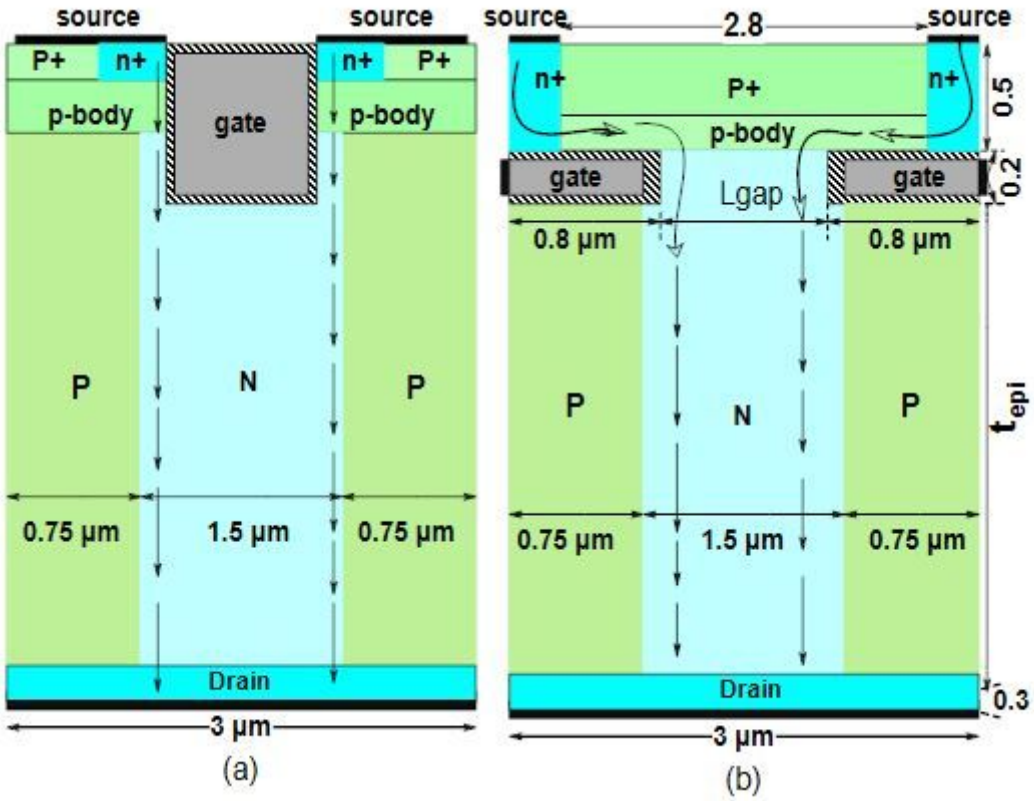

Figure 2

cross section of the (a) conventional trench gate super junction MOSFET and (b) proposed dual buried gates super junction structure (BGP-SJMOS), with same cell pitch. All the dimensions of the figure are in

micrometer with the black arrows showing the current conduction path.

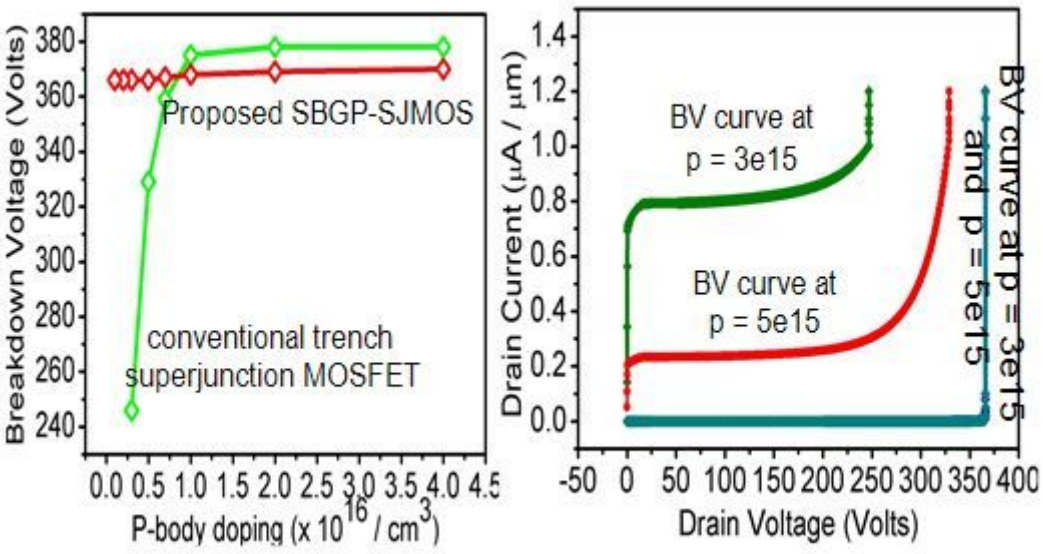

Figure 3

(a): variation of the breakdown voltage with the variation in P-body doping in the conventional and the proposed super junction devices. (b) breakdown voltage curves for two different p-body doping concentrations at which the BJT activation occurs, resulting in the reduction of breakdown voltage. The curved breakdown characteristics of the conventional device in contrast to the sharp breakdown characteristics of the proposed device can also be seen.

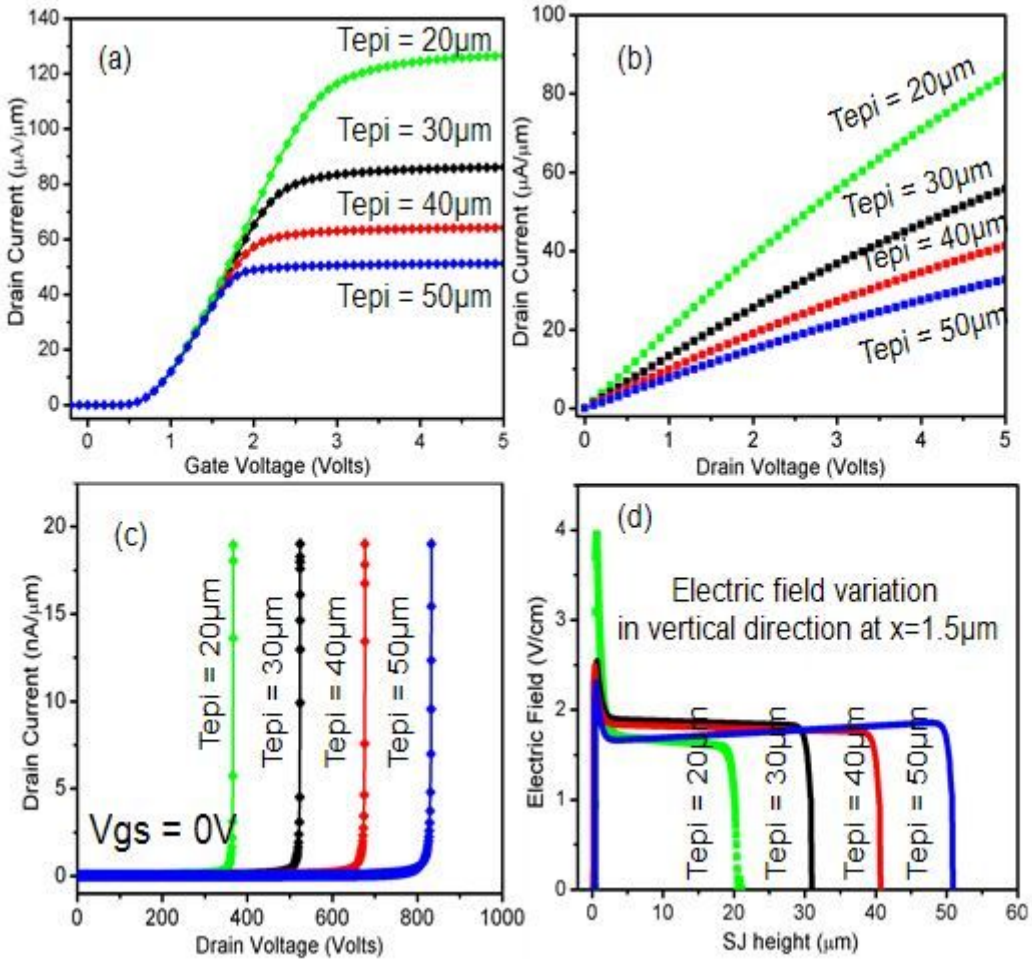

Figure 4

(a) I-V characteristics of the proposed super junction structure for different values of drift thickness. (b). output characteristics for varying drift thickness at Vgs=0V, (c) corresponding breakdown curves. (d). Electric field profile for increasing values of drift layer thickness

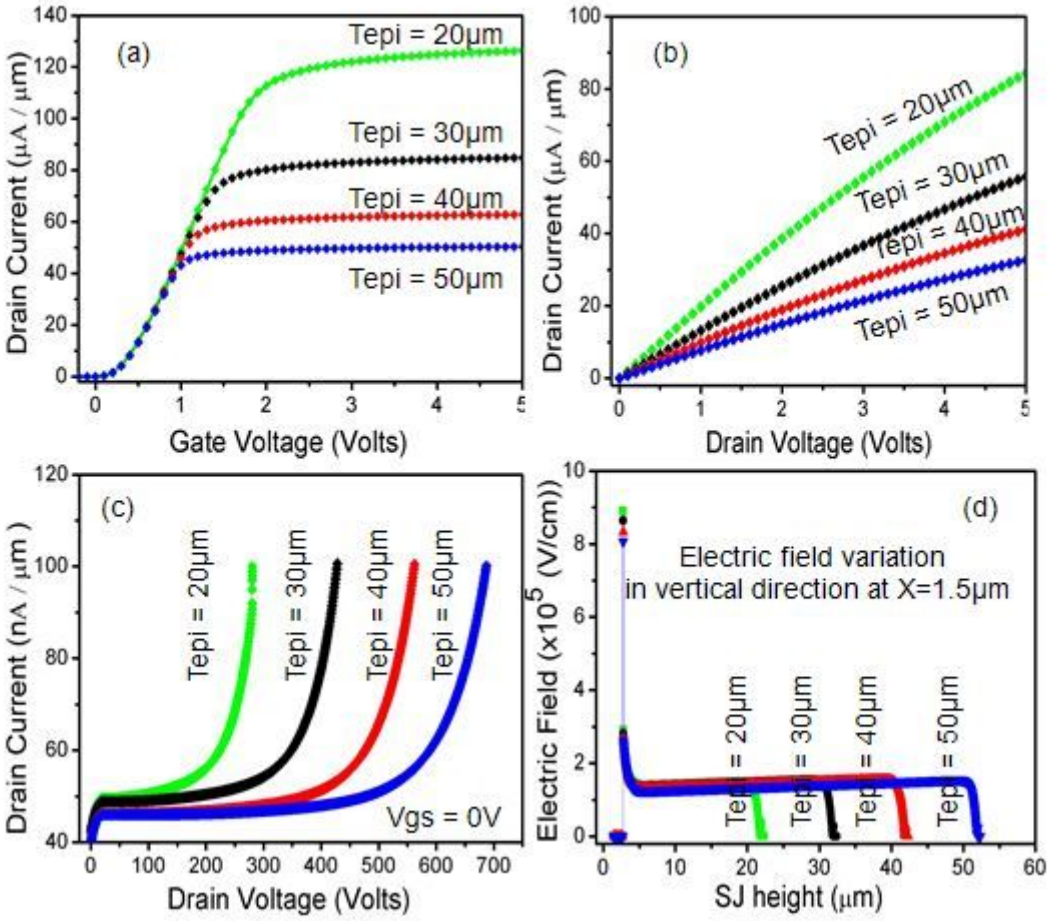

Figure 5

(a) I-V characteristics of the conventional trench gate super junction structure for different values of drift thickness. (b). output characteristics for varying drift thickness at Vgs=0V, (c) corresponding breakdown curves. (d). Electric field profile for increasing values of drift layer thickness

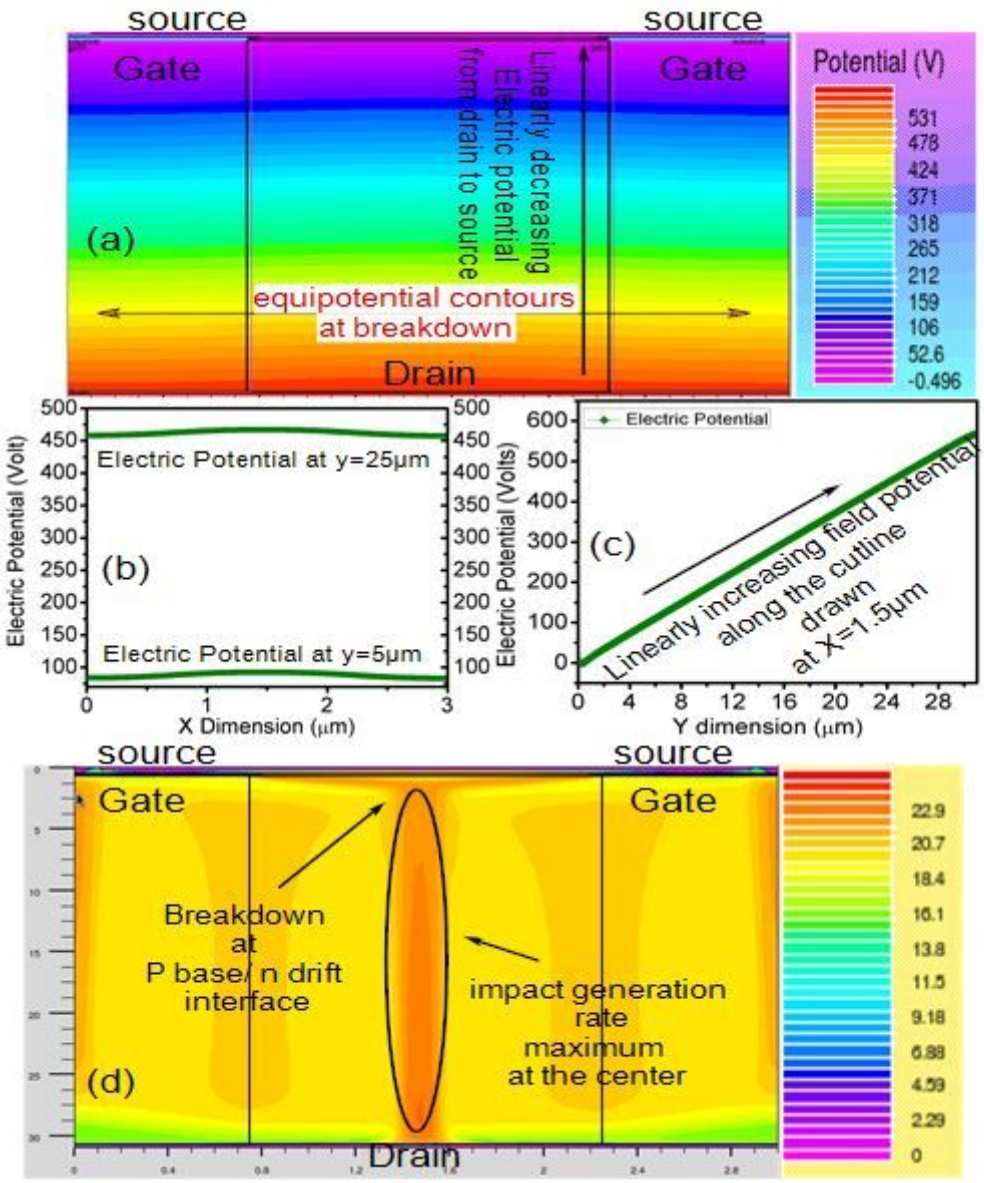

Figure 6

(a) Uniform distribution of potential contours in the super junction drift region, (b) Uniform distribution of electric potential lines laterally in the drift region which is taken by drawing a lateral cut line at y=5μm and y=25μm respectively (c) vertical variation of electric potential inside the drift region taken at x=1.5μm, (d) the distribution of impact generation rate inside the super junction drift region before breakdown.

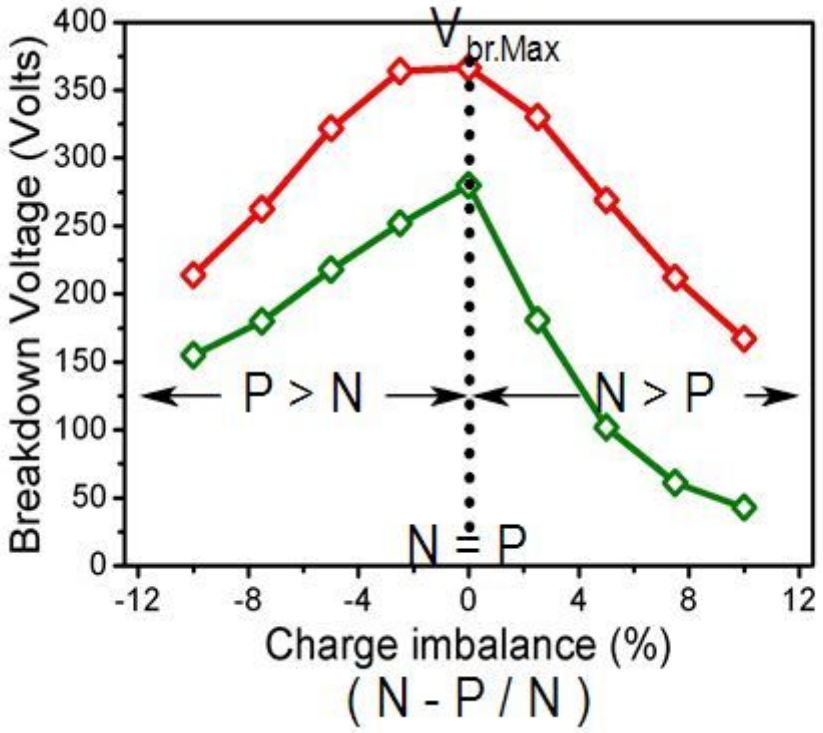

Figure 7

sensitivity of breakdown voltage for unequal n and p pillar charges. The red curve shows variations of the proposed device while the green one is for the conventional device.

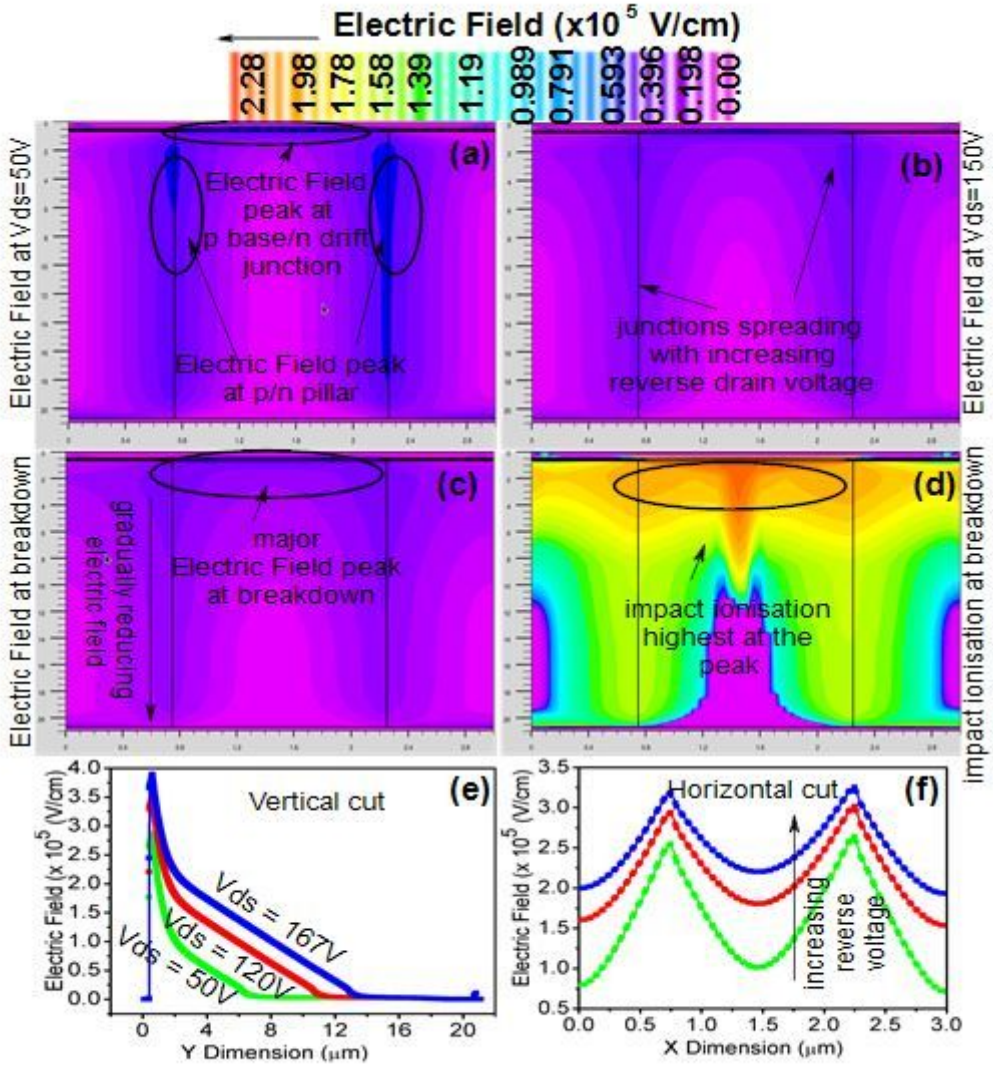

Figure 8

(a)(b)(c) Electric field contours at different values of reverse drain voltage for the condition when N>P. (d) impact ionization contours at breakdown. (e)The electric field profile which is taken by drawing a vertical cutline in the middle of the drift layer at x=1.5μm.(f) The lateral electric field profile taken by drawing a cutline at y=15μm.

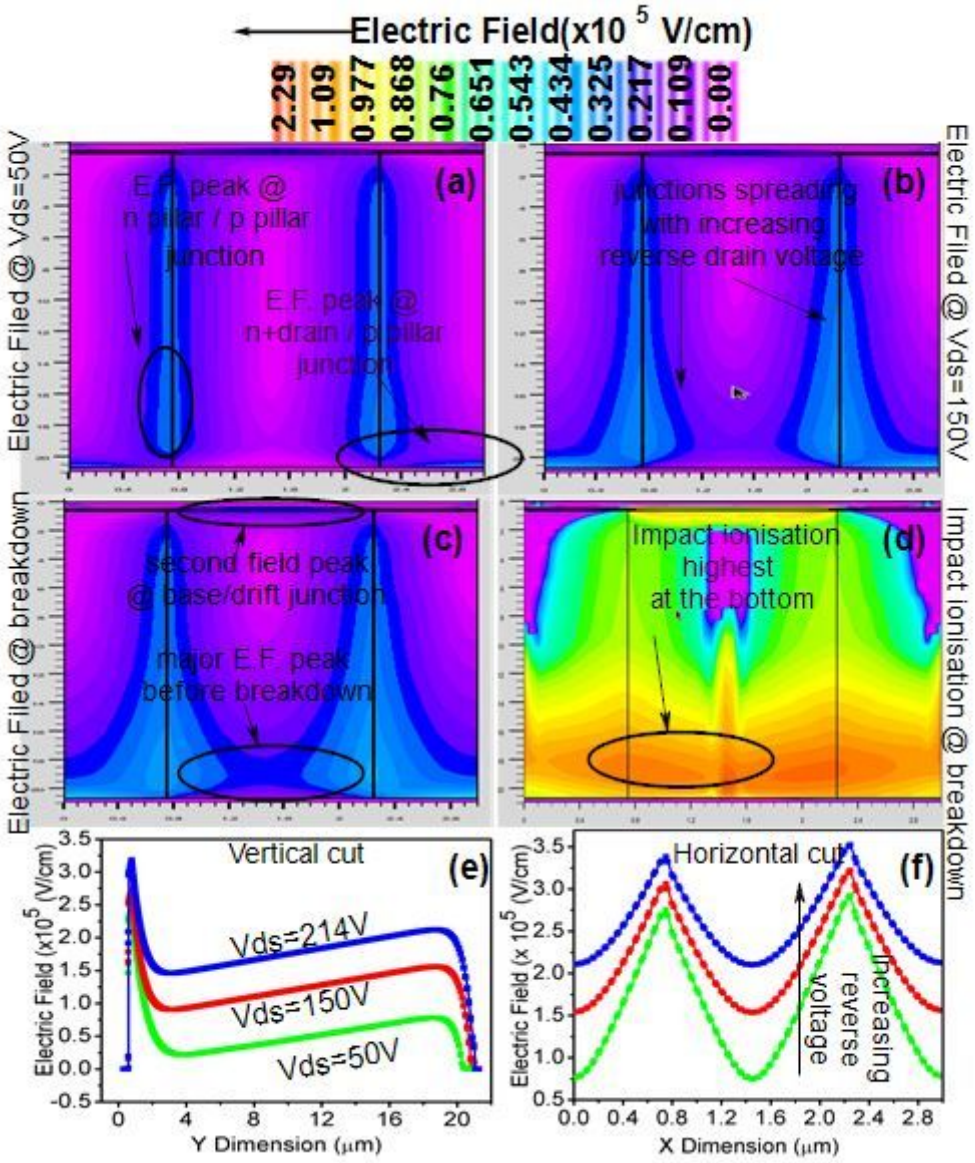

Figure 9

(a)(b)(c) Electric field contours at different values of reverse drain voltage for the condition when P>N. (d) impact ionization contours at breakdown. (e) The electric field profile which is taken by drawing a vertical cutline in the middle of the drift layer at x=1.5μm. (f) The lateral electric field profile taken by drawing a cutline at y=15μm.

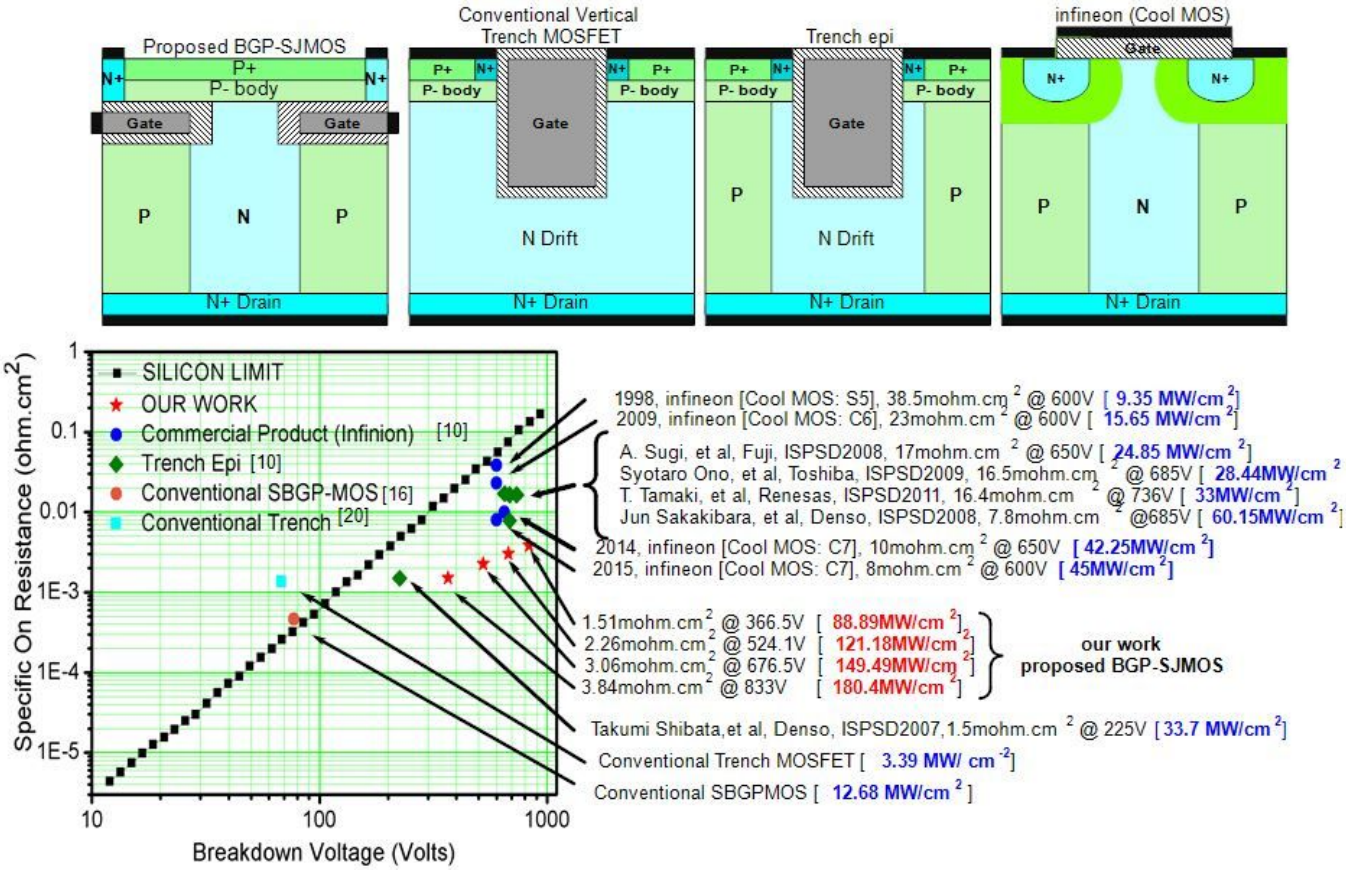

Figure 10

Specific ON resistance versus BV with the ideal silicon limit line, the reported structures in the literature [10],and the proposed super junction structure with different breakdown voltages

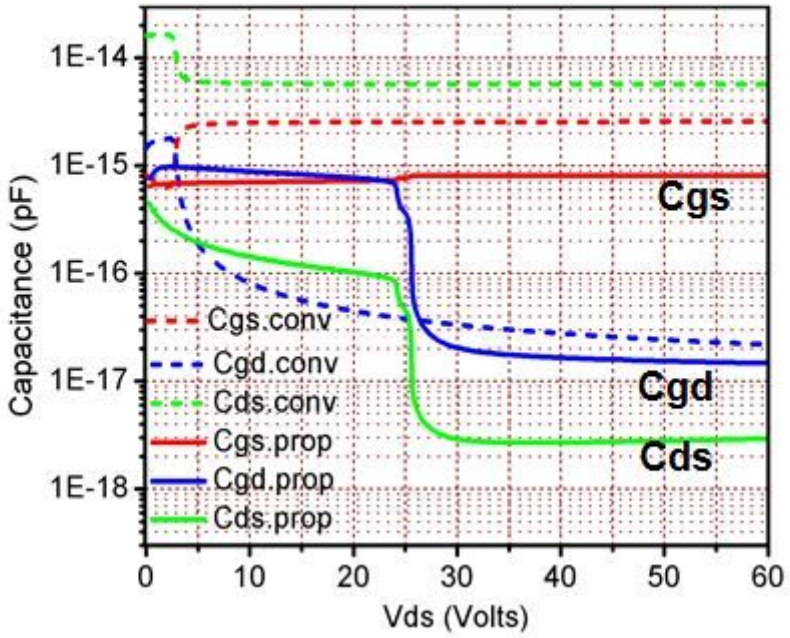

Figure 11

Comparison of Cgd, Cgs and Cds of the proposed GBP-SMOS and the conventional superjunction trench MOSFET, with increasing drain to source voltage (Vds).

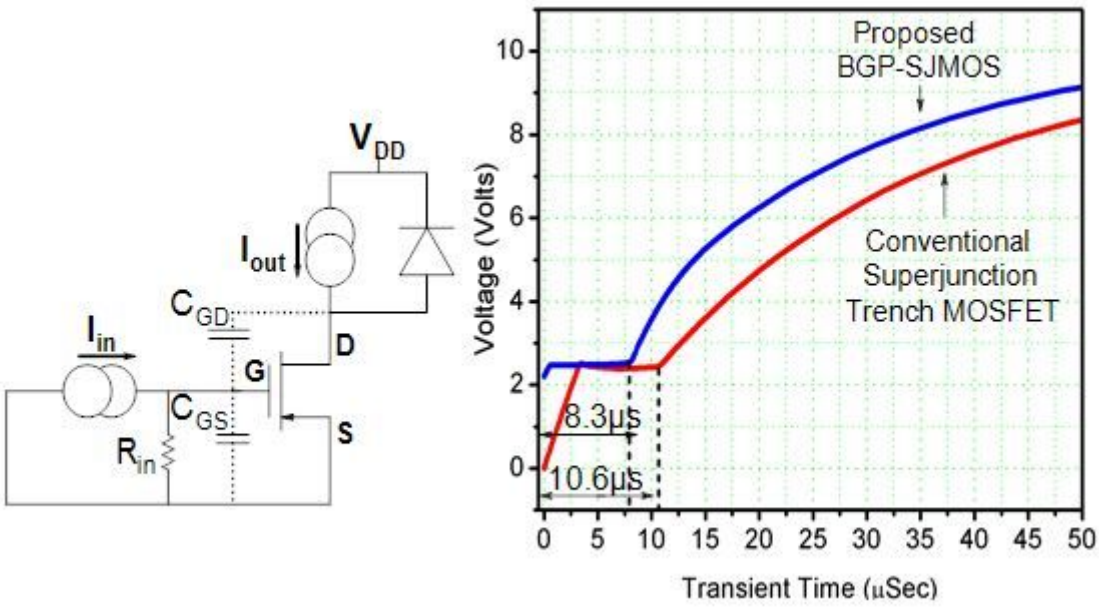

Figure 12

Gate charging transient curve for the proposed super junction MOSFET device with the circuit used to simulate the same

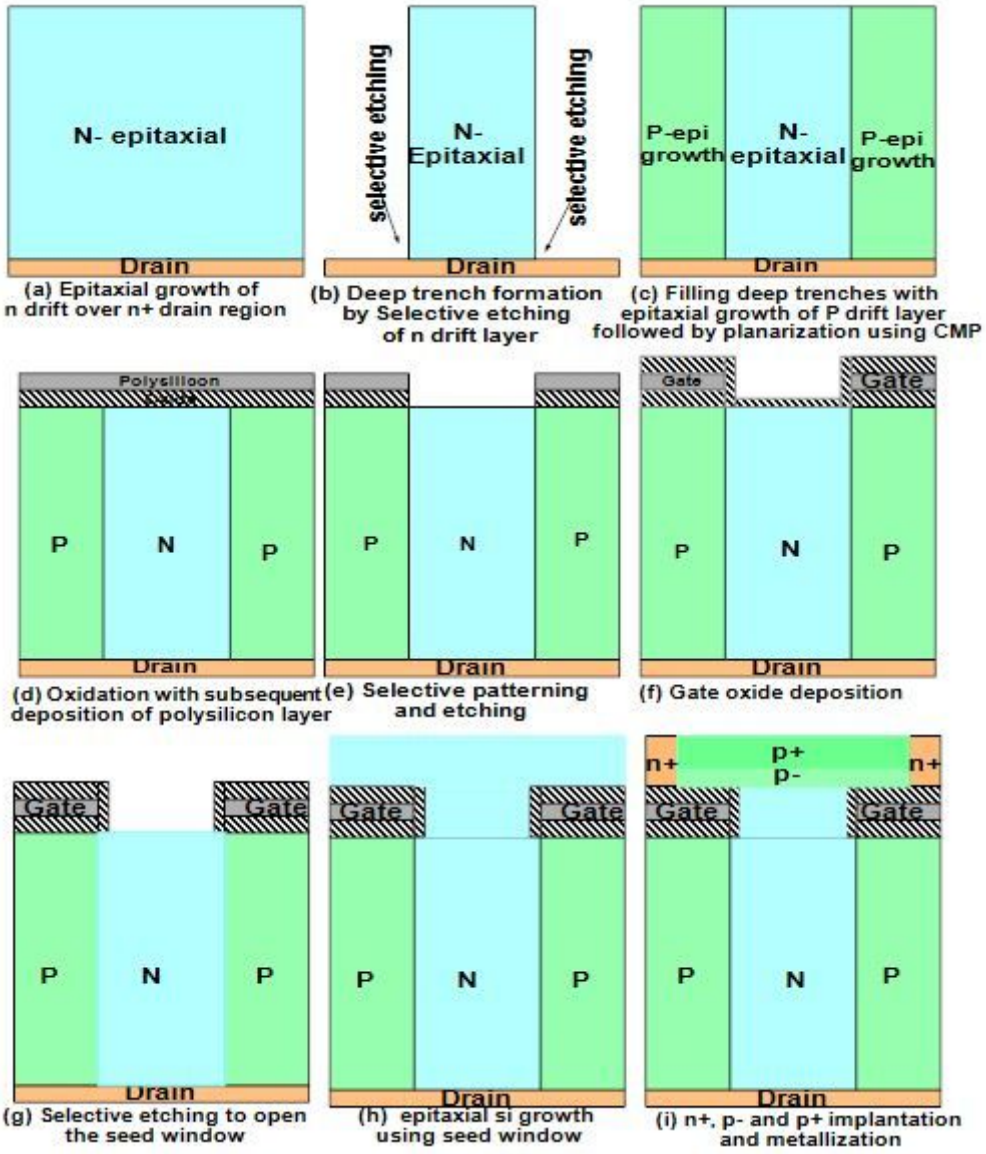

Figure 13

Process flow for the proposed device