Design and Analysis of Negative Capacitance Assisted SRAM: A Compact Model Based Study

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Design and Analysis of Negative Capacitance Assisted SRAM: A Compact Model Based Study

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Abstract

In this paper, a detailed evaluation of negative capacitance FinFET (NC-FinFET) based volatile static random access memory (6T-NCSRAM) is carried out by utilizing L-K equation for ferroelectric and calibrated BSIM-CMG model with 14nm conventional FinFET to form NC-FinFET. Static and dynamic behaviour of NC-FinFETs is explored and evaluated at different ferroelectric thickness. At supply voltage scaling, important SRAM performance metrics such as stability at different operation condition (hold, read and write mode) and standby leakage power were evaluated. When compared to traditional FinFET-based SRAM, 6T-NCSRAM exhibits distinct behaviour during low and high supply voltages. Moreover, the effect of wordline (WL) voltage pulse variation on 6T-NCSRAM is captured and minimum RC multiplier of 2RC is found to avoid functional failure of 6T-NCSRAM.

Keywords: Negative Capacitance, Steep Slope Devices, Ferroelectric Materials, Volatile Memories, Low Power Applications

1 Introduction

SRAM technology enables improved CMOS circuit technology scaling, which has huge consequences for Moore's law's continued existence [1]. Because of the rapid expansion of data-intensive computing, large-capacity SRAMs are in high demand across all product sectors, including machine learning accelerators, battery-powered SoCs, and high-performance ASICs. SRAM bitcell optimization, on the other hand, necessitates a delicate balancing act in order to meet the opposing read-write needs. In order to ensure proper read and write needs under normal operating conditions, SRAM bitcells have usually been built with a size ratio of (Pull-down > Access > Pull-up). Such scaling optimizations requirement are much more limited in FinFET CMOS technology due to

the intrinsic width quantization effect [2, 3]. This restricts the circuit designer's ability to implement a high-density memory array by requiring them to use single fin transistors for creating Pull-down, Access, Pull-up transistors for the SRAM bit cell. Because the bitcell's transistors are of the same size, contention can occur during read (in Access and Pull-down transistors) and write (in Access and Pull-up transistors), which results in a huge number of read or write failures. Furthermore, the expanding complication of process integration in semiconductor, exacerbated by the scaling in feature sizes, has resulted in increased intra-die and inter-die process variability. The major causes for these process variations include random dopant fluctuations [4], line edge roughness [5], and mask edge misalignment [6], which give rise to the threshold voltage (V_t) variation in the transistors. Since circuit characteristics are more susceptible to V_t fluctuations, the SRAM bitcell is much more prone to write and read failures, mainly at low supply voltages. This restricts the minimal supply voltage (also known as V_{min}) scaling to achieve functional SRAM operation. One way to prevent such possible failures is to utilize circuit-assist techniques such as wordline underdrive (WLUD) [7] for read operations and supply voltage collapse (SVC) [8] and negative bitline (NBL) [9] during write operations. The aforementioned circuit-level assist solutions, on the other hand, necessitate a increment in power and area requirement, as well as a substantial increase in cycle time. In addition, scaling necessitates the placement of more SRAM cells on a single word line (WL). Also, in the system with multiple loads in a long wire, coupling capacitance, especially the WL rising transition and the precharge signal lowering transition, can have a considerable effect on SRAM bit cell performance [10]. This is because the resistance and coupling capacitance of WL wire formed the resistor-capacitance (RC) network at the WL's signal [11]. This results in non-scaling RC with scaling [12], which is unacceptable in a high-performance SRAM design. The SRAM's performance is affected by the parasitic RC. As a result, the performance loss is compensated by using SRAM's coupling delay and RC correction circuit which requires additional circuits and increases area overhead in SRAM technology for lower technology node. So, in order to reduce overheads, researchers must evaluate SRAM-assist techniques on numerous levels, which includes: utilizing new materials, exploring device structure topologies, optimizations of process, and different circuit assisted techniques. Ferroelectric materials-based transistors [13] have gotten a lot of interest recently for their ability to provide ultra-low power in memory and steep switching applications due to the negative capacitance property exhibit by ferroelectric materials. These devices have gotten a lot of interest because of their simpler design and CMOS compatibility [14], compared to other state-of-the-art devices such as TFETs [15], HyperFETs [16], and Hybrid FETs [17–19]. In addition, the recognition of ferroelectricity in doped hafnium oxides like HZO [20] has rekindled curiosity in NC based FET. The interaction of the ferroelectric and MOSFET capacitances has a big impact on the NCFET's properties. The coercive field and residual polarization of ferroelectric materials determine the amount of internal magnification that can be achieved in an NCFET, and any changes in these key parameters can have a major influence on the overall NCFET performance. Logic circuits [21], flip-flops [22], oscillators [23], TCAM [24], and SRAM [25, 26] are just a few of NCFET-based circuits that have been researched and documented in the literature. It's worthy to note that physical insight of the negative capacitance process, as well as accompanying device engineering, is still in its infancy, and the future of NC technology, as well as the extent of benefit it can provide over current state-of-the-art CMOS technology, is in debate. Experiments have repeatedly shown that NCFET devices and circuits outperform traditional FETs, which is encouraging. Various NCFET modeling approaches, as well as investigations of their influence in improved transistor properties on circuits, have been reported. In [26], performance analysis of SRAM built using NCFinFET in 7nm technology node was detailed. NC transistors also exhibit low variability [25], which should increase the minimum supply voltages (V_{min}) of SRAM.

In this paper, we have investigated in detailed about the stability of NC-FinFET-based 6T-SRAMs (6T-NCSRAM) utilizing circuit driven simulations and a physics-based model of NCFinFETs, as well as variability tolerance using supply

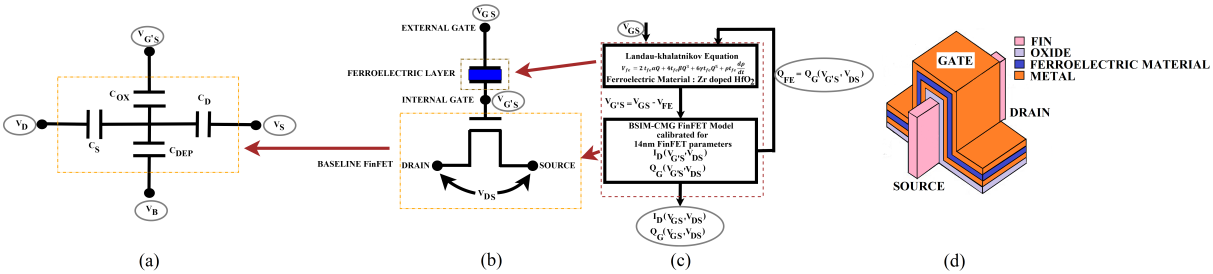


Figure 1 NCFinFET compact model approach (a) capacitor divider equivalent circuit, (b) its circuit equivalent of integrated ferroelectric in the FinFET transistor gate terminal, (c) its modeling flow chart, and (d) M-F-M-I-S device structures.

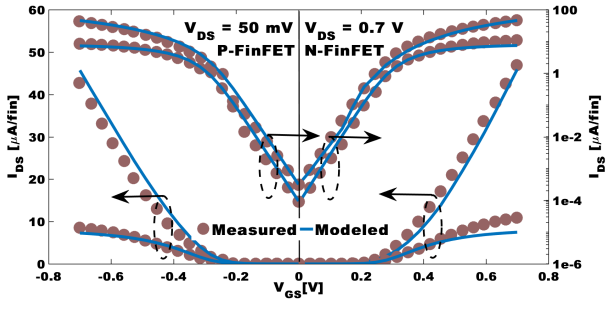
voltage scaling, ferroelectric thickness and RC delay arising due to wordline voltage variation. As a result, the findings of the study can be used as a modelling framework for circuit designers looking to evaluate and improve SRAM endurance to RC delay. The article is structured as follows: The basics and modelling approach used to design NCFinFET are discussed in Section II. The design of a 6T-SRAM cell employing NCFinFET transistors is discussed in Section III. In Section IV, the simulation findings and analysis are discussed, followed by a conclusion in Section V.

2 Negative Capacitance FinFET

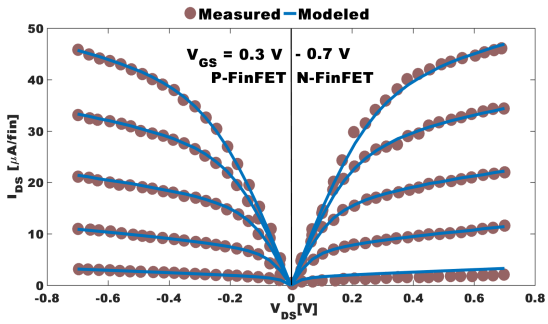
This section deals with the basic theory behind NCFinFET, its compact modelling procedure used and device verification.

2.1 Basics theory of NCFET

The NCFET structure is created by sandwiching ferroelectric material in the baseline FET's gate stack. Depending on the application, the baseline FET might be a MOSFET or a FinFET. Under a specific constraints ferroelectric material shows negative capacitance property to enhance transistor performance. Fig. 1 shows the metal-ferroelectric-metal-insulator-semiconductor (M-F-M-I-S) structure of NCFET, its flow chart and equivalent capacitor divider circuit. The experimentally realized M-F-M-I-S [28, 29] configuration might be thought of as two structures connected by wire, namely ferroelectric capacitance and baseline FinFET. The internal metal gate of the M-F-M-I-S structure may provide higher ON current and makes the device less vulnerable to



(a)



(b)

Figure 2 Calibration of BSIM-CMG model with experimental 14nm FinFET [27] (a) its transfer characteristic at low $V_{DS} = 50mV$ and high $V_{DS} = 0.7V$ and, (b) its output characteristic at varying V_{GS} for $V_{DS} = 0.7V$ for P-type and N-type FinFET respectively

hysteresis than its counterpart metal-ferroelectric-insulator-semiconductor (M-F-I-S) device structure [30]. However, because of the existance of ferroelectric leakage current and domain creation, several studies [31, 32] have indicated that the internal metal gate destabilizes the negative capacitance state. Furthermore, the internal metal gate includes an additional source of traps in NCFETs that creates reliability issues in NCFETs

[33–35]. In this paper we have consider M-F-M-I-S structure for the analysis. To explain further how NC inclusion benefits in reducing subthreshold slope (SS) it can be mathematically derive that SS can be split into two component namely: body factor (p) and transport factor (q) and is given by Eq. (1). NCFinFET achieves $SS < 60mV/decade$ by reducing body factor in the following way: body factor can further be split into the inverse of multiplication of voltage amplification factor (A_V) (Eq. (3)) and (m) Eq. (2). For positive connected series gate oxide capacitance, p is always greater than 1 and q is limited by thermionic limit $2.3K_BT/q$ i.e $60mv/decade$. But after inclusion of ferroelectric layer i.e negative capacitance in the gate stack, the total series capacitance formed due to ferroelectric capacitance (C_{FE}) and total internal FinFET capacitance (C_{INT}) is responsible for voltage amplification in NCFinFET. The inner voltage magnification at internal metal gate $V_{G'S}$ occur owning to the negative value of C_{FE} which make $A_V > 1$ and m is always less than unity. This voltage amplification is responsible for improvement of NCFinFET in terms of reducing SS beyond the Boltzmann limit (below 60mV/decade) and increment in the ON current for same applied voltage compared to FinFET because the combined term $A_V * m > 1$ which leads to the reduction of term $p < 1$ and finally reduces the overall SS.

$$SS = \frac{\partial V_{GS}}{\partial log_{10} I_{DS}} = \underbrace{\frac{\partial V_{GS}}{\partial V_{G'S}} * \frac{\partial V_{G'S}}{\partial \psi_S}}_{\text{p}} * \underbrace{\frac{\partial \psi_S}{\partial log_{10} I_{DS}}}_{\text{q}} = \frac{1}{A_V.m} * \frac{\partial \psi_S}{\partial log_{10} I_{DS}} \tag{1}$$

$$m = \frac{\partial \psi_S}{\partial V_{G'S}} = (1 + \frac{C_S}{C_{OX}})^{-1} < 1 \tag{2}$$

$$A_V = \frac{\partial V_{G'S}}{\partial V_{GS}} = (1 - \frac{C_{INT}}{|C_{FE}|})^{-1} > 1 \quad for\ C_{FE} < 0 \tag{3}$$

In article [36], it is recommended that an unstable NC state can be stabilized by coupling a positive dielectric capacitance in series with the ferroelectric, causing the system's total capacitance to become positive. In case of NCFinFET, internal gate of baseline FinFET behave as positive capacitance (C_{INT}) and is in series with the capacitance formed by ferroelectric material. Unstable NC state stabilizes if the net gate capacitance $= 1/(C_{INT}^{-1} + C_{FE}^{-1})$ becomes positive. In order to achieve a thermodynamically stable NC state of the ferroelectric in NCFinFET, $|C_{FE}|$ must be larger than C_{INT}. It is to be noted that both capacitance ($|C_{FE}|$ and C_{INT}) are function of applied drain voltage (V_D) and gate voltage (V_G). For any combination of V_G and V_D, violation of the foregoing condition leads to hysteresis behaviour in the device's electrical characteristics [37]. To prevent these conflicts, ferroelectric thickness T_{FE} must be controlled because $|C_{FE}|$ changes inversely with T_{FE}. Moreover, $|C_{FE}|$ is also impacted by ferroelectric material's coercive field (E_c) and remnant polarization (P_r). Ferroelectric material with high (P_r) and low (E_c) increases the $|C_{FE}|$ value [38]. This assures that in the range of operating voltages, the requirement of no hysteresis, i.e. $|C_{FE}| > C_{INT}$, is always met. It is to be noted that capacitance matching between C_{INT} and C_{FE} reduces which also reduces the ferroelectric gain (Eq. 3) if ferroelectric material has low E_c, high P_r and a low T_{FE}. Thus, critical values must be carefully selected, such that higher NC gain is achieved while avoiding hysteresis, which is undesirable for logic applications.

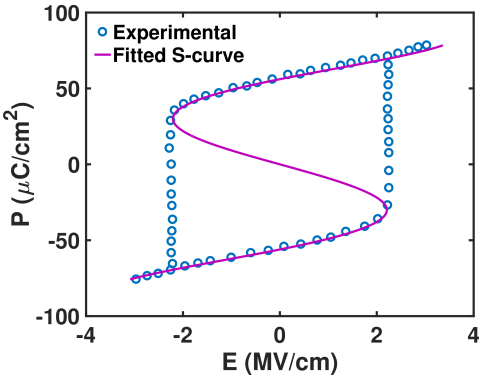


Figure 3 Calibration of FE model with P-E curve of Zr-doped HfO_2 material [39].

2.2 Compact Modeling Methodology of NCFET

In the compact modeling technique, the self-consistent coupling of the industry standard

BSIM-CMG model [40] with the ferroelectric model created in verilog-A is used. To create a ferroelectric model single domain time-dependent L-K equation (Eq. 4) derived from Equations A1, A2, A3, A4 (refer appendix A) is used.

$$V_{FE} = (2\alpha Q_G + 4\beta Q_G^3 + 6\gamma Q_G^5 + \rho\frac{dQ_G}{dt})T_{FE} \quad (4)$$

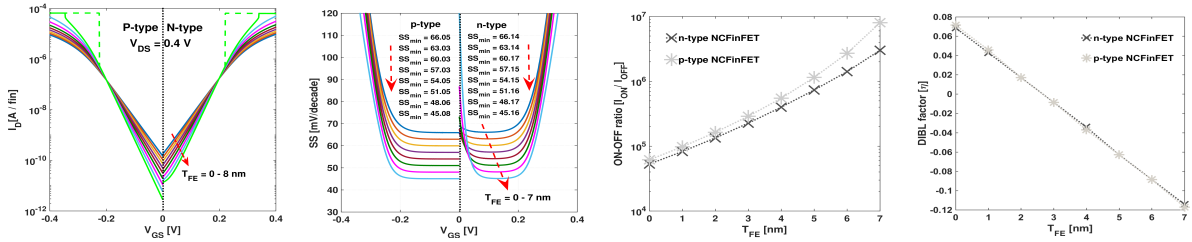
where α , β, γ are materials specific landau coefficients and the kinetic coefficient ρ is related with the time constant associated with ferroelectric polarisation change. Ferroelectric model (S-curve) is calibrated to experimental P-E curve of doped $Zr-HfO_2$ [39] as shown in Fig. 3. The flowchart in Fig.1 depicts the whole modeling flow of the NCFinFET. Initially, the BSIM-CMG model is calibrated to a 14nm high performance model card for FinFET acquired from [41]. Further calibration is done by tuning model card parameter of BSIM-CMG model: mobility degradation, SS, velocity saturation, series resistances and DIBL parameters for matching with the experimental results [27]. The calibrated device transfer and output characteristics are illustrated in Fig. 2 (a) and Fig. 2 (b), respectively, for number of fins (Nfin) = 1, gate length (Lg) = 20 nm. The self-consistent approach then begins by first extracting the gate charge (Q_G) from the 14nm calibrated BSIM-CMG model. This Q_G is given to the ferroelectric L-K model developed in verilog-A. The output of L-K model is the difference in the voltage between ferroelectric V_{FE} and applied gate voltage V_{GS} which is termed as internal voltage $V_{G'S} = V_{GS} - V_{FE}$. This modeling approach is based on certain assumptions, such as the consideration of mono-domain formation in ferroelectrics. Polarization (P) is assumed to be equal to Q_G, i.e. $P = Q_G - \epsilon_o * V_{FE}/T_{FE} \approx Q_G$. Table 1 lists the required parameters of ferroelectric material (doped HfO_2) in the L-K model and baseline FinFET. The main criticism levied at the L-K theory of phase transition based phenomenological modeling technique is a lack of experimental support for the S-shaped P-E curve. However, [42] recently demonstrated experimentally validated methods for detecting S-curves and steady-state negative capacitance, lending validity to the utilized modeling methodology. Despite its simple approach, the model is capable of capturing all of the NCFET's unique properties, unlike other techniques [43]. In addition, the L-K model was able to reproduce experimental results of NCFinFETs with ferroelectric thicknesses as small as 1.5nm [44], 3nm [45]. Furthermore, there is no additional delay penalty in the NC effect on its own [45]. The transfer characteristics of the n-type and p-type NCFinFETs with different ferroelectric thickness (T_{FE}) are shown in Fig.4(a). The baseline FinFET transfer characteristic, denoted by $T_{FE} = 0nm$, is also plotted for comparison. NCFinFET have a greater sub-threshold swing(lower subthreshold slope) (Fig.4(b)) and ON to OFF current ratio (Fig.4(c)) than the baseline FinFET. These advantages become more evident as T_{FE} increases. It can be seen that at $T_{FE} = 8nm$, hysteresis appears to occur in the output characteristics. This is due to a mismatch in the ferroelectric capacitance and internal total baseline FinFET capacitances (discussed in 2.1), which should be avoided if such an NCFinFET device is to be used for logic and memory applications [46]. The unique feature: negative DIBL [47] and NDR [48] in the NCFinFET indicating the small model's capacity is shown in Fig. 4(d).

Table 1 Parameters of the NC and 14nm-FinFET

Physical Parameters			
Parameters	NC[39]	Parameters	14nm-FinFET
$\alpha(m/F)$	$-1.17\text{x}10^9$	L_g	$20nm$
$\beta(m^5/F/C^2)$	$4.9\text{x}10^9$	T_{FIN}	$10nm$
$\gamma(m^9/F/C^4)$	$3.9\text{x}10^9$	H_{FIN}	$50nm$
$\rho(\Omega.m)$	0.18	$Finpitch$	$42nm$

3 NCFinFET based SRAM Cell

Fig.5 shows the basic six transistors SRAM cell designed using negative capacitance FinFET (6T-NCSRAM). It is composed of two pull-up (PM1,PM2), two pull-down (NM1,NM2) and two access (NM3,NM4) NCFinFET transistors. The internal node is denoted by Q and QB and is accessed by NM3 and NM4 through bitlines BL and BLB respectively. Word line (WL) is connected to gate of NM3 and NM4 for read, write and retention of bit stored in internal node. PM1, NM1 and PM2, NM2 formed two NCFinFET based inverter connected back to back through internal



(a) (b) (c) (d)

Figure 4 N-type and P-type NCFinFET device (a) Transfer Characteristics (b) its subthreshold slope (c) its ON-OFF current ratio (d) Drain induce barrier lowering (DIBL) factor (η) for different thickness at $V_{DS} = 0.4V$

node Q and QB. Vdd is the supply voltage to provide power to two inverters. p-type NCFinFET is used to designed pull-up transistors. Pull-down and access transistors are designed using n-type NC-FinFET. Designed 6T-NC-SRAM is considered with '1:1:1' fin configuration where pull-up (PM1, PM2), access (NM3, NM4) and pull down (NM1, NM2) transistors are in 1:1:1 fin-ratio. This aspect ratio allows to use single fin transistors and eliminates width quantization effects occur in FinFET based structures.

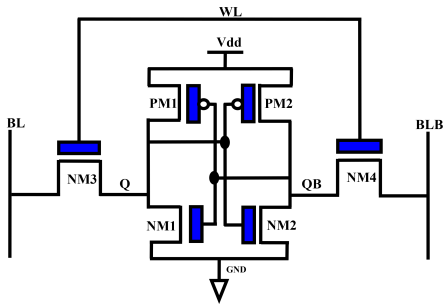


Figure 5 Circuit schematic of 6T-NC-SRAM Cell where each conventional FinFET transistor is replaced with NCFinFET transistor.

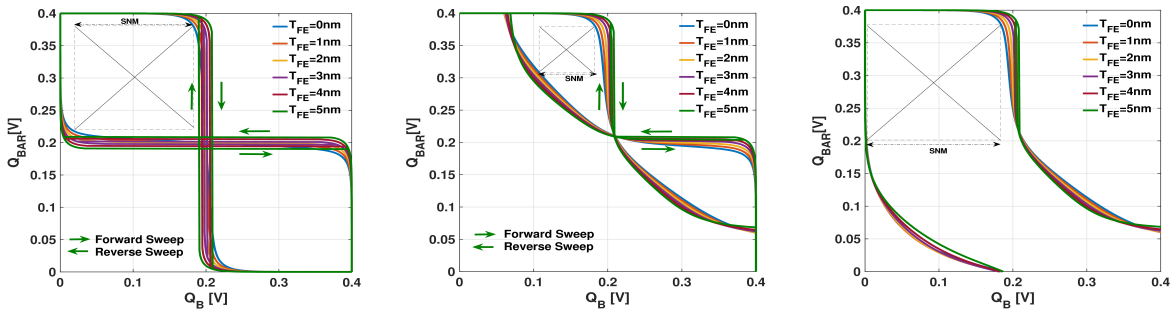
4 Results & Discussions

This section begins with the stability analysis, the effect of supply voltage scaling in the stability, real time transient analysis and effect of RC delay in the WL voltage.

4.1 Stability Analysis

To assess the performance of the designed SRAM, we first examine the stability of the 6T-NCSRAM cell in hold, read, and write modes using well-known methodologies such as the butterfly curve (BC) [49] and the N-Curve [50]. For the sake of this analysis, we used a $Vdd = 0.4V$. Using the circuit arrangement depicted in Fig.5, we begin by examining the 6T-NCSRAM static noise margin. WL, BL, and BLB are connected to ground in hold mode. WL is connected to supply voltage (Vdd) for read mode, and BL, BLB is precharged to Vdd. In write mode, WL is connected to the Vdd, BL voltage is precharged with Vdd, and BLB is connected with the GND rail. QB is assumed to be storing logic '1' in all modes, and node Q is swept from GND to Vdd. Node QB is pulled to logic '0' when logic '1' is written. Side of the maximum squares fit inside the forward VTC and backward mirrored VTC or vice versa is used to compute the effective noise margin in hysteretic situations, as described in [51]. The hold, read, and write butterfly curves for NC based SRAM at various NC thicknesses and conventional FinFET (denoted by $T_{FE} = 0nm$) are exhibit in Figure 6(a), (b) and (c) respectively. Enhanced hold SNM is achieved by steep switching of inverter, which is further aided by the VTC hysteresis, which increases with the T_{FE} increment. Despite the fact that greater loading impact of the access transistor during read and write operations results in higher read-disturb and write-disturb voltage in 6T-NCSRAM compared to traditional SRAM, the read SNM and write SNM are enhanced because of the bigger lobes in the VTC described in Fig.6 (b),(c).

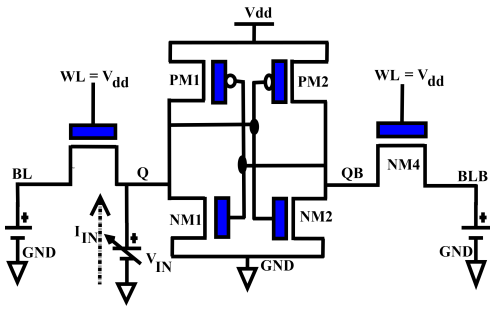
We also analyze the critical current during write and read operations using N-curve method. The arrangement for obtaining the N-curve that detects the current flowing through the node Q is given in Fig.7(a) and the respective N-curve is exhibit in Fig.7(b) under read condition. The peak



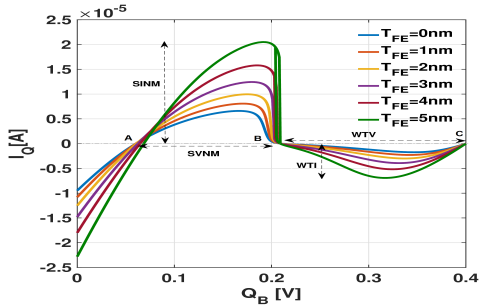
(a) (b) (c)

Figure 6 Simulation performed for stability analysis using butterfly curve method to calculate static noise margin (a) during hold mode, (b) read mode, and (c) write mode for $Vdd = 0.4V$ at different ferroelectric thickness.

current (SINM) in the N-curve between region 'A' and 'B' determines the minimum current required to induce a destructive read, whereas the critical write current (WTI) between region 'B' and 'C' is determined by the minimum value obtained. It can be noticed that increasing T_{FE} improves the cell's read-stability and write-stability.



(a)



(b)

Figure 7 N-curve method for stability analysis (a) its setup to obtain N-curve and, (b) the corresponding N-curve for critical current at different ferroelectric thickness.

4.2 Transient Analysis

Once 6T-NC-SRAM cell is stable we perform the real time transient analysis with different NC thickness as shown in Fig. 8. WL is applied with 5 GHz input signal and BL and BLB time period is varied to obtain hold, read and write state. Voltage at node Q and QB is analyzed for different conditions. Proper functionality of SRAM is obtained with different hold, read and write condition. In compared to FinFET based SRAM ($T_{FE} = 0nm$), the read delay lowers and the read speed increases as FE thickness increases, as shown in inset Fig. 8, while write time penalty occurs as NC thickness increases.

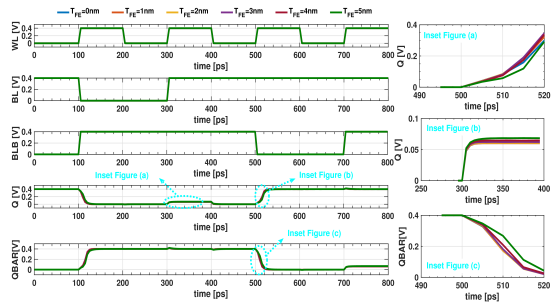


Figure 8 Real time transient analysis of stable and functional 6T-NC-SRAM cell for different ferroelectric thickness.

4.3 Supply voltage scaling

To analyze the effect of variability with supply voltage we analyze the stability metrics of the 6T-NCSRAM with scaling in supply voltages. Fig.9 exhibit the effect of supply voltage variation in

stability of 6T-NC-SRAM for different thickness. It can be seen that hold SNM improves as we increases the supply voltages for both conventional FinFET based SRAM and NCFET based SRAM. However, the hold SNM starts to reduce slightly at higher supply voltages after a critical T_{FE}, because of the increment in access transistors strength in the starting of the transition region. In case of read stability, at higher supply voltage the stability decreases in the NCFinFET. On the other hand write stability also increases with increasing supply voltage. While analyzing N-curve at different supply voltage we plotted static current noise margin (SINM) and write trip current (WTI) (Fig. 10(a), (b)). SINM and WTI increases with the scaling of supply voltage and enhances with respect to conventional FinFET based SRAM with increasing thickness. Also, for better visualization of the stability analysis, static power noise margin (SPNM) is calculated for varying T_{FE} as describe in Fig. 10(c), from the N-curve using the values of A and B as seen in Fig.7(a) and is expressed as:

$$SPNM = \frac{1}{(B-A)} \sum_{n=A}^{n=B} I_{in}(n) * V_{in}(n) \qquad (5)$$

Large value of SPNM and SINM is obtained at $T_{FE} = 5nm$ which reveals enhanced read stability. Similarly, write trip power (WTP) is calculated for varying T_{FE} as exhibit in Fig. 10(d), from the N-curve using the values of B and C as seen in Fig.7(a) and is given as:

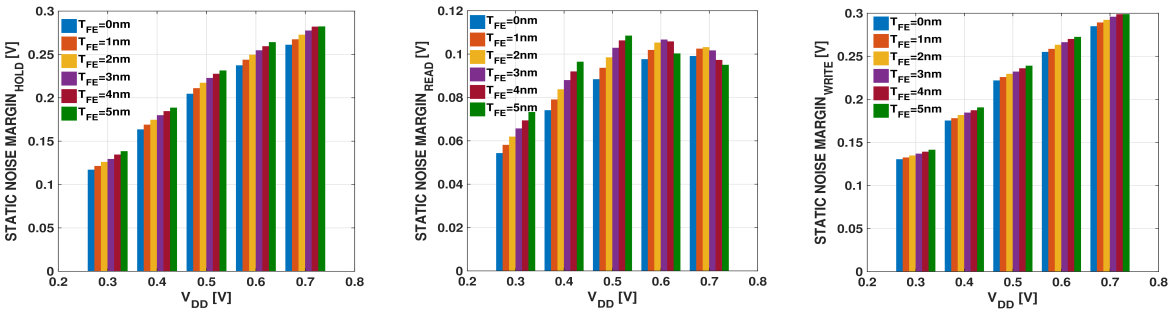
$$WTP = \frac{1}{(C-B)} \sum_{n=B}^{n=C} I_{in}(n) * V_{in}(n) \qquad (6)$$

It can be seen that SPNM must be positive (i.e. SPNM > 0) and WTP must be negative (i.e. WTP < 0) for successful read and write operations.

We also analyze effect of supply voltage and effect of NC thickness in the speed of the NCFinFET based SRAM during read and write case. We calculated the normalized delay with respect to FinFET based SRAM and it is shown in Fig.12(a), and (b) that as we increase the supply voltage the read time increases but for increasing FE thickness it decreases in comparison to reference to FinFET SRAM. On the other hand write time slightly increases with increasing NC thickness and with supply voltages.

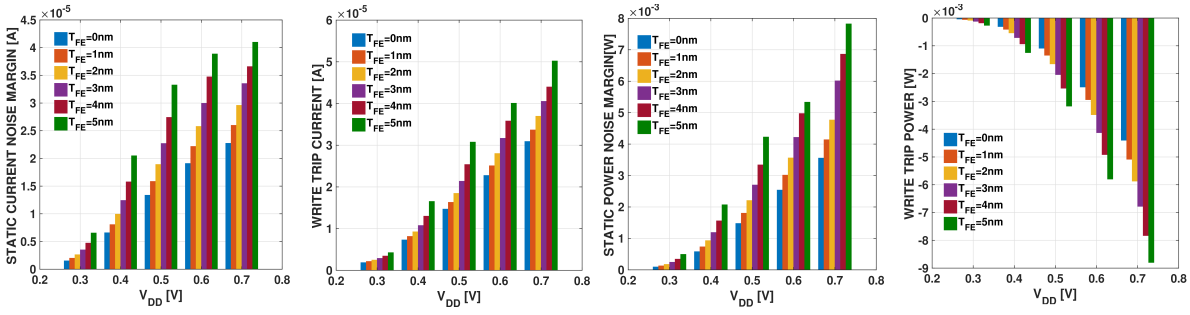
4.4 Word Line variation

To analyze the variability in WL voltage, we begin with the variation of WL voltage. To do so we have used RC model to induce variation in the WL as shown in Fig. 11. Table 2 shows the different RC multiplier used to analyze the effect of WL variation. Fig. 13 depicts the 6T-NCSRAM transient analysis at $T_{FE} = 3nm$ within 800ps simulation time range for periodic wave input obtained by applying 100, 20, 4, 2.2 and 2 RC multiplier applied to the word line. The result in Fig.13 is split down into eight segments, each of which is examined separately. In segment 1, 6T-NCSRAM bit cell Q node is initialized with logic '1'. In segment 2, WL is applied, and the 6T-NCSRAM internal nodes (Q and QB) are dictated by V(BL) and V(BLB). V(Q) sinks to '0' instantly for V(WL) with a 100 RC multiplier. For V(WL) with decreasing RC multiplier, node Q voltage drop is much gradual. V(WL) decreases in segment 3 after achieving the peak value of voltage in the end of segment 2 at 200ps. It can be seen that at time value 200ps, for 2RC multiplier, V(WL) achieve maximum peaks nearly at 0.4V. As a result, the access transistor's drain current is insufficient to flip the signal at nodes Q and QBAR. Thus, at 200 ps, the 6T-NCSRAM is unable to hold logic '0'. In segment 3, V(WL) for 2RC decreases, and the node Q signal is gradually stabilizes to logic '1'. Nonetheless, 6T-NC-SRAM is storing the wrong value for V(WL) of 2RC at V(Q) and V(QBAR). In segment 4, 6T-NCSRAM works in read mode. V(WL) of 2RC rises, but since both V(BLB) and V(BL) are in high state, V(QBAR) and V(Q) remain same and wrong values are read. In segment 5, V(WL) of 2RC gradually decreases and does not effect the node Q. In segment 6, logic '1' is written into 6T-NCSRAM cell. The write operation is successful for V(WL) of 100RC, 20RC, 4RC, and 2.2RC, with a visible and longer delay for lower RC. Nonetheless, with V(WL) of 2RC, the voltage at node Q remains at 1. The internal nodes of the 6T-NCSRAM are consistent for all V(WL) in segment 7. (WL). In segment 8, the 6T-NCSRAM is being read, and the internal nodes of the 6T-NCSRAM have not changed significantly.



(a) (b) (c)

Figure 9 Supply voltage scaling in NC-SRAM static noise margin calculated using butterfly curve method (a) at retention mode, (b) read operation and, (c) write operation at different ferroelectric thickness.



(a) (b) (c) (d)

Figure 10 Supply voltage scaling effect in 6T-NC-SRAM stability using N-curve derived metrics (a) static current noise margin, (b) write trip current, (c) static power noise margin, and (d) write trip power at different ferroelectric thickness.

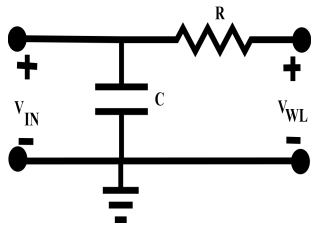
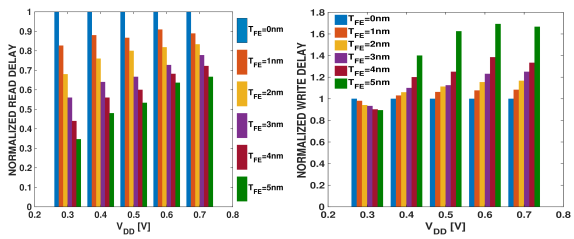


Figure 11 RC network for inducing variation in word line signal



(a) (b)

Figure 12 Effect of supply voltage scaling in 6T-NC-SRAM normalized delay time (a) during read access and, (b) write access at different ferroelectric thickness.

Table 2 Different RC multiplier values used for variation in word line signal

Resistor(R) (in Ω)	Capacitor(C) (in pF)	Time Constant(RC) (in $p.sec$)	Input Half Cycle (in $p.sec$)	RC Multiplier
1	1	1	100	100
1	5	5	100	20
1	25	25	100	4
1	44	44	100	2.2
1	50	50	100	2

We also analyze the leakage power during static mode and average power of NCFinFET and FinFET based SRAM. It can be seen in Fig. 14 (a) leakage power decreases with increasing FE thickness for Vdd = 0.4 V upto a certain critical thickness. This means that keeping the operating point out of the improved GIDL zone is critical for taking advantage of lower subthreshold currents in NCFinFETs. Fig. 14 shows the total average power dissipation with different RC multiplier and it can be seen that increasing RC multiplier decreases the average power while increasing the NC thickness slightly increases the average power.

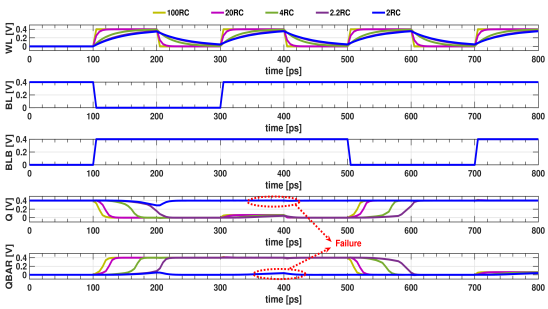
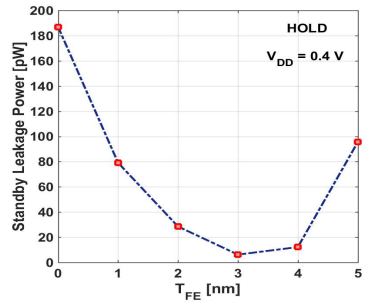
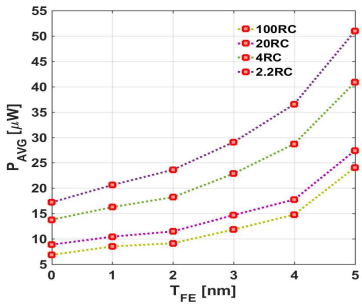


Figure 13 Transient Analysis of 6T-NC-SRAM Cell at $T_{FE} = 3nm$ with different RC multiplier showing failure at 2RC multiplier



(a)



(b)

Figure 14 (a) Leakage Power and (b) average power consumption for different RC multiplier at $V_{DD} = 0.4V$ with varying ferroelectric thickness

5 Conclusion

In this article, we have analyzed and discussed the stability for the conventional FinFET and NC-FinFET based 6T-SRAM cell in 14nm technology using direct current (DC) and transient analysis in SPICE. Verilog-A driven physics based compact approach is used to model the NC-FinFET. By examining the SRAM in retention, read and write mode its voltage transfer characteristics (VTC) is obtained which become hystertic with increasing NC thickness. In addition, stability is verified by using well-known Butterfly Curves and N-curves metrics to calculate the Static Noise Margin (SNM). Once the SRAM cell of both FinFET and NC-FinFET is stable, transient analysis is performed to verify the functionality and delay analysis is performed using real time signal. Apart from this, variability tolerance in stability and read and write delay due to supply voltage scaling is analyzed for both FinFET and NC-FinFET SRAM. Moreover, the different reasonable values of RC delay is given to word line signal, and the value of RC delay for which the SRAM failure happen is calculated. Power calculation is performed with both conventional FinFET and NCFinFET based SRAM. As a result, the findings of the research can be used as a modelling platform by circuit designers to investigate and improve SRAM tolerance to RC delay.

Appendix A Model of Negative Capacitance using L-K equation

The Gibbs free energy can be expressed as the function of electric field and polarization Eq. (A1)

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{A1}$$

Also, the rate of change in polarization charge in the FE, where P is the polarization, can be written as Eq. (A2):

$$\rho \frac{dP}{dt} = -\frac{dG}{dP} \tag{A2}$$

Combining Eq A1 and A2 expresses the time dependent L-K equation which describe relationship between electric field (E) as a function of polarization (P) Eq. (A3) :

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \tag{A3}$$

Also, electric field and voltage can be expressed as Eq. (A4):

$$E = V_{FE}/T_{FE} \tag{A4}$$

Substituting Eq. (A4) in Eq.(A3) provide us a final form Eq. (4) suitable for implementation in Verilog-A driven approach

Acknowledgments. Not Applicable

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Ethics Approval Ethical responsibility are followed by authors.

Consent to Participate All authors agreed with the content and give explicit consent to participate.

Consent for Publication All authors agreed with the content and give explicit consent to submit.

Data availability No datasets are generated.

Code availability The data presented in this study are available on request from the corresponding author.