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Analyzing A High Gain, Low Power OTA for Biomedical applications in 180 nm CMOS Technology

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Analyzing A High Gain, Low Power OTA for Biomedical applications in 180 nm CMOS Technology

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ABSTRACT
As biopotential signals are having very small frequency variations tens of Hz and micro to millivolts amplitude in the range. While acquiring biopotential signals from a human body, intrusions occur in the acquisition system. Thus for acquiring noise-free signals, the enhanced Biopotential Acquisition unit having a high gain with an improved common-mode rejection ratio readout front-end is designed. To solve mentioned issues, a Fully Differential Two-Stage OTA is introduced in this paper to achieve high DC gain and high Unity-gain frequency. Operational Transconductance Amplifier operates at ±0.2 V supply voltage, the bias current of 20µA, and achieves a high gain of 74dB. The design comprises a frequency compensation structure by connecting a capacitor across a high voltage stage and the load capacitor is connected across output by following the relation of $C_C > 0.22\ C_L$. The proposed high gain stage achieves additional gain with reduced noise of 0.2 mV/$\sqrt{\text{Hz}}$ with a minimal power consumption of 1.9 nW. The analog readout front-end is executed using 180 nm CMOS Technology and utilizes less power, making it ideal for battery-powered devices in Biopotential Acquisition systems.

Keywords:
Bandwidth, CMOS integrated circuits, Gain, Noise, Operational Transconductance Amplifier (OTA), Power consumption, Two-Stage Amplifiers.

1. INTRODUCTION

A major challenge in the 21st-century Biopotential Acquisition System is high power dissipation with the increase in noise. With the advancement in VLSI technologies, the size of CMOS, value of power supply, and power consumption are the critical parameters [1]. With the development in amplifier technology, designers have placed more emphasis on high gain, improved phase margin, and less occupied area [2-6]. The growing need for an unambiguous biopotential acquisition system being periodically checked on the sensing signals has turned analog mixed CMOS circuit design for high performance into a principal field [7]. The biopotential signals are observed to be accompanied by various repugnant signals like (1/f) noise, thermal noise, and power line distortion [8]. Thus an effective acquisition system designed for the removal of noise in biopotential signals shows a low-power readout front-end with high CMRR [9-10]. Over the last few decades, the scaling of transistor size resulted in a reduction in both power supply, Vdd, and transistor gain with efficient designing methodologies of multistage amplifiers that have been updated and optimized [11-15]. CMOS OTA with Miller Frequency Compensation Network is one of the important elementary units of mixed-signal processing. OTA i.e, a Voltage-Controlled Current Source, is chosen over traditional OP-AMPS due to its low output impedance with high power dissipation. Its cumulative DC gain improves as the magnitude of output conductance reduces [16-20]. While OTA can also be analyzed using low voltage with low power results in a device with additional battery life [21]. A few issues that OTA designers encounter are the DC offset errors, flicker noise, coupling, and common mode interference of signals [22-24]. To achieve high gain, these interferences should be avoided. A behavioral representation of an Operational Transconductance Amplifier provides high gain, high stability, low noise, and high speed while devouring minimum power consumption [25-27]. The proposed OTA is analyzed in a differential mode and will overcome the issues of noise and the number of devices on a chip. The appropriate voltage and stability are maintained while using a technique for compensating for noise gain and negative resistive feedback [28-29]. The paper is organized as follows:

- Section 2 reviews the literature on OTA.
- Section 3 designs a proposed Differential OTA schematic with enhanced performance criteria.
- Section 4 presents a simulation and results in the analysis of the proposed two-stage OTA using the miller frequency

compensation technique.

- Section 5 discusses a comparative analysis of the proposed OTA with the existing one.
- Section 6 presents conclusions and the future scope of a proposed design.

This paper is concentrated on the Miller Frequency Compensation Approach for designing a low-power, two-stage OTA by reducing offset voltage and increasing its DC gain, and amplifying output voltage swing to 56.4 mV. The proposed technique achieves enhanced performance with low power of 1.9 nW and is implemented at low supply voltage ±0.2 V.

2. RELATED WORK

Advancements in noise performance, DC gain, size of transistors, and power consumption in acquisition systems have been published by several prior studies. The frequency compensation technique has been proposed with improved phase margin and analyzed the features of Miller OTA and Pseudo-Cascode OTA, which are both implemented with higher supply voltage and occupied more space in Zhao et al. [3]. Khameh et al. [9] presented a Fully Differential OTA at 180 nm CMOS technology with high DC gain. For battery-operated gadgets, high power consumption is a significant challenge. Miller Compensation Technique is introduced in Viswanathan et al. [13] analyzed using a ±0.9 V voltage and biasing current of 30 µA. Still, there is a lot of power utilization with more noise. Palmisano et al. [14] discuss well-defined optimization strategies of two-stage OTA bandwidth, essential characteristics such as DC gain, output swing, noise analysis, area occupied, and other electrical parameters, but are not significantly improved. According to Akbari et al.[8] [21], flicker noise and DC offset voltage are the main issues in designing OTA. A simple approach to reduce noise and increase DC offset voltage is using the Miller Compensation Technique.

3. PROPOSED OTA

An Operational Transconductance Amplifier is a Current Source with Voltage Control (VCCS), the OTA differential inputs could amplify a thousand times the signal at the output. Two-stage Operational transconductance amplifier is a combination of two stages as shown in Figure 1 has the following features:

- Differential Transconductance as the first stage
- A common source amplifier capable of improving gain and output swing voltage is the second stage.
- The Miller Frequency Compensation Circuit is used to promote system stability.
- The output buffer provides low output impedance whereas the second stage employs level shifting to improve gain.

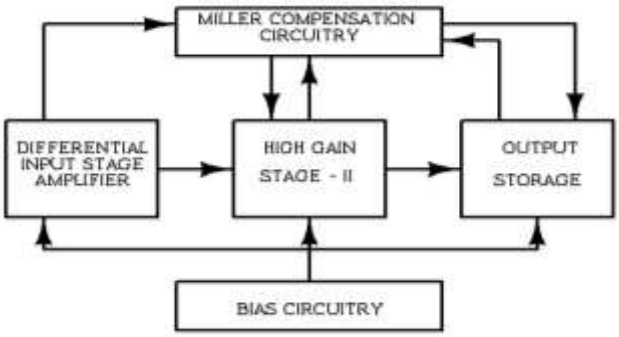

Figure 1. Block Diagram of Two-stage OTA

The proposed Miller compensation technique uses two capacitors as a compensation network. This technique uses a nulling resistor for erasing the RHP zero in the transfer function. Thus the phase margin has deteriorated.

The typical two-stage CMOS OTA comprises three subsections: Differential Gain Stage, High Gain Stage, and Bias Stage. This circuit requires a compensation technique using compensating capacitor connected with a high gain stage amplifier. The schematic representation of the two-stage OTA is given in Figure 2.

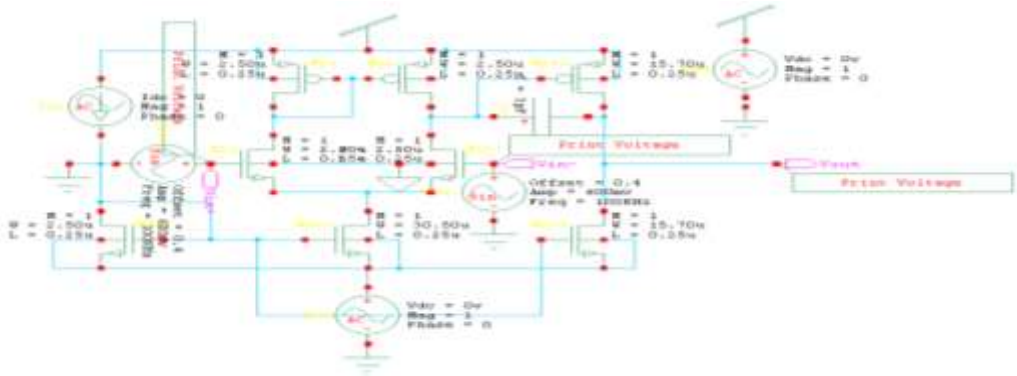

Figure 2. Schematic Representation of Proposed OTA

Table 1 defines design specifications for Proposed Two-Stage OTA as:
Table 1: Proposed Design Stipulations

Performance Parameters	Specifications
Process Technology	180 nm
Vin+, Vin-	±1 µV
Bias current Idd	20 µA
Vdd	0.2 V
Vss	-0.2 V
Leff	0.25 µm
CL	10 pF

Table 2 shows the transistor's sizing of the proposed OTA design as:

Table 2: Transistor aspect ratio (W/L) of the proposed OTA

Transistors used	W (µm)	L(µm)
Mn1, Mn2, Mp1, Mp2(Differential Amplifier)	2.5	0.25
Mn13, Mp11(Second-Stage CS Amplifier)	15.70	0.25
Mn11 (Mirror Amplifier)	2.5	0.25
Mn12(Tail Amplifier)	30.50	0.25

4. SIMULATION AND RESULT ANALYSIS

4.1 Time-Domain Transient analysis

The simulated transient analysis of differential inputs of Two-Stage OTA is shown in Figure 3.

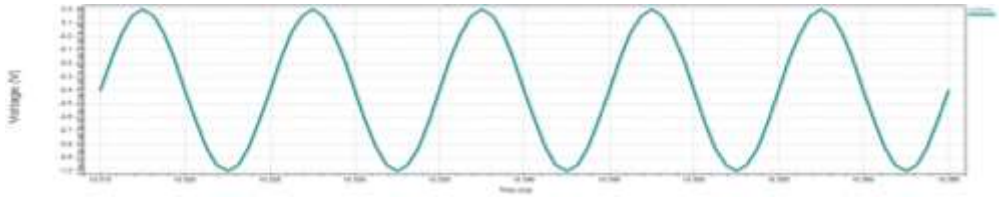

Figure 3. Simulated Transient Analysis of Inputs of Two-Stage OTA

The simulated output is shown in Figure 4 which is the inverse of input voltage with 180° phase shift.

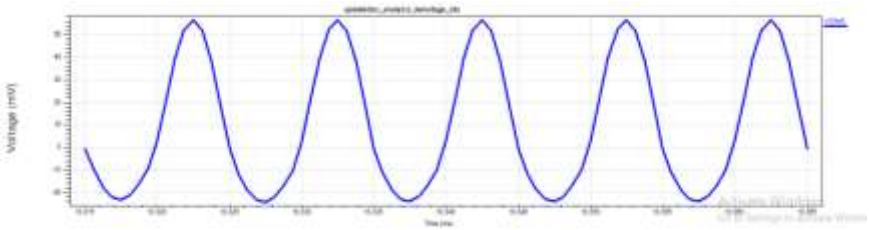

Figure 4. Simulated Transient Analysis of Two-Stage OTA

The input applied to Differential Two-Stage OTA is ±1 μV and is getting an output of 56.4 mV.

4.2 Power Analysis

Equation 1 shows the circuit's power consumption as:

$$P_{OTA} = 2V_{dd}\,(I_{stage1} + I_{stageII})(1+\alpha) \quad (1)$$

α is taken to be 0.2.

The power consumption of the proposed design across voltage sources Vin+ and Vin- are given in Table 3:

Table 3: Power Analysis of Proposed OTA

Voltage Sources (V)	Average Power (pW)	Max. Power (nW)
Vin+ (0 – 0.1)	1.21	1.9
Vin-(0 – 0.1)	1.17	1.9

Using the above design specifications, the simulated DC sweep analysis result is presented in Figure 5.

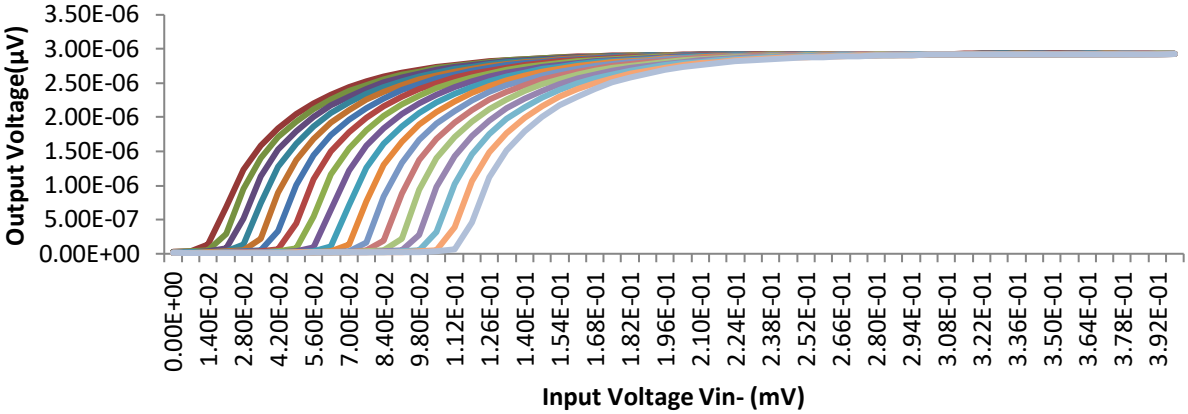

Figure 5. DC Transfer Characteristics of Two-Stage OTA

4.3 AC analysis

Using its designing strategies and specifications at 180nm CMOS process technology for differential mode has resulted in Figure 6. The ac analysis can be used to evaluate the resonance frequency, phase shift, Q-factor, power dissipation factor, and min and max impedance.

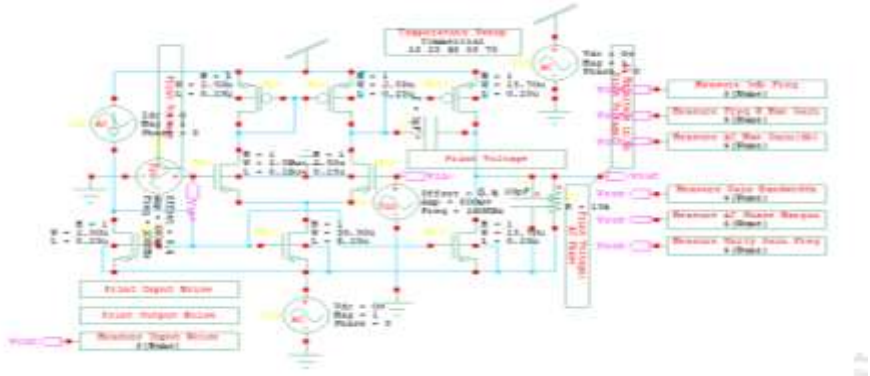

Figure 6. Schematic for AC Two-stage OTA

The following equation 2 defines the current parameter for saturated devices.

$$I_{dd} = \frac{K(Vgs - Vth)^2}{2[1+\theta(Vgs - Vth)]} \quad (2)$$

Here the value of K is represented by Equation 3

$$K = \mu_n \, Cox \left(\frac{W}{L}\right) \quad (3)$$

Here

K	:	Transconductance parameter
V_{gs}	:	Gate to Source voltage
V_{th}	:	Threshold voltage
μ_n	:	Electron mobility
Cox	:	Gate oxide capacitance per unit area
θ	:	Mobility reduction coefficient
W/L	:	Transistor Aspect Ratio

The designing procedure for two stages of operational transconductance is given as: firstly choose the device length L as 0.25µm used in all transistors of the circuit, but the device width of transistors may be changed. The value of compensation capacitor is calculated by using following Equations 4, 5, and 6 as:

$$Cc > 2.2/10 \, C_L \quad (4)$$

$$Cc > 2.2pF \quad (5)$$

$$Cc = 3pF \quad (6)$$

The transconductance of the input transistors is calculated by using formulas 7 and 8:

$$gm1 = \sqrt{\mu_n \, Cox \left(\frac{W}{L}\right) I_{dd}} \quad (7)$$

$$gm1 = gainbandwidth * C_C \quad (8)$$

The input signal oscillates at the slew rate of 6.67V/µ sec and is calculated using Equation 9.

$$SR = \frac{I_{dd}}{Cc} = \frac{20*10^{-6}}{3*10^{-12}} = 6.6 * 10^6 \quad (9)$$

The phase margin is represented as equation 10.

$$PhaseMargin(\psi m) = Arg[-A(jw0dB)F(jw0dB)] = Arg[L(jw0dB)] \quad (10)$$

To make the system much more stable and disallowing claiming of the circuit, the following condition (11) should be satisfied.

$$Argument[-A(jw0dB)F(jw0dB)] = Argument[L(jw0dB)] > 0^o \quad (11)$$

where w0dB is defined by Equation (12) as:

$$|L(jw0dB)| = |A(jw0dB)F(jw0dB)| = 1 \quad (12)$$

Stability is measured when the phase becomes |A(jw_0dB)F(jw_0dB)| = 1 Figure 7 and Figure 8 present the simulation of AC analysis of the proposed OTA.

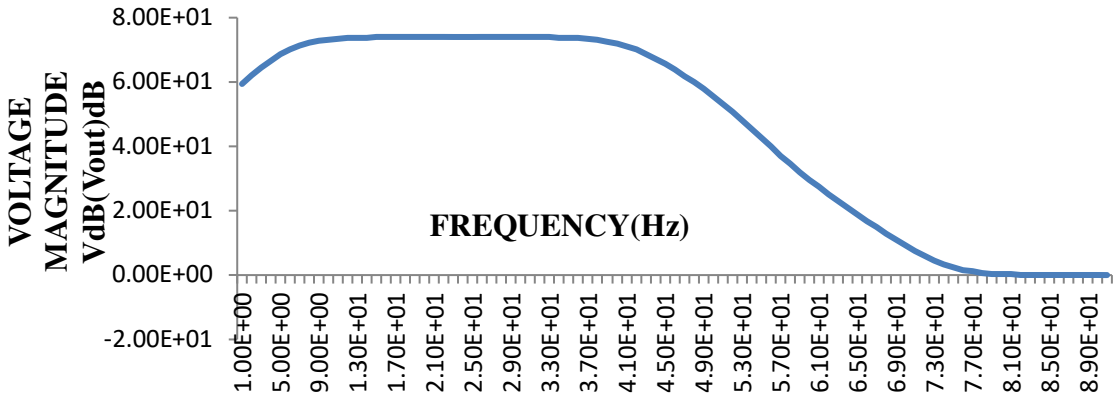

Figure 7. Simulated Gain Analysis Two-Stage OTA

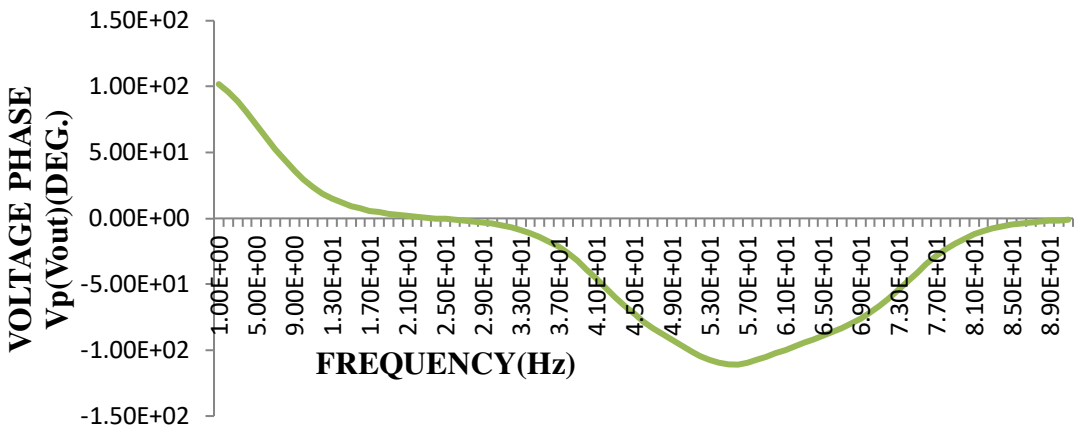

Figure 8. Simulated Phase Analysis Two-Stage OTA

4.4 Unity-gain Bandwidth

The Unity-gain bandwidth is given by equation (13):

$$\text{UGB} = \frac{G_m}{C_L} = \frac{\sqrt{\mu n\ \text{Cox}\ (\frac{W}{L})\text{Idd}}}{\text{CL}} \tag{13}$$

The Figure of Merit for evaluating better power-bandwidth efficiency of two-stage OTA's small-signal and large-signal performance is as follows in Equation 14:

$$\text{FOM}_{\text{OTA}} = \frac{\text{Gain Bandwidth} * C_L}{\text{Power consumed}} \tag{14}$$

4.5 Noise Analysis

The transistors used in differential mode give rise to noise in the device. The input-referred noise density of transistors in the sub-threshold region is defined using equation (15).

$$v^2{}_{niMOS} = \frac{4KTY}{G_m} = \frac{4KTV_T}{2k * k\, I_{dd}} = \frac{2KTV_T}{k * k\, I_{dd}} \tag{15}$$

Here,

K : Boltzmann's constant
T : Absolute Temperature
G_m : Transconductance of transistor
k : Sub-threshold slope coefficient of a MOS transistor
Y : Thermal noise coefficient

Gm is given as $G_m = \frac{KI_{dd}}{V_T}$

Equation (16) defines the noise efficiency factor (NEF) as a standard representation of the noise-to-power trade-off for low-noise amplifiers.

$$NEF = v_{nirms}\sqrt{\frac{2I_{dd}}{\Pi * BW * 4KT * V_T}} \quad (16)$$

Here,

v_{nirms} : Input-referred noise of the amplifier
V_T : Thermal voltage
I_{tot} : Total current flows through the input devices

$v^2{}_{niMOS}$ also rewritten as in Equation (17).

$$v^2{}_{niMOS} = v^2{}_n * \frac{\Pi}{2} BW \quad (17)$$

By the analytical analysis of the above-defined equations, the input noise of proposed OTA is represented in Figure 9.

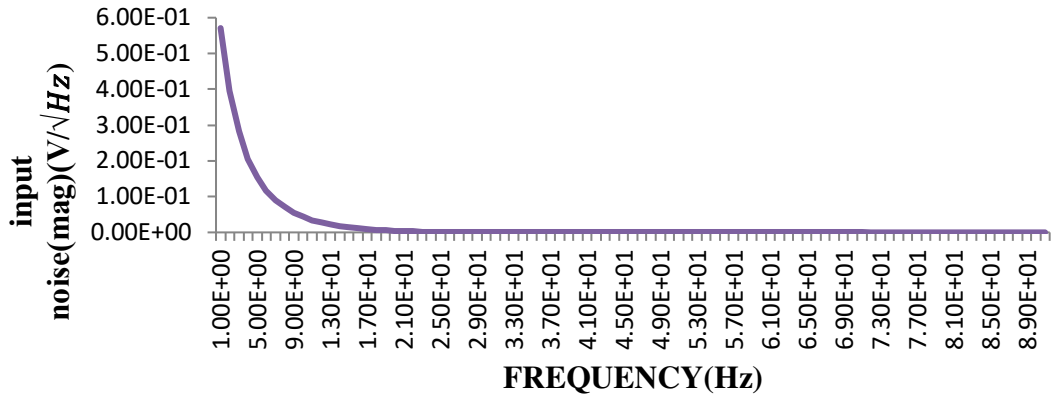

Figure 9. Simulated Input Noise Analysis of Two-stage OTA

The OTA's dynamic range is determined by the noise plot. By integrating output noise, the total output noise is calculated and represented in Figure 10.

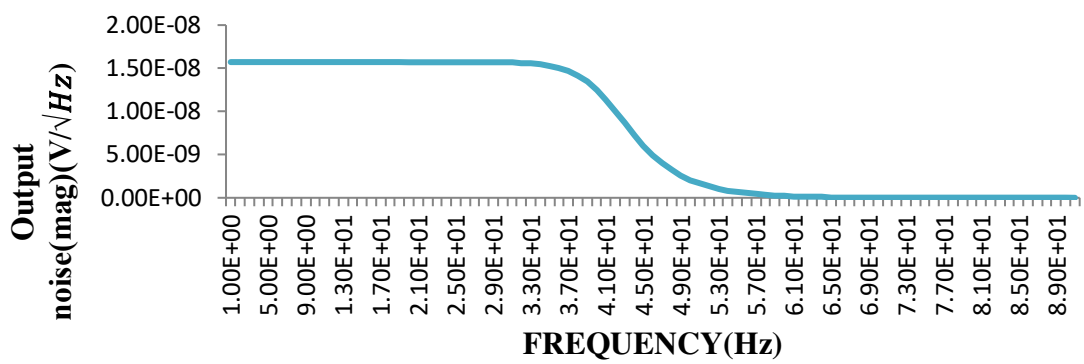

Figure 10. Simulated Output Noise Analysis of Two-stage OTA

The simulated noise PSD of the proposed OTA is $4.54 * 10^{-4}$ and is shown in Figure 11.

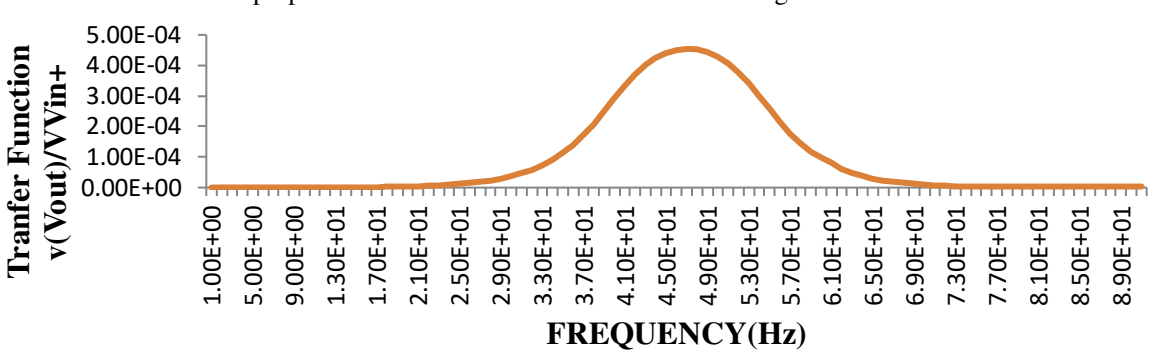

Figure 11. Simulated noise PSD of two-Stage OTA

4.6 Temperature analysis

Table 4 shows the performance parameters of AC analysis based on temperature influences and simulated result behavior represented in Figures 12, Figure 13, and Figure 14.

Table 4: Simulated performance parameters under AC analysis with temperature variations

The temperature used(o)	AC Measure Gain(dB)	AC Measure Phase Margin (o)	AC Measure Unity Gain Freq(Hz)	AC Measure 3db Freq (Hz)	AC Measure Gain Bandwidth Product(Hz)	NOISE Measure Output Noise(V/$\sqrt{Hz}$)
10	74.0	88.6	$9.3 * 10^{10}$	$1.03*10^{6}$	$6.8*10^{12}$	$1.8*10^{-4}$
25	73.9	88.6	$9.23*10^{10}$	$1.04*10^{6}$	$6.8*10^{12}$	$1.87*10^{-4}$
40	73.9	88.6	$9.15*10^{10}$	$1.04*10^{6}$	$6.77*10^{12}$	$1.94*10^{-4}$
55	73.9	88.6	$9.05*10^{10}$	$1.04*10^{6}$	$6.7*10^{12}$	$2.0*10^{-4}$
70	73.9	88.6	$8.9*10^{10}$	$1.04*10^{6}$	$6.6*10^{12}$	$2.1*10^{-4}$

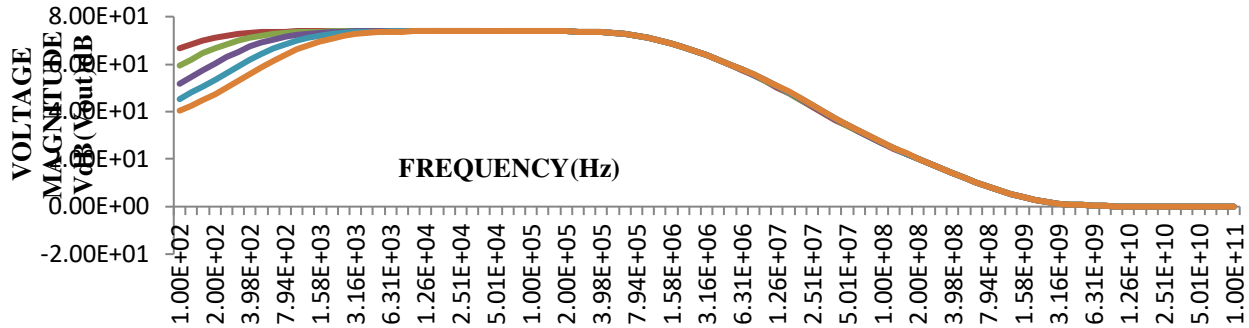

Figure 12. Gain Analysis with Temperature variations

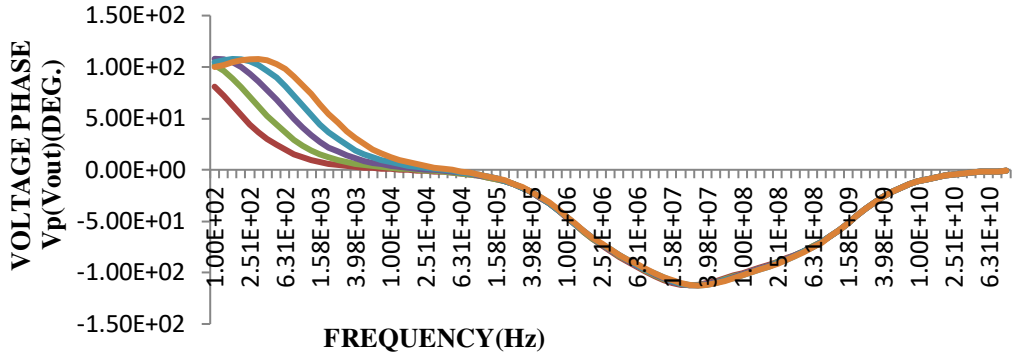

Figure 13. Phase Analysis with Temperature variations

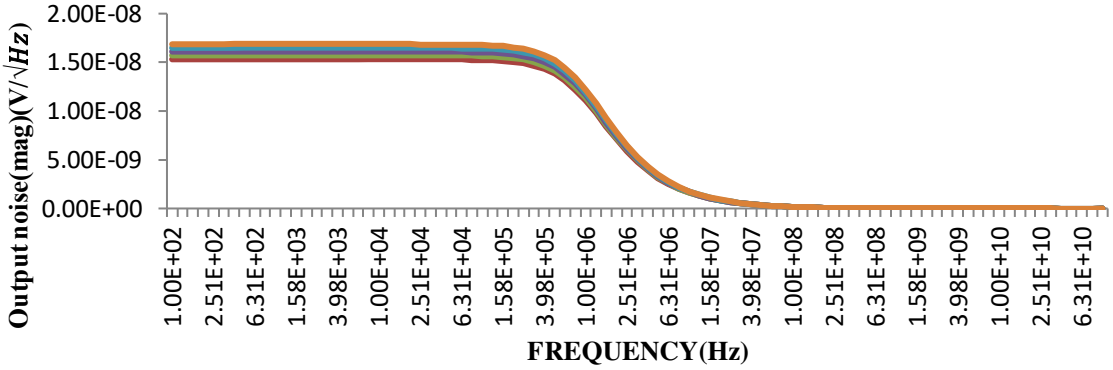

Figure 14. Simulated Output Noise Analysis with temperature variations

4.7 Time Delay Parameter Response

Table 5 shows the Time Delay Parameter of the Proposed OTA.

Table 5: Time Delay parameters

Delay parameters	Time (in seconds)
Parsing delay	0.01
Set-up time	0.01
DC-operating point	0.22
DC Analysis	0.62
Transient Analysis	1.73
Overhead	4.48
Total	7.07

5. LAYOUT DESIGN

A low-power, low noise front end device is fabricated using 180nm CMOS process technology and its layout design is shown in **Figure 15**. In this design layout, NMOS is used in a cross-coupled feature with occupying area having dimensions X= 58.320µm and Y=40.000µm. The most of area of the layout is utilized in dummy fillings. The complete design layout is surrounded by a group of guard rings to remove noise spikes in device performance. For compressing the size of MOSFETs, divide the width of MOSFETs by increasing the number of figures as gate or poly in the device.

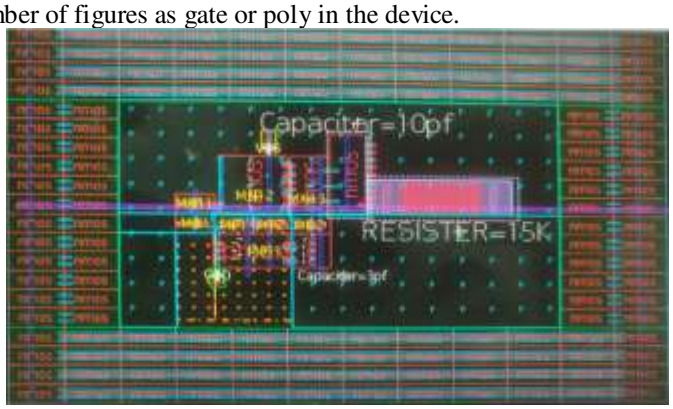

Figure 15. Layout Design of Two-stage OTA

The layout is designed by considering the following specifications given in Table 6.

Table 6: Layout Specifications

Transistors used	Width (W)	Length (L)	NF(Number of Figures)
Mn1, Mn2, Mp1, Mp2(differential amplifier)	2.5µm	0.25µm	1
Mn13, Mp11(second-stage CS amplifier)	5.23µm	0.25µm	3
Mn11 (Mirror-amplifier)	2.5µm	0.25µm	1
Mn12 (Tail amplifier)	5.08µm	0.25µm	6
Mn13(second-stage CS amplifier)	2.615µm	0.25µm	6

6. COMPARATIVE ANALYSIS

Table 7 summarizes the simulation results and compares them to past research. In comparison to prior similar works conducted utilizing 180 nm CMOS process technology with Tanner EDA, the proposed designed amplifier achieves a favorable performance with minimal NEF despite operating at reduced power.

Table 7: Comparison of Proposed Two-stage OTA with Prior Two-stage OTAs

Performance features	[3]	[11]	[12]	[13]	Proposed
Process technology	180 nm	180 nm	180 nm	180 nm	180 nm
Gain	63 dB	39.2 dB	46.5 dB	70 dB	73.9 dB
Phase margin	54.4°		75°	68°	88.6°
Supply voltage	±0.5	±1.2	±2.5	±0.9V	±0.2V

	V	V	V		
Power			0.403 mW	0.26 mW	1.9 nW
Compensation Capacitor(Cc)	2.3pF		3pF	3pF	3pF
Load Capacitor (CL)	15pF				10pF
Bias current	20nA	2µA		30µA	20µA
Unity gain BW	4.5 KHz	28KHz	9.9 MHz	5.6 MHz	6.8e+010
Differential inputs				±1mV	±1µV
Differential Output				150mV	56.4 mV

In [3] paper, an enhanced Pseudo-Cascode technique is implemented to improve phase margin, whereas the proposed technique uses MOSFET devices having a small channel length of 0.25 µm which consumes less area with high gain at minimal power requirement. The proposed design gives an improved output swing of voltage 56.4 mV at small input differential voltage ±1µV, while [13] gives 150mV at ±1mV. The improved performance parameters are observed in decreasing the channel length of MOSFETS. **Figure 16** represents a comparative gain analysis of OTAs with different methodologies.

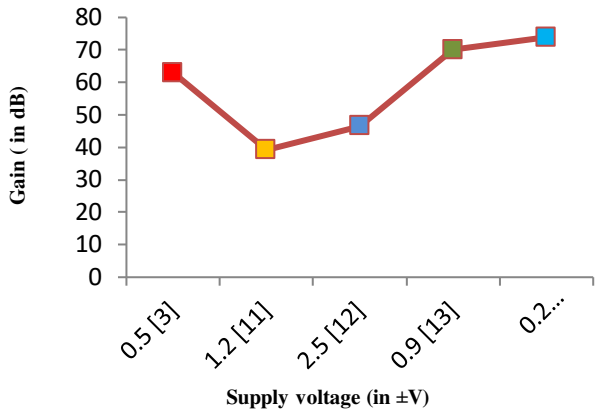

Figure 16. A Comparative Gain analysis of Existing and Proposed OTA versus Supply voltage

The proposed OTA achieves the best gain of 74 dB as compared to the existing OTA on basis of their corresponding supply voltage. The supply voltage used in the proposed OTA is ±0.2V is very much less than the voltages of existing OTAs. The phase margin 88.6° achieved using the proposed designed OTA is better than the existing ones as shown in **Figure 17.**

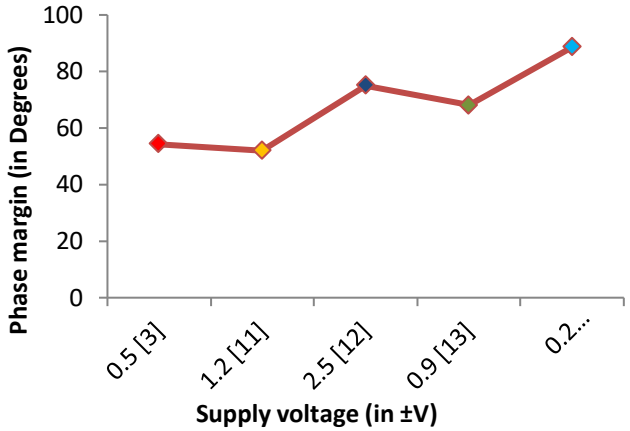

Figure 17. A Comparative Phase analysis of Existing and Proposed OTA versus Supply voltage

In paper [3], the Miller compensation technique is implemented with a channel length of 1.0 µm, and the Supply voltage of 0.5 V resulted in ~ 65 dB gain. Two-stage OTA based on capacitive feedback is presented in paper [11] with a supply voltage of 1.2 V and channel length of 2µm consumes 2.4µW power with input-referred noise of 5.79 µ Vrms and achieves ~ 40 dB gain. whereas, the proposed OTA analyzed using the Frequency compensation technique achieves ~74 dB gain by using 0.2 V supply voltage. Because of the small channel length with low supply voltage, the proposed design consumes much less power of 1.9 nW

as compared to different existing OTAs.

7. CONCLUSION AND FUTURE SCOPE

In this paper transient time-domain analysis, AC analysis, temperature analysis, power, and noise analysis of the proposed OTA are implemented in an improved manner. The Tanner EDA simulations show the better performance of the device. After analyzing the above results obtained, one can conclude that

1. The proposed Two-Stage OTA uses the Miller Frequency Compensation technique at ±0.2 V supply voltage consumes low power of 1.9nW and results in a reduction of noise parameters.
2. The comparative performance of the two-stage OTA was designed with 180nm CMOS process technology with a gain of 74dB, phase margin 88.6o, 3dB frequency $1.04*10^6$ Hz, and $1.87 *10^{-4}$ V/$\sqrt{\text{Hz}}$ output noise.
3. Minimizing the occupied area, reducing noise with low power consumption, and high gain are recommended to be employed using the proposed technique.

It is also recommended to explore multi-stage differential OTA and other low-power design analyses. These modeling results may inspire researchers to improve the experimental realization of multistage OTAs.

DATA AVAILAIBILITY:

The datasets generated during or analysed during the current study are available from the corresponding author on reasonable request.

AUTHORS' CONTRIBUTION:

Jyoti Sehgal, Manoj Kumar : original draft, Methodology, Software: Designing schematic, make its code and get simulated results, Conceptualization, Writing- review and editing.

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