Power Efficient Model of PWM Generator for Green Computing and Communication on High Performance FPGAs

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Abstract

PWM generator is one of the core modules of a communication model. Its main function is to control the amplitude of signal and used for reducing average power of the pulses and signals. The PWM generator can also be used in promoting the green computing and green communication other than data and wireless communication if it is made power and energy efficient. In this work we are using different Stub Series Terminated Logic (SSTL) IO with three distinguished FPGAs of different Nano meter (nm) gate size that are 28 nm SPARTAN-7, 20 nm KINTEX-7 Ultra scale, and 16 nm ZYNQ Ultra scale+. The model has been synthesized and implemented on VIVADO ISE tool. From the power analysis it is observed that 16 nm ZYNQ Ultra scale+ requires the highest amount of power for operation with SSTL18_I IO and 28 nm SPARTAN-7 uses least amount of power for the operation with SSTL135 IO, while the 20 nm KINTEX-7 Ultra scale lies in mid of both of these devices.

Full Text

Due to technical limitations, full-text HTML conversion of this manuscript could not be completed. However, the latest manuscript can be downloaded and [accessed as a PDF](#).

Figures

Figure 1

Generation of PWM waves

Figure 2

Generation of PWM waves

Figure 3

Pulse waveform with low value $y_{\min}$, high value $y_{\max}$, and D [5]

Figure 4

Building design of FPGA

Figure 5

Efficient model for green communication

Figure 6

RTL of PWM generator

Figure 7

The implementation process on FPGA

Figure 8

Post implementation resources utilization

Figure 9

Post implementation resources utilization

Figure 10

Post implementation resources utilization

Figure 11

IO standard based communication model

Figure 12

Internal architecture of SSTL [52]

Figure 13

Total Power consumption for SSTL135

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.635 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.5°C
Thermal Margin:	73.5°C (29.9 W)
Effective θ_{JA} :	2.4°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

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On-Chip Power

Figure 14

Total Power consumption for SSTL15

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.637 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.6°C
Thermal Margin:	73.4°C (29.9 W)
Effective θ_{JA} :	2.4°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

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On-Chip Power

Figure 15

Total Power consumption for SSTL18_I

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 0.64 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.6°C
Thermal Margin: 73.4°C (29.9 W)
Effective θ_{JA} : 2.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

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On-Chip Power

Figure 16

Total Power consumption for SSTL18_II

Figure 17

TP for SPARTAN-7

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 1.04 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.5°C
Thermal Margin: 73.5°C (50.2 W)
Effective θ_{JA} : 1.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

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On-Chip Power

Figure 18

Total Power consumption for SSTL135

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 1.041 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.5°C
Thermal Margin: 73.5°C (50.2 W)
Effective θ_{JA} : 1.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

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On-Chip Power

Figure 19

Total Power consumption for SSTL15

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 1.042 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 26.5°C
Thermal Margin: 73.5°C (50.2 W)
Effective θ_{JA} : 1.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

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On-Chip Power

Figure 20

Total Power consumption for SSTL18_I and SSTL18_II

Figure 21

TP for KINTEX-7 Ultra scale

ummary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.094 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 27.6°C
Thermal Margin: 72.4°C (30.0 W)
Effective θ_{JA} : 2.4°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

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Figure 24

Total Power consumption for SSTL18_II

Figure 25

TP for ZYNQ Ultra scale+ SoC

Figure 26

TP consumption for various FPGA and SSTL IO