Hetero - Gate Oxide Dual Metal Vertical Tunnel FET

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Abstract

A Silicon based Vertical Dual metal Double gate Tunnel FET (Si-VDMDGTFET) has been proposed and simulated in Sentaurus TCAD tool with improved DC and analog/RF characteristics. The vertical In-line tunneling dominates in the proposed device which results in better subthreshold slope (SS). The vertical in-line tunneling tunes the tunneling barrier and eventually controls the ON current. The dual metal gate and the heterogeneous gate stack oxide within the proposed device design gives the mouldability for controlling and improving the DC characteristics such as ON current, OFF current. The analog/RF behaviour of the proposed device has been calculated and compared with conventional lateral Silicon based dual metal double gate Tunnel FET furthermore it is seen that the proposed device outperforms the conventional lateral device.

Introduction

Tunnel FET (TFET) is one of the capable contenders in the CMOS technology due to the factor that it has the ability to overcome the thermionic limitation of subthreshold swing (SS). It is the one of the candidate to reduce the supply voltage VDD and the power consumption. Rigorously continuous scaling down of the conventional CMOS for improving the current driving capability, increase in device density, cost saving and improved RF performance has led to the deterioration in its performance [20]. Due to the non-scalable of subthreshold swing of MOSFET which is below 60mV/decade it is not capable to achieve the requirements of low power applications. Due to this Tunnel FET comes into the limelight. In Tunnel FET the charge carrier transportation is build on mechanism of band-to-band tunneling (BTBT) which is the quantum tunneling mechanism instead of the thermionic emission which helps to overcome the limitations of MOSFETs. It is independent to the Boltzmann distribution since the function tail is detached [10,24-27].

The transportation of charge carriers in Tunnel FET is based on BTBT mechanism which is independent of the Boltzmann distribution and thermionic emission. It is the unidirectional and ambipolar devices. The same device acts as both n-type and p-type by changing the polarity of the applied voltages. But the ON state driving current of the conventional planar p-i-n TFET structure is low, which is not acceptable in the applications of low power. For improvising the driving ON state current various different structures have been presented such as double gate TFET (DGTFET), Dual metal TFET structure [2-3], SOI TFET structure [15-16], SOI TFET with ground plane [4] which improves the ON driving current, transconductance (g_m) and minimizes the OFF current. The SOI structure reduces the leakage current but it increases the fabrication cost. Using the lower bandgap material for the fabrication of the different structures of TFET not only increases the fabrication cost but also increases the OFF-state leakage current and the tunneling efficiency in the reverse direction in the form of ambipolar leakage current [11-12]. So, TFET suffers from a forthcoming problem of optimization of the subthreshold swing and I_{ON}/I_{OFF} simultaneously.

For this reason this paper focuses to study a TFET for applications of low power, which can reimburse the weak points of TFET which was discussed earlier. A Silicon based Vertical Dual Metal Double Gate

TFET (Si-VDMDGTFET) with stacked dielectric oxide has been introduced. In the VDMDGTFET the channel is vertical and the tunneling direction is perpendicular to the channel which results in steeper switching characteristics. The switching of the vertical TFET occurs by regulation of the energy band edges. The tunneling window is either induced or removed amid the source and the channel layers or the drain and the channel layers for switching the device ON and OFF. The device shows reduced SS, reduced threshold voltage, improved tranconductance and improved I_{ON}/I_{OFF} ratio which makes it appropriate for applications of low power. Furthermore, due to the improvement in its RF parameters the device demonstrates its usability for applications in circuits of high frequency.

Device Structure

Fig 1 (a) portrays the Silicon based Vertical Dual Metal Double Gate TFET (Si-VDMDGTFET). In the structure the source region is overlapped by the gate. A thin silicon channel layer is interposed in between the source layer and the gate oxide. The proposed structure has gate stacked heterogeneous oxide. Using high-k dielectric gate oxide below the gate electrode helps to reduce the leakage current. But using high-k dielectric gate oxide over the Silicon layer creates the undesirable effect of likely large concentration of interface defects at the interface of high-k/Silicon which results from the large lattice-mismatching between the Silicon layer and the high-k dielectric which is below the gate electrode of the TFET [3-4]. So we use heterogeneous gate stacked oxide. The high-k gate dielectric (HfO_2) is stacked over the thin layer of SiO_2 . Further, the gate electrode comprises of metals with different work function that is Tunnel Gate (TG), Controlling Gate (CG) and Auxiliary Gate (AG). The metal gate near the source is known as the tunnel gate (TG); it tunes the energy band of the source and channel regions which helps in tunneling the carriers from the region of source to channel as a result there is increase in the ON current. The metal gate near the drain side is the Auxiliary gate (AG) which helps to keep the OFF state current minimum. The control gate (CG) is the metal gate between the TG and AG. The work-function of the TG is taken low than the two gates to achieve higher I_{ON} , lower I_{OFF} and improve the subthreshold swing (SS) [2-3, 16].

Table 1 Device Parameters

Parameters		Symbol	Si-DMDGTFET	Si-VDMDGTFET
Length of Channel(nm)		L_{Ch}	50	20
Length of Source (nm)		L_S	50	80
Length of Drain (nm)		L_D	50	50
Gate oxide thickness	SiO ₂ (nm)	T_{SiO_2}	0.8	0.8
	HfO ₂ (nm)	T_{HfO_2}	1.2	1.2
Silicon layer thickness (nm)		T_{Si}	10	10
Doping concentration of Source (cm ⁻³)		N_S	1×10^{20}	1×10^{20}
Doping concentration of Drain (cm ⁻³)		N_D	1×10^{19}	1×10^{19}
Doping concentration of Channel (cm ⁻³)		N_{Ch}	1×10^{17}	1×10^{17}
Tunnel Gate Work function (TG) (eV)		Φ_{TG}	4.0	4.0
Auxillary Gate Work function (AG) (eV)		Φ_{AG}	4.4	4.4
Control Gate Work function (CG) (eV)		Φ_{CG}	4.0	4.0
Length of Tunnel (nm)		L_{TG}	10	30
Length of Auxillary Gate (nm)		L_{AG}	25	15
Length of Control Gate (nm)		L_{CG}	15	5

For the conventional Si-DMDGTFET structure the length of the source (L_S), channel (L_{Ch}) and drain (L_D) is 50nm respectively, the tunnel gate (L_{TG}), the control gate (L_{CG}) and the auxiliary gate (L_{AG}) lengths are 10nm, 25nm and 15nm respectively. However, for the structure of Si-VDMDGTFET the source length (L_S) is 80nm, the channel length (L_{Ch}) is 20nm, the drain length (L_D) is 50nm , the tunnel gate length (L_{TG}) is 30nm, the control gate length (L_{CG}) is 15nm and the auxiliary gate length (L_{AG}) is 5nm . The high-k dielectric constant HfO₂ whose $k = 29$ is choosen as the high k dielectric to improvise the coupling between the junction of gate and tunnel. The gate has more control over the tunnel junction by the using of the high-k dielectric gate oxide. But directly placing the high-k dielectric over the Silicon substrate creates the lattice mismatch between the Silicon/high-k interfaces. So a thin layer of SiO₂ is inserted between the Silicon and the high-k dielectric HfO₂. The heterogeneous gate stacked oxide helps better coupling of the gate/tunnel junction which leads to the enhancement in the I_{ON} and SS. The work functions of TG, CG and AG is 4.0eV (Metal 1), 4.5eV (Aluminum) and 4.0eV (Molybdenum) respectively.

The work function engineering of the TG, CG and AG also helps to optimize the performance of the device constraints such as I_{ON} , I_{OFF} and SS.

The simulations are carried in the Sentaurus TCAD tool [22]. The tunneling at the junction of the source/channel is integrated by including the nonlocal BTBT model. The Shockley-Read-Hall (SRH) model in company with the Auger Recombination model is employed for the recombination effect. The models such as Lombardi mobility and the drift-diffusion are employed for the conventional flow of charge carriers [29].

The process of fabrication to obtain the proposed Si-VDMDGTFET is illustrated in Fig 2. A N^+ Silicon substrate is taken. A photoresist mask is employed to describe the source area and eventually implantation of P^+ is done. A low temperature epitaxial development of 2nm Si having concentration and the doping type like the N-type region is done in-situ [28]. After that the heterogeneous gate stacked oxide and the metals of the required work function are created. The Tilt Angle Evaporation (TAE) method is used for the formation of the dual metal gates [29]. After that the drain is defined and like the source region the implantation of N^+ is done and for the dopant activation rapid thermal processing is done. Afterward the metallization of the source and the drain is done.

Results And Discussion

The comparison of the energy band diagram between the proposed device and the Si-DMDGTFET at thermal equilibrium ($V_{GS} = 0$ V and $V_{DS} = 0$ V) is depicted in Fig 3(a) and at ON state ($V_{GS} = 1$ V and $V_{DS} = 1$ V) is depicted in Fig 3(b). At thermal equilibrium, when no voltage is applied at the gate ($V_G = 0$ V), the aperture in between the valence energy band (VB) and the conduction energy band (CB) of the source and channel respectively, is too much, so the charge carriers are not able to tunnel between the source and the channel, thus the device remains OFF. When V_G increases the valence band edge of the source moves downward towards the channel's conduction band edge, thus, there is narrowing of the energy band between the source/channel junction and the tunneling of carrier occurs between the source/channel junction and thus current flows and the device turns ON. The electric field is highest at this source/channel junction. The tunneling width at the source/channel junction of the proposed device is less thus resulting in the improved ON-current.

Fig 4 depicts the carrier generation of the Si-DMDGTFET device and the proposed Si-VDMDGTFET device. In case of Si-VDMDGTFET device the concentration of the carrier occurs at the Si-epitaxial layer of source/gate interface. In the proposed device the tunneling pathway is orthogonal and is all beneath the gate. Due to this, the degradation of SS occurs because the diagonal tunneling path is minimized. Contrary, the tunneling in Si-DMDGTFET takes place only at the periphery of the gate which is at the interface of source and channel.

Fig 5 depicts the comparison of the transfer characteristics of the Si-DMDGTFET and Si-VDMDGTFET at the ON state.

Table 2 compiles the results of DC characteristic of Si-DMDGTFET and Si-VDMDGTFET devices.

Table 2 DC characteristics

Parameters	Si-DMDGTFET	Si-VDMDGTFET
I_{ON} (A/ μ m)	2.26×10^{-8}	2.51×10^{-6}
I_{OFF} (A/ μ m)	1.22×10^{-16}	1.81×10^{-17}
I_{Amb} (A/ μ m)	3.51×10^{-15}	7.98×10^{-16}
I_{ON}/I_{OFF}	1.89×10^8	1.39×10^{11}
g_m (S)	8.19×10^{-8}	4.57×10^{-8}
DIBL	0.009	0.002
SS (mV/dec)	62	48

The amplification capability is described by the transconductance (g_m) of a device. The device whose transconductance is higher is preferred because the conversion of input voltage into output current is better. Transconductance is computed as

$$g_m = \partial I_{DS} / \partial V_{GS} \quad (1)$$

Fig 7 depicts that Si-VDMDGTFET has better responsiveness to convert the input voltage into drain current in comparison to the Si-DMDGTFET.

The effectiveness of Si-VDMDGTFET in the applications of RF is analyzed. When the device works at high frequencies, while determining the AC behavior the parasitic capacitances allied with the device have a vital job. The pathway between the input and the output is created by these parasitic capacitances whose outcome is signal distortion and circuit oscillation. The gate to drain capacitance (C_{GD}) governs the total gate capacitance (C_{Total}) relatively than the gate to source capacitance (C_{GS}), hence it is vital to minimize the C_{GD} for improvement in RF performance.

Fig 8 depicts the C_{GD} vs V_{GS} at $V_{DS} = 0.5$ V. The injection of carriers to gate from drain originates C_{GD} . The C_{GD} increases with increase in V_{GS} because an inversion layer is formed from the drain region to source which reduces the energy barrier width at drain. Fig 9 depicts the C_{GS} vs V_{GS} at $V_{DS} = 0.5$ V. The C_{GS} reduces with the increase in V_{GS} because at the source side the potential barrier increases leading to the reduction of the coupling at the source and gate electrode. Si-VDMDGTFET has higher C_{GS} than the Si-DMDGTFET. The sum of C_{GD} and C_{GS} is the total capacitance (C_{Total}) that is depicted in Fig 10. Si-VDMDGTFET has improved electrical performances as its overall capacitance is less.

The different Figure of Merits (FOMs) such as transconductance (g_m), cut of frequency (f_T), Transconductance Frequency Product (TPF), transit time (τ) and Gain Bandwidth Product (GBP) have been studied that is vital in understanding the device performance regarding the RF applications.

The frequency at which the device's short circuit current gain becomes unity is known as the cut-off frequency. It is computed as

$$f_T = g_m / (2 \pi (C_{GS} + C_{GD})) \quad (2)$$

f_T results from the collective effect of C_{GD} and reduction in g_m owing to mobility degradation. The f_T of Si-VDMDGTFET is 0.36 GHz which is considered appropriate for RF applications of high frequency. The Gain Bandwidth Product (GBP) of the device is formulated as

$$GBP = g_m / (20 \pi (C_{GD})) \quad (3)$$

GBP is the trade-off between gain and bandwidth of the device. The GBP of the proposed Si-VDMDGTFET is better than Si-DMDGTFET because of the similar cause as that of f_T .

Transit time (τ) is the time needed by the device to transport the charge carriers to drain from source. τ decreases as V_{GS} increases because an inversion layer is considerably incremented and the charge carriers pass through the reduced layer of the inversion layer. τ is computed as

$$\tau = 1 / 2\pi f_T \quad (4)$$

It is observed that Si-VDMDGTFET device has less transit time which implies that its switching speed is high.

Transconductance frequency product (TPF) is also a significant parameter for inspecting the functioning of the device at high frequency. It is computed as

$$TPF = (g_m / I_{DS}) * f_T \quad (5)$$

Table 3 summarizes the result of AC characteristics.

Table 3 AC characteristics

Parameter	Si-DMDGTFET	Si-VDMDGTFET
C_{GD} (F)	4.07×10^{-15}	9.23×10^{-16}
f_T (Hz)	3.1×10^6	3.6×10^8
GBP	3.2×10^5	7.8×10^7
τ (sec)	5.13×10^{-9}	4.42×10^{-11}
TFP	1.12×10^7	6.6×10^8

Conclusions

A dual metal DGTFET with the channel incorporated between the source and the gate oxide where vertical (in-line) tunneling occurs is studied. There is improvement in the DC and analog/RF characteristics when compared to the conventional lateral Si-DMDGTFET. The proposed device has better transconductance and reduced total capacitances (C_{Total}). DC constraints are as follows: I_{ON} is increment by 1.1×10^2 times, I_{OFF} and I_{Amb} is decremented, I_{ON}/I_{OFF} ratio is improved by 10^3 times, SS reduced by 15. RF constraints enhancement is as follows: g_m is incremented by 10^2 times, f_T incremented by 10^2 times, GBP incremented by 2×10^2 times, τ reduced by 10^2 times, TFP is increased, C_{Total} reduced by 0.48 times. From the result it is clear that the proposed device shows outstanding characteristics for applications of low power and RF.

Declarations

I would like to submit the manuscript “**Hetero - gate oxide dual metal Vertical Tunnel FET**”.

I affirm that this manuscript is original, has not been published before and is not currently being considered for publication elsewhere.

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Author’s Contribution - The first author is a Doctoral research scholar at the National Institute of Technology, Rourkela, India and the second author is the supervisor of his Ph.D. programme. All the authors have jointly contributed to this research. As the authors are student and guide respectively, the contributions of all towards the preparation of manuscript are significant.

Compliance with ethical standards - The authors confirm that the manuscript has not been submitted to any other journal for consideration of publication. This article does not contain any studies involving animals or human participants performed by any of the authors.

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Figures

Figure 1

(a). Device design of Si-VDMDGTFET. (b). Device design of Si-DMDGTFET

Figure 2

Fabrication process of the proposed device

Figure 3

(a). Energy band diagram at thermal equilibrium. (b). Energy band diagram at ON-state.

Figure 4

(a). Carrier generation of Si-VDMGTFET. (b). Carrier generation of Si-DMDGTFET.

Figure 5

Transfer characteristics at $V_{DS} = 1.0$ V

Figure 6

Output transfer characteristics at $V_{GS} = 1.0$ V

Figure 7

Transconductance (g_m) vs V_{GS} at $V_{DS} = 1$ V

Figure 8

CGD at VDS = 0.5 V

Figure 9

C_{GS} at $V_{DS} = 0.5$ V

Figure 10

C_{Total} at $V_{DS} = 0.5$ V