

Application of Intermediate CMOS Layer-based Defected Ground Structure to Design a Dual-Band On-chip Antenna with Improved Gain

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Application of Intermediate CMOS Layer-based Defected Ground Structure to Design a Dual-Band On-chip Antenna with Improved Gain

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Abstract In this paper, a novel CPW-fed dual-band on-chip antenna (OCA) by introducing a Crossed Bowtie shaped Defected Ground Structure (CB-DGS) in one of the intermediate layers of the CMOS layout is proposed. In general, a CPW fed OCA has its ground plane on the same plane of antenna, however, introducing a DGS in one of the intermediate layer using Through Silicon Vias (TSVs) to obtain dual band characteristics of antenna as well as to improve its gain is performed in this work. A 10 dB operating band of 9 GHz (2.25 GHz – 11.75 GHz) is obtained by employing the meandered loop miniaturization technique on the antenna designed on top CMOS layer, while the introduction of DGS layer enforced a comparatively less stop band at the middle of the operating band and the resultant structure offered a dual-band resonance characteristic at 3.1 GHz and 10.4 GHz. Here, the intermediate DGS layer between the top-layered antenna and Silicon (Si) wafer reduces the substrate loss by preventing the coupling of the electromagnetic radiation with the substrate and enhances the antenna gain significantly at both the resonance frequencies respectively by +16.01 dB and +12.7 dB. A prototype of the proposed antenna structure is fabricated and the obtained simulated result is validated through experimental measurement.

Keywords On-chip Antenna · Defected Ground Structure · Dual Band Antenna · Gain Improvement

1 Introduction

In the last 20 years, the rapid scaled down of the CMOS technology node from 130 nm to 2 nm paves the way to realize more compact system on chip

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(SoC) devices [1]. However, along with the other circuit components of a system, the integration of comparatively bulky and oversized components like antenna on the same chip is still a challenging task. For integrating different circuit module of a system, silicon (Si) wafer is preferred by the IC firms due to its low cost, abundance availability, and economical manufacturing process of ICs. In contrary, high dielectric constant ($\epsilon_r=11.9$), and low resistive ($\rho = 5-10 \Omega.cm$) properties of Si have adverse effect on the antenna radiation characteristics. The high dielectric constant attracts the electro-magnetic (EM) wave towards the substrate instead of radiation in the free space while the low resistivity leads to substrate loss and results in low gain and efficiency of the antenna. Meanwhile, various methods are reported to suppress the substrate loss. Among them, one is the replacement of Si with other substrates like, GaAs [2,3,4], SiGe [5,6], Polyimide [7]Silicon on Insulator (SoI) [8,9,10]. However, the replaced alternative substrates are not only uncommon among the IC design foundries but also are quite expensive. High resistive Si with incorporation of through silicon vias (TSVs) can be used to miniaturize the size and enhance the gain of OCA [11]. Silicon lens [12] and dielectric resonators [13,14], are also employed in this regard. Another method of reducing substrate loss is to exploit the multiple intermediate metal layers of the CMOS technology. In [15,16], meta-material surfaces are used as artificial magnetic conductor layers which reflect the in-phase waves towards the antenna and enhance the radiation. In [17], an additional intermediate conductor layer along with on-chip ground layer is utilized and the gain enhancement up to 2 dB is observed. The ground layer acts as shield between antenna and lossy Si substrate and improves the radiation characteristics.

On the other hand, defected ground structure (DGS) is extensively used to improve different characteristics of low profile microstrip patch antennas [18,19]. However, in the OCA, there is a major hindrance in incorporating microstrip-like DGS in which the ground plane resides underneath the radiating patch. This is because, the two commonly used patch antenna feed methods - coaxial probe and microstrip line, are not useful for OCAs. Since, the first method needs TSV from the bottom of the substrate and for the second one, available "Sub-Miniature Version A (SMA)" connectors will not fit with the tiny size OCAs. Therefore, coplanar waveguide (CPW) feed is the preferable choice for the OCA. Conversely, OCA with microstrip like DGS having radiating patch in the top and the underneath ground in one intermediate layer of the CMOS layout as shown in Fig.1 may primarily provide several benefits. Firstly, the potentiality of well approved DGS can be engineered to improve OCA characteristics as it is already implemented in low profile microstrip patch antenna [20]. Secondly, the underneath ground metal layer can reduce the substrate losses and enhance the antenna gain simultaneously as investigated in [17]. It is worth to mention here that the OCAs with similar dimensions can offer better radiation characteristics at higher frequency ranges (like mm-wave and submm-wave) as the standard antenna size ($\lambda_0/2$) over these frequencies ranges becomes small and suitable for chip application without any miniaturization. In general, miniaturization reduces the

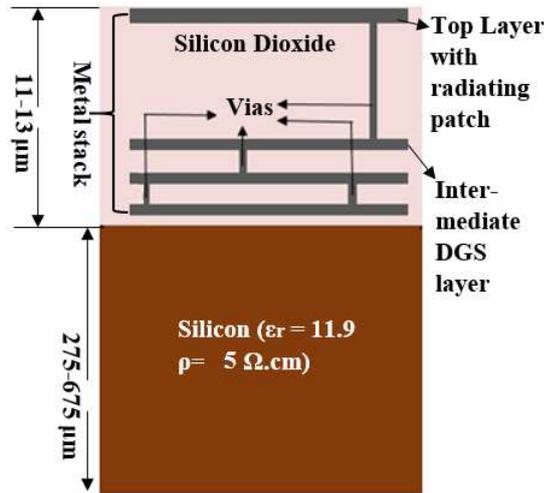


Fig. 1 A layout of standard CMOS technology node

effective antenna aperture and consequently degrades the antenna's radiation characteristics, particularly, gain and efficiency. In this work, a novel method of incorporating DGS in the underneath of CPW-fed antenna is proposed. The incorporation of DGS not only offers dual-band characteristics at the operating frequencies 3.1 GHz and 10.4 GHz, but also improves the antenna gain. The rest of the paper is organized as follows.

The detailed stepwise design and analysis of the proposed dual-band OCA (DB-OCA) is demonstrated in section II. The fabrication process of the proposed antenna is discussed in section III. Along with comparative analysis, the results obtained through the simulation and device characterizations are presented and extensively demonstrated in section IV. Finally, some conclusions are drawn in section V.

2 Design of miniaturized dual band on-chip antenna (DB-OCA)

The stepwise progress to design the proposed DB-OCA is illustrated as follows:

2.1 Design of OCA

In a typical CMOS layout as shown in Fig.1, 9-11 metal layers are sandwiched between the oxidized (or deposited) oxide layers. The electronic circuits corresponding to the various parts of a complete SoC are interconnected with different intermediate metal layer through vias [21]. Here, the top layer is selected as the radiating layer of the proposed antenna. Step wise, the layered and cross-sectional view are presented in Fig. 2 (a-d). A 2 inch Si wafer of thickness 325 μm with low resistivity ($\rho \approx 5\Omega.cm$) is taken as the substrate.

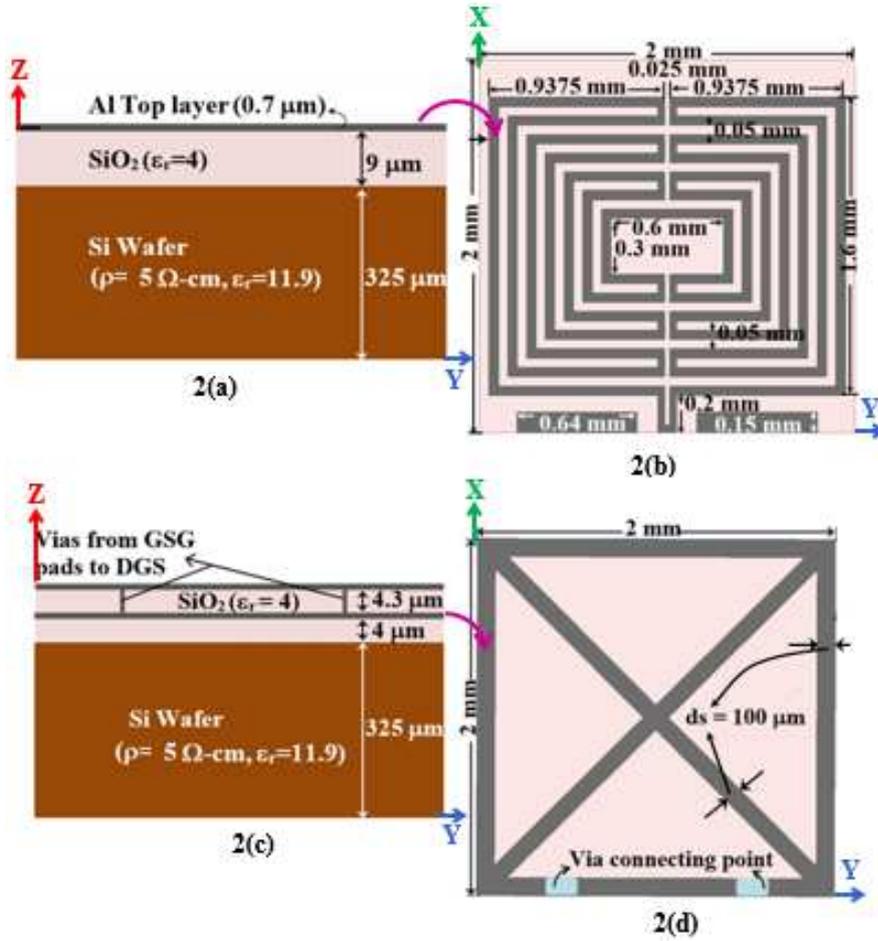


Fig. 2 Structure of proposed antenna; 2(a): Layered view of OCA, 2(b): Top view of OCA, 2(c): Layered view of DB-OCA with DGS layer, 2(d): Top view of DGS layer

Then, a $9 \mu\text{m}$ thick SiO_2 layer is deposited over Si wafer as shown in the layered view in Fig. 2(a). In the top metal layer, a meandered loop antenna as shown in Fig. 2 (b) is designed by using aluminum metal (Al) of thickness $0.7 \mu\text{m}$. The S_{11} characteristics as depicted in Fig. 3 shows a 10 dB operating frequency band from 2.25 GHz to 11.75 GHz. From the Fig. 3 and the gain characteristics in Fig. 4, it can be observed that, though the meandered structure of the loop provides larger electrical length for the current path and hence, better miniaturization in antenna size, however, the maximum achievable gain is quite low.

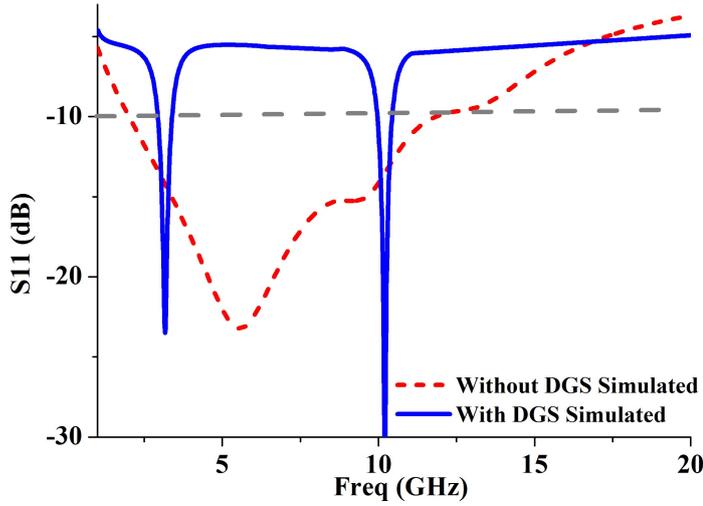


Fig. 3 Return loss plot of proposed antenna with and without DGS

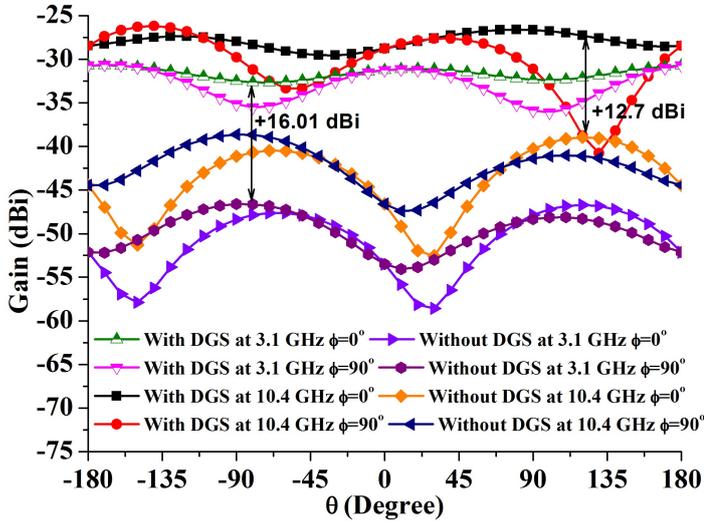


Fig. 4 Gain of proposed antenna with and without DGS at both 3.1 GHz and 10.4 GHz

2.2 Design of DB-OCA

In order to exploit the potentiality of the underneath DGS, a metal layer is sandwiched within the SiO_2 layer as shown in Fig. 2 (c). In CMOS design layout, this becomes an intermediate metal layer. Now, two vias from the two grounds of CPW feed line are connected to the already created two metal pads on it. Hence, the CPW ground is extended to the underneath metal layer of the antenna. Since, DGS embedded in the metallic ground plane can be em-

ployed to realize bandstop characteristics [18,22]. Inspired from it, to obtain dual-band characteristics by introducing a stop-band in the operating band of the designed antenna, a DGS with two mutually orthogonal bow-tie shaped slots are adopted in the intermediate ground plane as shown in Fig. 2 (d). The final dimensions of the DGS are obtained through parametric study. From the S_{11} characteristics as shown in Fig.3, it can be observed that the frequency-selective property of the DGS [18,22,23] provides a stopband characteristic within the antenna operating band, and the resultant structure offers a dual-band property with resonating frequencies 3.1 GHz and 10.4 GHz. At two principle planes – $\phi = 0^\circ$ and $\phi = 90^\circ$, the gain characteristics of the antenna with and without DGS are plotted in Fig. 4. It is observed that, before the introduction of the DGS, the gain of the antenna at the two resonance frequencies was -46.6 dBi and -38.6 dBi, while after incorporation of the Crossed Bowtie-DGS (CB-DGS), the gain is significantly enhanced by +16.01 dB and +12.7 dB and becomes -30.6 dBi and -25.9 dBi respectively. The antenna with achieved gain is suitable for the short and ultra short range communication like inter-chip, intra-chip [24], RFIDs[25], clock distribution[26], wireless sensors [27], and many other integrated microsystems [28,29].

2.3 Parametric analysis

The strip width of the CB-DGS and thickness of the SiO_2 layer are parametrically optimized and the change in antenna characteristics with their variations are presented as follows.

2.3.1 DGS strip width

The change in S_{11} characteristics of the antenna by varying the strip width, “ d_s ” of the CB-DGS from 75 μm to 150 μm are presented in Fig. 5. The figure shows that with increasing the strip width, stopband width is reduced as the lower resonance frequency is shifted towards the higher frequency whereas the higher resonance frequency almost remains unchanged. In general, the stopband filter is the combination of minimum one low pass and one high pass filter with former cutoff frequency lower than the latter. The cut-off frequency of the low-pass and high-pass filters depends on the equivalent shunt capacitance and inductance of the DGS, respectively. With increasing “ d_s ”, the net conducting surface area of the CB-DGS is increased. Due to the intermediary position, the increased surface area of CB-DGS increases the isolation between the top-layer antenna and the substrate in the bottom. This leads to decrease the substrate capacitance effectively prevailed in the antenna while the equivalent inductance remains unchanged as it primarily depends on the number of turns and length of the current path. Thus, the lower resonance frequency i.e., the lower cut-off frequency of the band-stop characteristics introduced by the CB-DGS shifts towards right side and the higher resonance frequency remains at the same value. The variation of “ d_s ” affects the isolation between

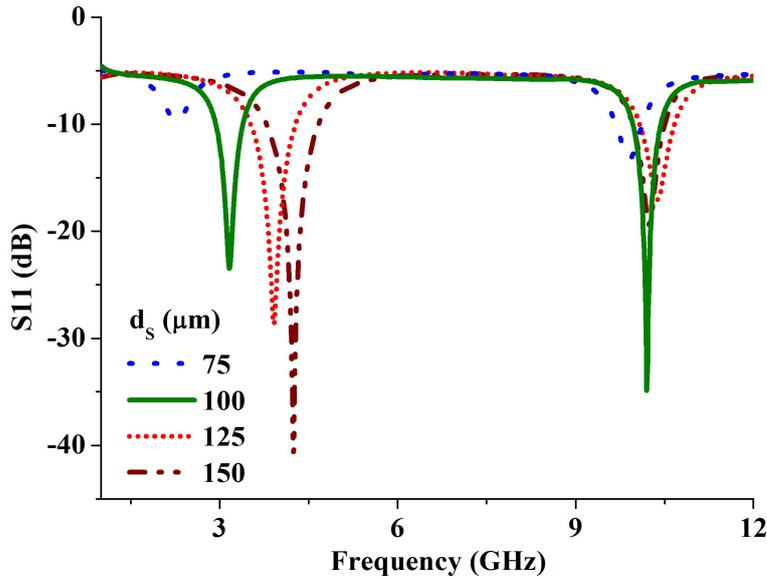


Fig. 5 Variation in return loss with “ d_s ”

the antenna and the substrate as with increasing the strip width, the isolation between the antenna and the substrate is increased. This isolation affects the lower cut-off frequency only and subsequently reduces the bandwidth of the stopband as shown in Fig. 5. Thus, the parametric analysis shows that, by suitably selecting the DGS strip-width, “ d_s ”, the lower resonance frequency can be tuned properly as per the requirement.

2.3.2 SiO_2 thickness

The effect of varying the thickness of SiO_2 between the top and DGS layer is depicted in Fig. 6. The figure shows that with increasing oxide thickness, along with the stop band, both resonance frequencies are shifted towards the right side. For different values of oxide thickness, obtained lower and upper resonance frequencies are plotted in Fig. 7. It can be observed that both frequencies are increasing linearly. The parallel variation of the two frequency plots reveals that the stop-band bandwidth remains unchanged. Since with increasing oxide thickness, the equivalent capacitance is decreased. Hence, the overall characteristics move towards the higher frequency.

3 Device Fabrication

The step by step fabrication process of the proposed dual-band meandered loop on-chip antenna is depicted in Fig. 8. Firstly, an RCA (named by Radio Corporation of America) cleaned low resistive n-type 2 inch Si wafer is taken

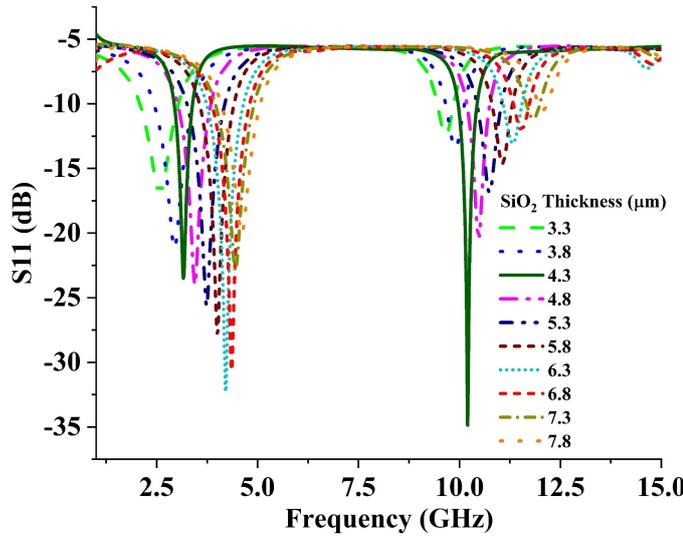


Fig. 6 Variation in return loss with silicon dioxide thickness

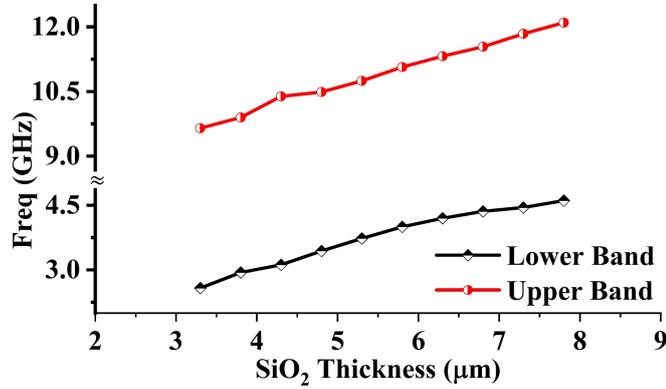


Fig. 7 Variation in resonance of both bands with silicon dioxide thickness

and the same is exposed for SiO₂ deposition of thickness 4.7 μm (Fig. 8(a)) by using plasma-enhanced chemical vapor deposition (PECVD) process at 350°C. Now, to incorporate the DGS in the intermediate layer, the crossed bow-tie shape (as shown in Fig. 2(d)) is engraved by etching the SiO₂ of thickness 0.7 μm (Fig. 8(b-c)). Etching is followed by Al metal deposition and liftoff processes for depositing and removal of extra metal, respectively (Fig. 8(d-e)). After the lift-off process, SiO₂ is deposited again by PECVD of thickness 4.3 μm (Fig. 8(f)). Then for the loop antenna in the top metal layer, Al is deposited by the sputtering process (Fig. 8(g-j)). Finally, the connection between the CPW grounds to the pads in the intermediate DGS layer is made (Fig. 8(k)), and this one is a critical step. Since, deposition of 4.3 μm thick Al is a complex

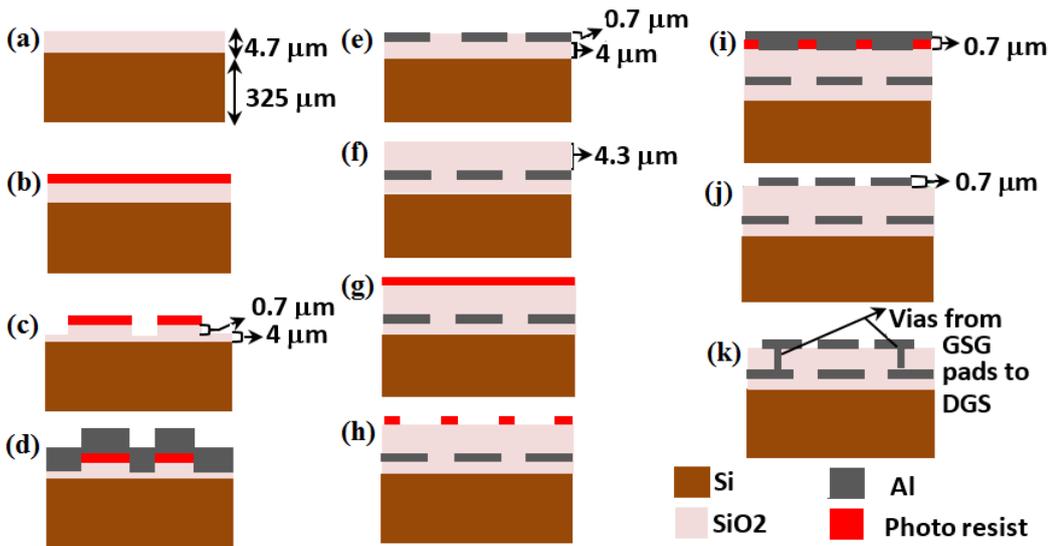


Fig. 8 Process flow of the fabrication of proposed antenna

and time consuming process as it require multiple run of the process. To avoid such complex, time-consuming and costly process, this connection between the CPW ground and pad is made by opening a small portion of the CPW pads and filling it with metallic paste. It is to be mentioned that this opening of the area by chemical etching and filling with the metallic paste is a critical step because of the smaller antenna dimension. However, the step uplifts the electric connection of introduced underneath DGS with top layer ground pads and enables easy feed to the antenna and so to DGS using GSG probe. In all the process steps, the chemicals- AZ4562 and HMDS (hexamethyldisilazane) are used as the photo-resist and developer, respectively.

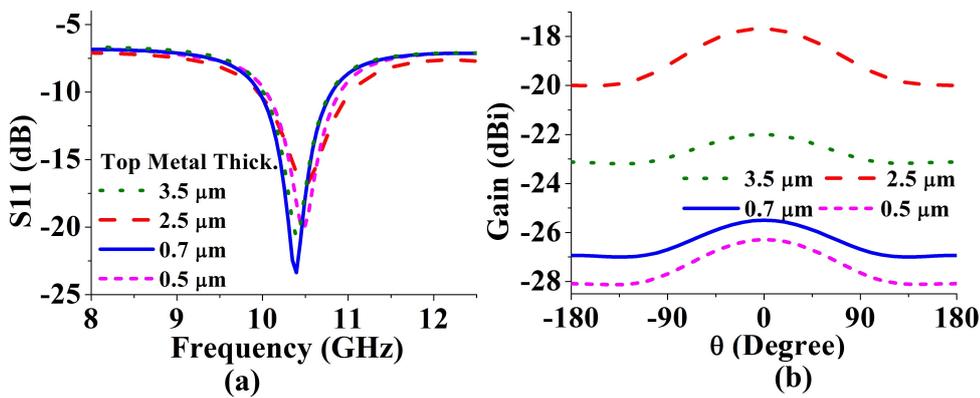


Fig. 9 Variation of top metal layer thickness; (a) S_{11} characteristics; (b) Gain (in dBi).

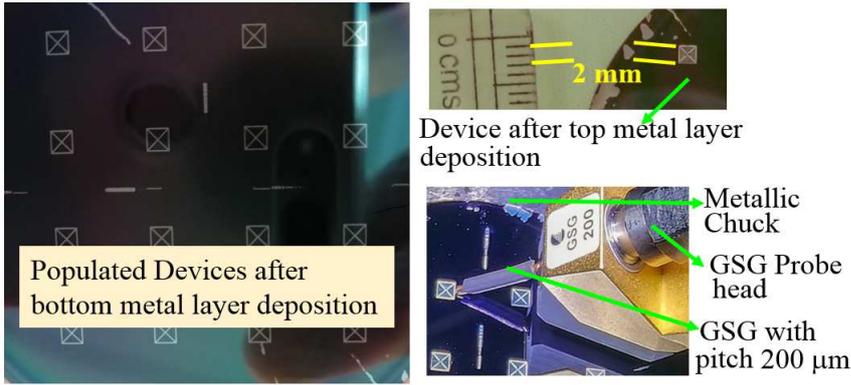


Fig. 10 Fabricated prototype and it's characterization (Picture courtesy: INUP CeNSE, IISc Bangalore)

To observe the effect of top metal thickness on antenna gain, a single band has been chosen for observation. From the S_{11} and gain characteristics of the antenna at 10.4 GHz band as depicted in Fig. 9 (a) and (b) respectively, it can be observed that with increasing the metal (Al) thickness from $0.5\mu\text{m}$ to $3.5\mu\text{m}$, the resonance frequency of the antenna is not affected. Elsewhere, initially with increase in metal thickness, the gain of the antenna is increased and reached to its maximum value of -17.6 dBi at $2.5\mu\text{m}$, and afterwards it starts to decrease. This is because of the skin effect and eddy current losses. At 10.4 GHz, the skin depth of Al is about $0.8\mu\text{m}$. Thus, initially with less thickness, the current flow through the loop is resisted while it is maximum with Al thickness of about $2.5\mu\text{m}$ and then further increase of thickness leads to eddy current loss. For different CMOS process foundries, the allowable maximum limiting values of the deposited metal and oxide layer thicknesses are different. Due to the limitation of the process foundry, the antenna is fabricated with Al thickness of $0.7\mu\text{m}$. Though with such a lower Al thickness, there is no change in the resonance frequency, the gain is compromised by 8.3 dBi. Thus one could expect 8.3 dBi higher antenna gain with Al thickness of about $2.5\mu\text{m}$. The populated devices after deposition of the DGS layer and the complete fabricated prototype with GSG probe are depicted in Fig. 10. The proposed DB-OCA is designed using 180 nm CMOS technology and the antenna is designed using EM stimulation software Ansys HFSSTM 17.0.

4 Results and Discussion

To examine the performance of the fabricated prototype of the proposed DB-OCA, as shown in Fig.10, a CASCADE Summit 11000 AP RF probe station equipped with VNA model R&S ZVA 40 is used. The measured S_{11} characteristics of the prototype is compared with the simulated results in Fig.11. Both the measured and the simulated results are in agreement with the dual band

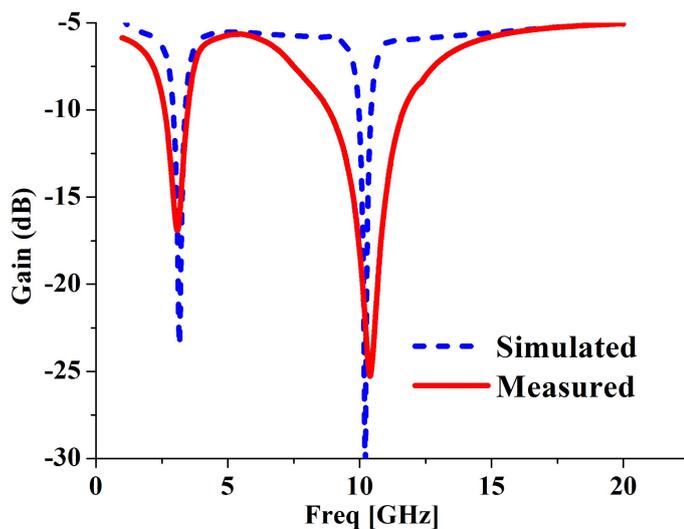


Fig. 11 Return loss comparison as obtained by HFSS and characterization of fabricated prototype

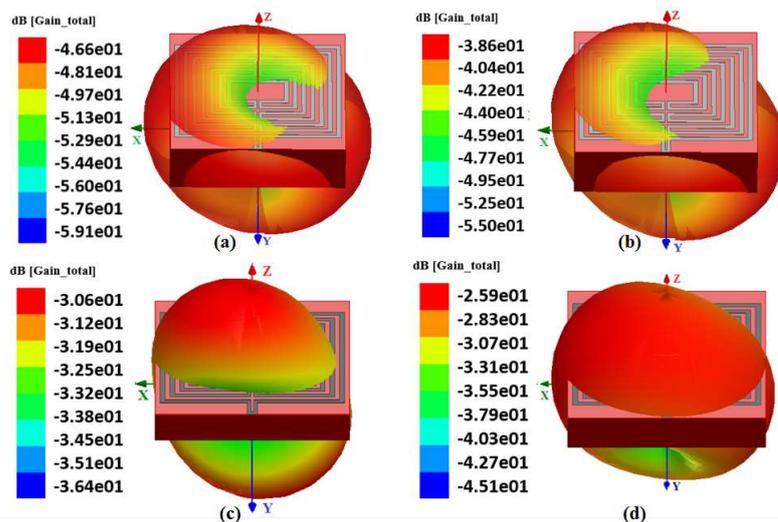


Fig. 12 3-D Gain based radiation patterns of OCA ; (a) without DGS at 3.1 GHz ; (b) without DGS at 10.4 GHz; (c) with DGS at 3.1 GHz ; (d) with DGS at 10.4 GHz

characteristics having resonance frequencies at 3.1 GHz and 10.4 GHz. However, the measured operating band at 10.4 GHz shows a comparatively larger bandwidth than the simulated one. This is primarily because of the metallic chuck is just bottom to the antenna under test(AUT) as shown in Fig. 10. The AUT along with chuck forms a parallel plate structure and generates sub-

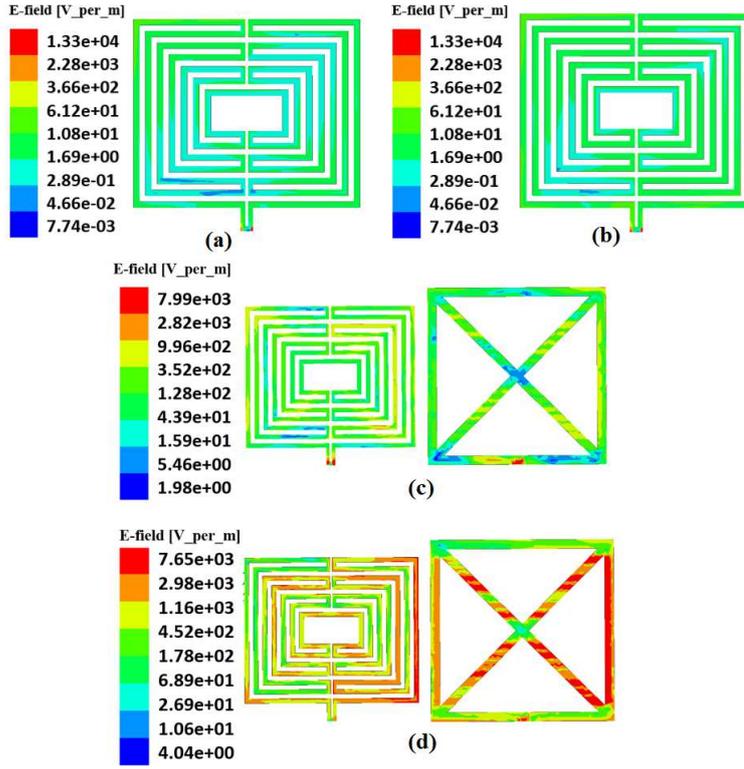


Fig. 13 Electric Field Distribution over OCA ; (a) without DGS at 3.1 GHz ; (b) without DGS at 10.4 GHz; (c) with DGS at 3.1 GHz ; (d) with DGS at 10.4 GHz

Table 1 Comparison of Proposed Antenna with Previous Works for On-chip Communication in SoC Applications

Ref.	f_r	Dim. $_{max}$	Min.	ρ	G	Technology
[30]	160	6	$\lambda_0/0.31$	10	+5	0.18 μ m CMOS
[31]	5.8	6	$\lambda_0/8.5$	20	-40	0.13 μ m CMOS
[32]	12	1	$\lambda_0/25$	10	-46	CMOS
[33]	24	2	$\lambda_0/6.25$	20	-50	CMOS
[34]	57,59	1.25	$\lambda_0/0.4$	NM	1.5,1	GaAs
[35]	60	0.45	$\lambda_0/11$	5	-20	CMOS
This work	3.1, 10.4	2	$\lambda_0/48.3$, $\lambda_0/14.5$	5	-30.6, -25.9	CMOS

f_r = Resonance freq.(GHz), Dim. $_{max}$ = Maximum Dimension (mm), Min.= Miniaturization, ρ = Resistivity (Ω .cm), G= Gain (dB), NM = Not Mentioned.

strate waves which leads to create undesirable results [21]. Also, performance of the OCAs are sensitive to fabrication errors and the possible discrepancies

in the forms of fabrication and material properties are another reason for the variation in the measured and simulated results. At two resonance frequencies, the simulated 3-D radiation patterns of the antenna with and without DGS are shown in Fig. 12 (a-d). It can be seen that, because of the smaller loop dimension (less than $\lambda_0/10$), the far-field patterns in Fig. 12 (a) and (b) are tilted towards the loop plane [36]. Also, without DGS, the direct coupling of the radiation with lossy Si substrate, and the back radiation degrade the antenna gain significantly and are obtained as -46.6 dBi and -38.6 dBi at 3.1 and 10.4 GHz respectively. However, by introducing the intermediate DGS layer, both substrate coupling and back radiation are reduced, and the corresponding improvement in the front radiation characteristics can be clearly spotted in Fig. 12 (c) and (d). Unlike the conventional microstrip patch antennas where the underneath DGS layer reduces the radiation gain due to back radiation [37], the introduced DGS layer serves as a reflector in OCA to prevent direct coupling of the radiated EM waves with Si, and reduces the substrate loss and back radiation significantly. Thus, an improvement in the antenna gain is realized at both the resonance frequencies. Usually, incorporation of the DGS affects the overall field distributions of the antenna by adding an equivalent capacitance and inductance of the DGS [38]. Thus, with DGS, an effectively increased current path moves the radiation maximum towards the broadside direction [36]. The electric field distributions of the OCA with and without DGS layer are presented in Fig. 13. A comparatively increased E-field intensity within the loop in presence of the DGS ensures the affects of DGS as a reflector. Thus, an enhancement in the radiation gain of the antenna by +16.01 dBi and +12.7 dBi at 3.1 GHz and 10.4 GHz are obtained, respectively.

The performance of the proposed antenna is compared with the related published works in Table 1 . The table summarizes that the radiation performance of the antenna is primarily depended upon the size as well as the characteristics of the used substrates. For the higher frequencies, necessity of the miniaturization is not essential as good antenna gain is obtained with dimension higher than the half-wavelength [30,31]. However, with miniaturization, the gain is compromised [32,33,34,35]. The other method to improve the performance is to implement the antenna on high resistive substrates like GaAs, SiGe. However, as mentioned early, these substrate are expensive and uncommon to the IC industries. The proposed method based on underneath DGS provides dual-band at 3.1 GHz and 10.4 GHz with miniaturized dimensions of $(\lambda_0/48.3)$ and $(\lambda_0/14.5)$. Moreover, the designed antenna on a low resistive ($5 \Omega.cm$) wafer supporting CMOS compatible technology offers significantly gain. Employing the proposed method, one can expect further improvement in the gain characteristics at higher frequencies as in [30,34,35]. This exhibits the effectiveness of the proposed approach to design OCA with improved radiation characteristics.

5 Conclusion

A dual-band meandered loop OCA has been successfully designed on a low resistive Si wafer for the resonance frequency of 3.1 GHz and 10.4 GHz bands. The proposed antenna with the introduced DGS underneath the radiating patch not only provides dual-band characteristics, but it also offers a significantly improved gain. Comparison of the antenna performance with the state-of-the-art literature reported brings out that the proposed method is a possible solution for the major challenge to realize OCA with improved gain by reducing substrate loss.

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Ethical Approval

Ethics approval was not required for this systematic study.

Consent to Participate

Informed consent was not required for this systematic study.

Consent to Publish

Authors give their consent for the publication of identifiable details, which can include photograph(s), data and other details within the text (“Material”) to be published in the Journal of Infrared, Millimeter, and Terahertz Waves.

Authors Contributions

HS has done the research work reported in the article. SKM has provided his supervision and reviewed the work. Both the authors read and approved the final manuscript.

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Competing Interests

Authors declare that they have no competing interests as defined by Springer, or other interests that might be perceived to influence the results and/or discussion reported in this paper.

Availability of Data and Material

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

References

1. Taiwan semiconductor manufacturing company (TSMC) annual report 2020 (1) (2020). 2021.
2. I. Chen, H. Chiou, and N. Chen. V-band on-chip dipole-based antenna. *IEEE Transactions on Antennas and Propagation*, 57(10):2853–2861, 2009.
3. Bal S. Alibakhshikenari, Mohammad andVirdee, Chan H. See, Pancham Shukla, Shahram Salekzamankhani, Raed A. Abd-Alhameed, Francisco Falcone, and Ernesto Limiti. Study on improvement of the performance parameters of a novel 0.41 - 0.47 THz on-chip antenna based on metasurface concept realized on 50 μm GaAs-layer. *Scientific Reports*, 10(1):11034, Jul 2020.
4. Mohammad Alibakhshikenari, Bal S Virdee, Chan H See, Pancham Shukla, Shahram Salekzamankhani, Raed A Abd-Alhameed, Francisco Falcone, and Ernesto Limiti. Study on improvement of the performance parameters of a novel 0.41–0.47 thz on-chip antenna based on metasurface concept realized on 50 μm gaas-layer. *Scientific Reports*, 10(1):1–9, 2020.
5. Wasif Tanveer Khan, A Çağrı Ulusoy, Gaetan Dufour, Mehmet Kaynak, Bernd Tillack, John D Cressler, and John Papapolymerou. A D-band micromachined end-fire antenna in 130-nm SiGe BiCMOS technology. *IEEE Transactions on Antennas and Propagation*, 63(6):2449–2459, 2015.
6. Benedikt Sievert, Jan Taro Svejda, Jonathan Wittemeier, Nils Pohl, Daniel Erni, and Andreas Rennings. Equivalent circuit model separating dissipative and radiative losses for the systematic design of efficient microstrip-based on-chip antennas. *IEEE Transactions on Microwave Theory and Techniques*, 69(2):1282–1294, 2021.
7. Mohammad Alibakhshikenari, Bal S Virdee, Chan H See, Raed A Abd-Alhameed, Francisco Falcone, and Ernesto Limiti. High-gain metasurface in polyimide on-chip antenna based on crlh-tl for sub-terahertz integrated circuits. *Scientific reports*, 10(1):1–9, 2020.
8. R. Pilard, F. Gianesello, D. Gloria, D. Titz, F. Ferrero, and C. Luxey. 60 GHz HR SOI CMOS antenna for a system-on-chip integration scheme targeting high data-rate kiosk applications. In *2011 IEEE International Symposium on Antennas and Propagation (APSURSI)*, pages 895–898, 2011.
9. J. A. Zevallos Luna, L. Dussopt, and A. Siligaris. Hybrid on-chip/in-package integrated antennas for millimeter-wave short-range communications. *IEEE Transactions on Antennas and Propagation*, 61(11):5377–5384, Nov 2013.
10. B. B. Adela, M. C. van Beurden, P. Van Zeijl, and A. B. Smolders. High-isolation array antenna integration for single-chip millimeter-wave FMCW radar. *IEEE Transactions on Antennas and Propagation*, 66(10):5214–5223, 2018.
11. Cheng Jin, Vasarla Nagendra Sekhar, Xiaoyue Bao, Bangtao Chen, Boyu Zheng, and Rui Li. Antenna-in-package design based on wafer-level packaging with through silicon via technology. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 3(9):1498–1505, 2013.

12. Aydin Babakhani, Xiang Guan, Abbas Komijani, Arun Natarajan, and Ali Hajimiri. A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas. *IEEE Journal of Solid-State Circuits*, 41(12):2795–2806, 2006.
13. Debin Hou, Yong-Zhong Xiong, Wang-Ling Goh, Sanming Hu, Wei Hong, and Mohammad Madhian. 130-GHz on-chip meander slot antennas with stacked dielectric resonators in standard CMOS technology. *IEEE Transactions on Antennas and Propagation*, 60(9):4102–4109, 2012.
14. Mai O Sallam, Mohamed Serry, Sherif Sedky, Atif Shamim, Walter De Raedt, Guy AE Vandebosch, and Ezzeldin A Soliman. Micromachined on-chip dielectric resonator antenna operating at 60 GHz. *IEEE Transactions on Antennas and Propagation*, 63(8):3410–3416, 2015.
15. W. E. McKinzie, D. M. Nair, B. A. Thrasher, M. A. Smith, E. D. Hughes, and J. M. Parisi. 60-GHz 2×2 LTCC patch antenna array with an integrated EBG structure for gain enhancement. *IEEE Antennas and Wireless Propagation Letters*, 15:1522–1525, 2016.
16. H. Kuo, H. Yue, Y. Ou, C. Lin, and H. Chuang. A 60-GHz CMOS sub-harmonic RF receiver with integrated on-chip artificial-magnetic-conductor yagi antenna and balun bandpass filter for very-short-range gigabit communications. *IEEE Transactions on Microwave Theory and Techniques*, 61(4):1681–1691, 2013.
17. Shiji Pan, Francis Caster, Payam Heydari, and Filippo Capolino. A 94-ghz extremely thin metasurface-based bicmos on-chip antenna. *IEEE Transactions on Antennas and Propagation*, 62(9):4439–4451, Sep. 2014.
18. Mukesh Kumar Khandelwal, Binod Kumar Kanaujia, and Sachin Kumar. Defected ground structure: Fundamentals, analysis, and applications in modern wireless trends. *International Journal of Antennas and Propagation*, 2017, 2017.
19. Li Hong Weng, Yu-Chun Guo, Xiao-Wei Shi, and Xiao-Qun Chen. An overview on defected ground structure. *Progress In Electromagnetics Research B*, 7:173–189, 2008.
20. Ashwini K. Arya, M.V. Kartikeyan, and A. Patnaik. Defected ground structure in the perspective of microstrip antennas: A review. *Frequenz*, 64(5-6):79–84, 2010.
21. Hammad M Cheema and Atif Shamim. The last barrier: on-chip antennas. *IEEE Microwave Magazine*, 14(1):79–91, 2013.
22. Santanu Dwari and Subrata Sanyal. Compact wide stopband low-pass filter using rectangular patch compact microstrip resonant cell and defected ground structure. *Microwave and Optical Technology Letters*, 49(4):798–800, 2007.
23. Arjun Kumar and Kartikeyan V Machavaram. Microstrip filter with defected ground structure: a close perspective. *International Journal of Microwave and Wireless Technologies*, 5(5):589–602, 2013.
24. Hristomir Yordanov and Peter Russer. Wireless inter-chip and intra-chip communication. In *2009 European Microwave Conference (EuMC)*, pages 145–148, 2009.
25. Emilie Charlot, Mototsugu Hamada, and Tadahiro Kuroda. An on-chip antenna with an area of 0.9 square millimeters for rfid applications in the 5.8 ghz – 24 ghz range. In *2020 International Symposium on Antennas and Propagation (ISAP)*, pages 41–42, 2021.
26. K.K. O, K. Kim, B. Floyd, J. Mehta, H. Yoon, C.-M. Hung, D. Bravo, T. Dickson, X. Guo, R. Li, N. Trichy, J. Caserta, W. Bomstad, J. Branch, D.-J. Yang, J. Bohorquez, L. Gao, A. Sugavanam, J.-J. Lin, J. Chen, F. Martin, and J. Brewer. Wireless communications using integrated antennas. In *Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)*, pages 111–113, 2003.
27. JP Carmo, PM Mendes, Carlos Couto, and JH Correia. 5.7 ghz on-chip antenna/rf cmos transceiver for wireless sensor networks. *Sensors and Actuators A: Physical*, 132(1):47–51, 2006.
28. PM Mendes, A Polyakov, M Bartek, JN Burghartz, and JH Correia. Integrated chip-size antennas for wireless microsystems: Fabrication and design considerations. *Sensors and Actuators A: Physical*, 125(2):217–222, 2006.
29. K.K. O, Kihong Kim, B.A. Floyd, J.L. Mehta, Hyun Yoon, Chih-Ming Hung, D. Bravo, T.O. Dickson, Xiaoling Guo, Ran Li, N. Trichy, J. Caserta, W.R. Bomstad, J. Branch, Dong-Jun Yang, J. Bohorquez, E. Seok, Li Gao, A. Sugavanam, J.-J. Lin, Jie Chen, and J.E. Brewer. On-chip antennas in silicon ics and their application. *IEEE Transactions on Electron Devices*, 52(7):1312–1323, 2005.

30. Junqiang Wu, Avinash Karanth Kodi, Savas Kaya, Ahmed Louri, and Hao Xin. Monopoles loaded with 3-D-printed dielectrics for future wireless intrachip communications. *IEEE Transactions on Antennas and Propagation*, 65(12):6838–6846, 2017.
31. Wen-Chung Liu. A coplanar waveguide-fed folded-slot monopole antenna for 5.8 GHz radio frequency identification application. *Microwave and optical technology letters*, 49(1):71–74, 2007.
32. Ding Yi, Lu Chong, He Xiao-wei, and Tan Hong-zhou. 12 GHz wireless clock delivery using on-chip antennas: A case for future intra/inter-chip wireless interconnect. In *2012 IEEE International Conference on Computer Science and Automation Engineering (CSAE)*, volume 1, pages 212–215. IEEE, 2012.
33. Kihong Kim and K Ko. Integrated dipole antennas on silicon substrates for intra-chip communication. In *IEEE Antennas and Propagation Society International Symposium. 1999 Digest. Held in conjunction with: USNC/URSI National Radio Science Meeting (Cat. No. 99CH37010)*, volume 3, pages 1582–1585. IEEE, 1999.
34. Jau-Jr Lin, Hsin-Ta Wu, Yu Su, Li Gao, Aravind Sugavanam, Joe E Brewer, et al. Communication using antennas fabricated in silicon integrated circuits. *IEEE Journal of solid-state circuits*, 42(8):1678–1687, 2007.
35. G Passiopoulos, S Nam, A Georgiou, AE Ashtiani, ID Robertson, and EA Grindrod. V-band single chip, direct carrier BPSK modulation transmitter with integrated patch antenna. In *1998 IEEE MTT-S International Microwave Symposium Digest (Cat. No. 98CH36192)*, volume 1, pages 305–308. IEEE, 1998.
36. J.D. Kraus. *Antennas*. Electrical engineering series. McGraw-Hill, 1988.
37. Yani Wang, Chaozong Guo, Jiao Yin, Huiqing Zhai, and Wuning Zhong. High isolation high front-to-back ratio antenna based on slotted siw. In *2021 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, pages 1–3, 2021.
38. Kin-Lu Wong. *Compact and broadband microstrip antennas*, volume 168. John Wiley & Sons, 2004.