Rail-to-Rail Input/Output Bulk Driven Class AB Operational Amplifier with Improved Composite Transistors (Invited paper)

Luis Henrique Rodovalho (luishenriquerodovalho@gmail.com)
Cesar Rodrigues
Federal Univ. of Santa Catarina
Orazio Aiello
University of Genova

Research Article

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Rail-to-Rail Input/Output Bulk Driven Class AB Operational Amplifier with Improved Composite Transistors *(Invited paper)*

Luis Henrique Rodovalho, Cesar Ramos Rodrigues[1] and Orazio Aiello[2]

[1*]Biomedical Engineering Institute, Federal Univ. of Santa Catarina, Department, Florianopolis, Santa Catarina, Brazil.
[2]Department of Electronics, University of Genova, via alla Opera Pia 11a, Genova, 16100, Italy.

*Corresponding author(s). E-mail(s): luishenriquerodovalho@gmail.com;
Contributing authors: cesar@ieee.com; orazio.aiello@ieee.org;

Abstract

This work presents two-stage single-ended Operational Transconductance Amplifiers (OTA) with very high voltage gain and rail-to-rail output voltage excursion. This is achieved by using Improved Composite Transistors (ICT) with safe forward-body-biasing, so the amplifier can be used with typical I/O supply voltages and high-VT thick-oxide transistors without significant parasitic substrate current. Two versions of the same OTA were designed and simulated using the open-source Skywater 130 nm PDK. The first version, made of only Trapezoidal Transistor Arrays (TTA), achieves an 83 dB voltage gain, 13.1 MHz GBW, and 60° phase margin for a 10 pF capacitive load while demanding 122.1 µW of power at 3.0 V power supply. The proposed ICT OTA version attains about the same specifications, except for its voltage gain, which has increased by 37 dB, thus reaching 121 dB.

Keywords: current mirror, operational amplifier, composite transistors,forward-body-biasing

1 Introduction

The operational amplifier is one of the most basic building blocks of analog circuits, and it is used in several applications, including signal amplification and filtering [1]. An ideal operational amplifier has infinite voltage gain and input/output voltage excursion. However, its real-world counterpart voltage gain is finite, limiting its maximum feasible amplification, while its voltage excursion is limited by the supply rails and transistor saturation voltages [2]. The voltage gain can be improved by using single-stage amplifiers with cascode output [3], or multiple cascaded gain stages [4], but this technique requires complex phase margin stability compensation circuits for proper operation with negative feedback for more than two cascaded stages.

A high-gain amplifier was proposed in [5] which uses the self-cascode transistor configuration [6], also known as composite transistors or trapezoidal arrays, which is an alternative to cascode gain stages. The composite transistor can be further improved [7–10] by using independent forward-body-biasing to reduce the transistors'

active area. Two-stage Miller operational amplifiers with improved composite transistors [11, 12] were proposed, but use external biasing voltage sources for forward-body-biasing. Those amplifier topologies can be self-biased by using the augmented technique Dynamic Threshold-Voltage MOSFET (DTMOS) [13, 14], as proposed in [15].

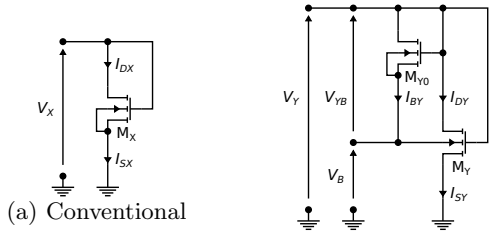
However, the above-mentioned Miller amplifiers have a class A common-source output stage, and are highly power inefficient while driving low resistance or high capacitance loads [16]. Also, their common-mode input range is limited by the input differential pair. The solution is to use a class AB output-stage, such as the one proposed in [17], to drive those kind of loads, and bulk-driven differential pair [18] to increase the common-mode input range without using complex biasing circuits used for input rail-to-rail operation.

This work presents two versions of a rail-to-rail input and output class AB operational amplifier [17], with bulk-driven input [18], by using either composite transistors [5, 6] or improved composite transistors [7, 12]. In sections 2 and 3 the safe forward-body-biasing technique [14] and how it can be used to improve the current mirror circuit design with ICT [7] are respectively discussed. Section 4 discusses how to use these techniques to improve the voltage gain of the proposed operational amplifier. Section 5 presents simulation results for both amplifiers designs, and, finally, Section 6 summarizes this work with conclusions.

2 Safe Forward-Body-Biasing

Figure 1a shows a MOSFET in the conventional diode configuration with short circuited gate and drain terminals ($V_G = V_D = V_X$) and short circuited bulk and source terminals ($V_B = V_D = 0$). Figure 1b shows a variation of DTMOS diode configuration [13], the augmented DTMOS [14]. In this configuration, the transistor M_Y bulk terminal is connected indirectly to its gate terminal by using the transistor M_{Y0} to limit the parasitic bulk current I_{BY}. This way, for normal circuit operation, $V_B \leq V_G$.

However, as the bulk-source voltage V_{BS} is still positive, the diode formed by the pn junction between the p-substrate and n-doped source will be forward biased and there will be a non-negligible current I_B flowing from the bulk to the source terminal. Considering that the MOSFET



(a) Conventional (b) DTMOS

Fig. 1: Transistor diode configurations

is also biased in weak inversion, accordingly to the UICM model [2], the drain current I_D can be approximated to

$$I_D \approx 2e^1 I_S \exp\left(\frac{V_{GS} + (n-1)V_{BS} - V_T}{n\phi_t}\right) \quad (1a)$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SQ} \frac{W}{L} \quad (1b)$$

where I_S is the normalization current, which is a function of the charge mobility μ, the oxide capacitance per area C'_{ox}, the slope factor n, the thermal voltage ϕ_t and the channel width and length W and L.

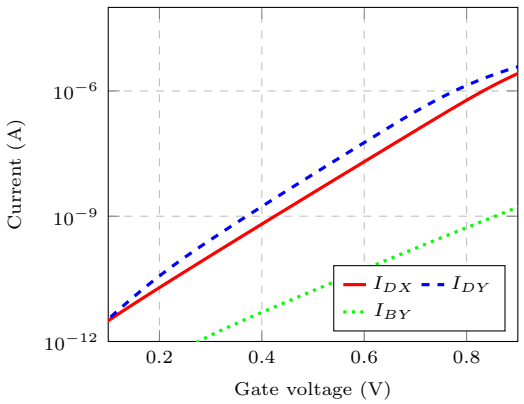
The parasitic bulk terminal current I_B can be approximated to

$$I_B \approx I_{Sdio} \exp\left(\frac{V_{BS}}{n_{dio}\phi_t}\right) \quad (2)$$

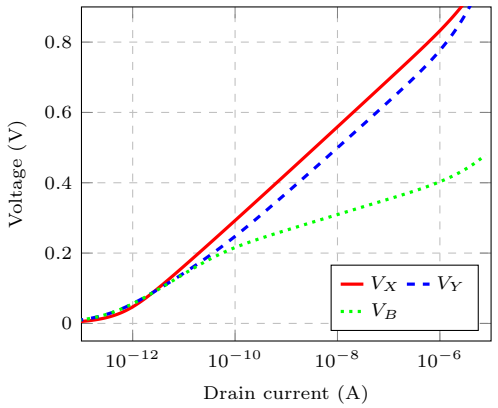
where I_{Sdio} is the scale current and n_{dio} is the ideality factor, accordingly to the Shockley diode equation [19].

Figures 2b and 2a shows the voltage-current curves for the diode configurations shown in Figures 1a and 1b. The transistors are high V_T ($\approx$ 860 mV) thick oxide devices with their respective channel width and length are 1.0 µm and 0.5 µm. First of all, it can be noticed that, while operating in weak inversion, M_Y drain current I_{DY} is much larger than the bulk current I_{BY}, which increased exponentially with V_Y, as expected. The source current I_{SY}, which is the sum of I_{DY} and I_{BY}, is approximately I_{DY} while $I_{DY} \gg I_{BY}$.

For $V_Y > 0.2$ V, there is a significant V_{YB} voltage drop due to negative feedback, as I_B increases. For $V_Y < 0.3$ V, the transistor M_Y I_D is just few tens of pA, while $V_Y \approx V_B$. For V_Y below this biasing point, the protection transistor M_{Y0} is not



(a) Current × Voltage



(b) Voltage × Current

Fig. 2: Transistor in diode configuration DC transfer functions

needed at all. It is worth noticing that transistors with lower V_T may use the conventional DTMOS technique without any forward-body-biasing protection for higher V_{BS} and I_D.

Also, it can be noticed that, for the same drain current ($I_{DX} = I_{DY}$), the transistor M_X gate voltage V_X is greater than transistor M_Y gate voltage V_Y. If $I_{DX} = I_{DY}$, considering (1), it can be inferred that

$$V_X \approx V_Y + (n-1)V_B = V_Y + \Delta V_T \qquad (3)$$

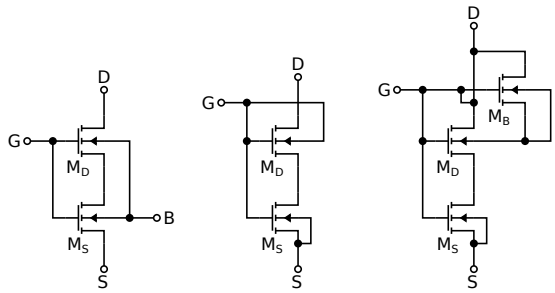
where ΔV_T is also an approximation for the threshold voltage body-effect [20]. This threshold voltage reduction resulting from forwarding body-biasing is a known analog circuit supply voltage reduction technique [21], and it is especially useful for current mirrors, as it will be discussed in the next section.

3 Improved Current Mirror

The desired ideal current mirror has a constant current gain independent of its operation conditions, such as temperature and output voltage. A practical current mirror behavior must be as close as possible to the ideal, and it can use several analog circuit design techniques to achieve that.

Figure 3a shows the Composite Transistor (CT) configuration [6, 22], also know as self-cascode or Trapezoidal Transistor Array (TTA). It is composed by two transistors M_D and M_S of different channel widths and length, or, alternatively, transistor arrays of different dimensions. Figure 3b shows the Improved Composite Transistor (ICT), where M_D is forward-body-biased using the DTMOS technique [13].

As explained before, there is a non-negligible parasitic substrate current as a result of forward-body-biasing, which flows from the gate input if it is directly connected to the bulk terminal. So, the transistor bulk terminal should be connected to another high-potential source, such as the supply voltage, either directly [8] or indirectly [10], but this limits the circuit's maximum supply voltage. One possible solution is to use the augmented DTMOS technique [14], as shown in Figure 3c, so forward-body-biasing is still defined by the gate input voltage.



(a) (b) (c)

Fig. 3: Conventional and improved composite transistor: (a) conventional Composite Transistor (CT) [6], (b) Improved Composite Transistor (ICT) [9] with DTMOS [13], and (c) improved with augmented DTMOS [14]

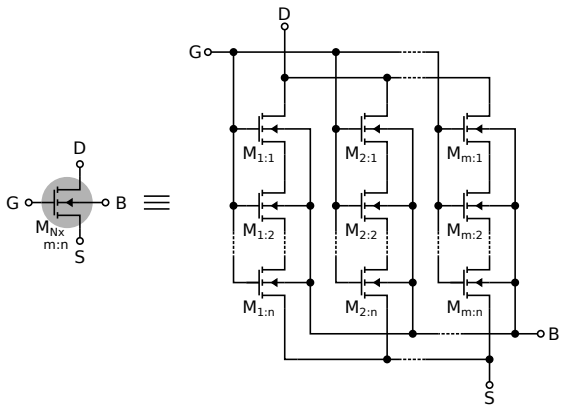


Fig. 4: A $1 \times (m : n)$ rectangular transistor array

Rectangular Transistor Arrays (RTA), such as the one shown in Fig. 4, can be modeled as a single transistor [6] with a higher output impedance. The rectangular array is a m by n matrix of single transistors composed of m parallel columns of n series single transistors.

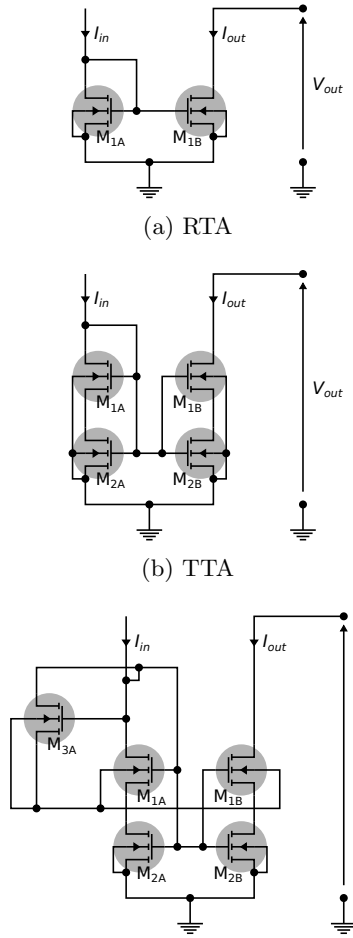
By using rectangular, trapezoidal and improved composite transistors, the basic CMOS current mirror can be designed in several ways, as shown in Figure 5. Their dimensions are shown in Table 1 and their simulation results are shown in Figures 6a and 6b.

Table 1: Current mirror transistor array dimensions

		k × $(m : n)$ -	W/L (µm)
RTA	$M_{1A\text{-}B}$	2 × (1:16)	1.0/0.5
TTA	$M_{1A\text{-}B}$	2 × (4:2)	1.0/0.5
	$M_{2A\text{-}C}$	2 × (1:8)	1.0/0.5
ICT	$M_{1A\text{-}B}$	2 × (4:2)	1.0/0.5
	$M_{2A\text{-}B}$	2 × (1:8)	1.0/0.5
	M_{3A}	2 × (4:2)	1.0/0.5

Fig. 5a shows the RTA current mirror. Transistor arrays M_A and M_B are made of the same single transistor and can be made of arbitrary dimensions for any fractional current gain [23]. This is the most efficient way to design non-unity gain current mirrors. However, this simple current mirror has a relatively low tolerance to output voltage variation due to its low output resistance.

The solution to improve current mirror output resistance is to use cascode current mirrors



(a) RTA

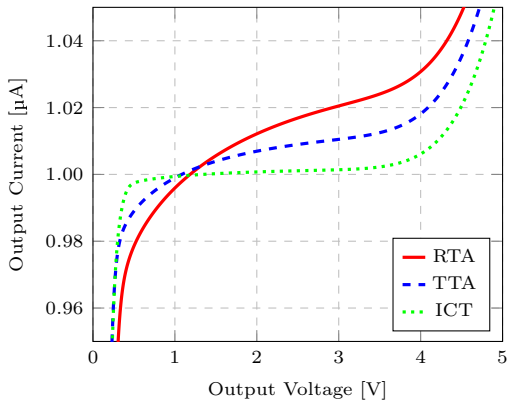
(b) TTA

(c) ICT

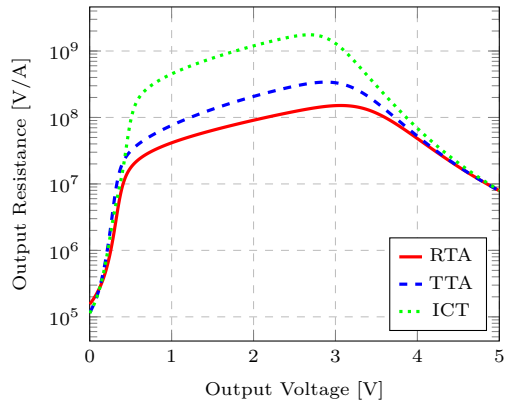
Fig. 5: Current mirrors

and their high-swing versions [24]. Fig. 5b shows the TTA self-biased current mirror [25], where $M_{1A\text{-}B}$ are parallel transistor arrays and $M_{2A\text{-}B}$ are series transistor arrays. The ICT current mirror [7], shown in Fig. 5c, is a variation of the TTA mirror with the addition of protection transistor M_{3A}, which forward-body-bias transistors $M_{1A\text{-}B}$, while $M_{2A\text{-}B}$ bulk terminals are connected to ground.

Figure 6a shows the current mirrors output current I_{out} as function of the output voltage V_{out} for a input current $I_{in} = 100$ nA, while 6b shows their respective output resistance $R_{out} = 1/I'_{out}$. As expected, the TTA version is a slight improvement of the RTA one, while the ICT version is



(a)



(b)

Fig. 6: Current mirror simulations results for $I_{in} = 100$ nA: (a) output current × ouput voltage, and (b) output resistance × output voltage

even better than the TTA one. All versions have deteriorated performance as the V_{out} is increased after some point due to Substrate Current induced Body Effect (SBCE) [26], but, still, the ICT current mirror is orders of magnitude better than the other ones.

It is worth noticing that the ICT current mirror has a high output resistance, but this performance is decreased for lower input currents I_{in} and for transistors with lower slope factor n, as forward-body-biasing is less effective. Additionally, isolated transistors require triple well process technologies, and isolated transistor wells must be placed further apart to obey design rules, so it can use more area than similar TTA current mirrors despite having the same transistor active area. Additionally, the TTA current mirror can be further improved by using even more parallel transistors in the $M_{1A\text{-}B}$ transistor arrays, but non-unity gains using this technique is extremely inefficient, contrastingly to the RTA version.

4 Proposed Operational Amplifier

The previously discussed techniques, used to improve the current mirror, are extremely useful for voltage amplifier design, as its gain is a function of the transistors output resistance. The circuit shown in Figure 7 combines three techniques: the bulk driven folded self-cascode stage [18], the compact class AB output stage [17], and trapezoidal transistor arrays [6].

The input differential pair, composed of transistors $M_{0A,B}$, have their gate terminals connected to the lowest available potential, preferably to a tie-low circuit, to avoid antenna effects (plasma-induced gate oxide damage). Meanwhile, their bulk terminals are connected to the amplifier inputs [16]. Their source terminals are shorted, as in any conventional differential pair, and their drain terminals are connected to the intermediate node between transistors $M_{5,6F}$ and $M_{5,6E}$, as in the conventional folded cascode topology. Nevertheless, those transistors gate terminals share the same connection, forming a self-cascode configuration, as in [18].

The compact class AB output stage [17] is composed by control $M_{6C,D}$, and push-pull transistors $M_{7A,B}$, and $M_{7D,E}$. The control transistors biases the output stage's DC operation point, and changes dynamically for any given load, for both PMOS and NMOS devices. The frequency compensation capacitors C_C are connected to the intermediate nodes to cancel the introduced by using the cascoded-Miller compensation technique. The floating class AB control transistors are biased by M_{1C} and M_{2D}. All the other transistors, including the output stage, are biased by a trapezoidal current mirror [6, 23, 25]. Table 2 summarizes the transistor dimensions.

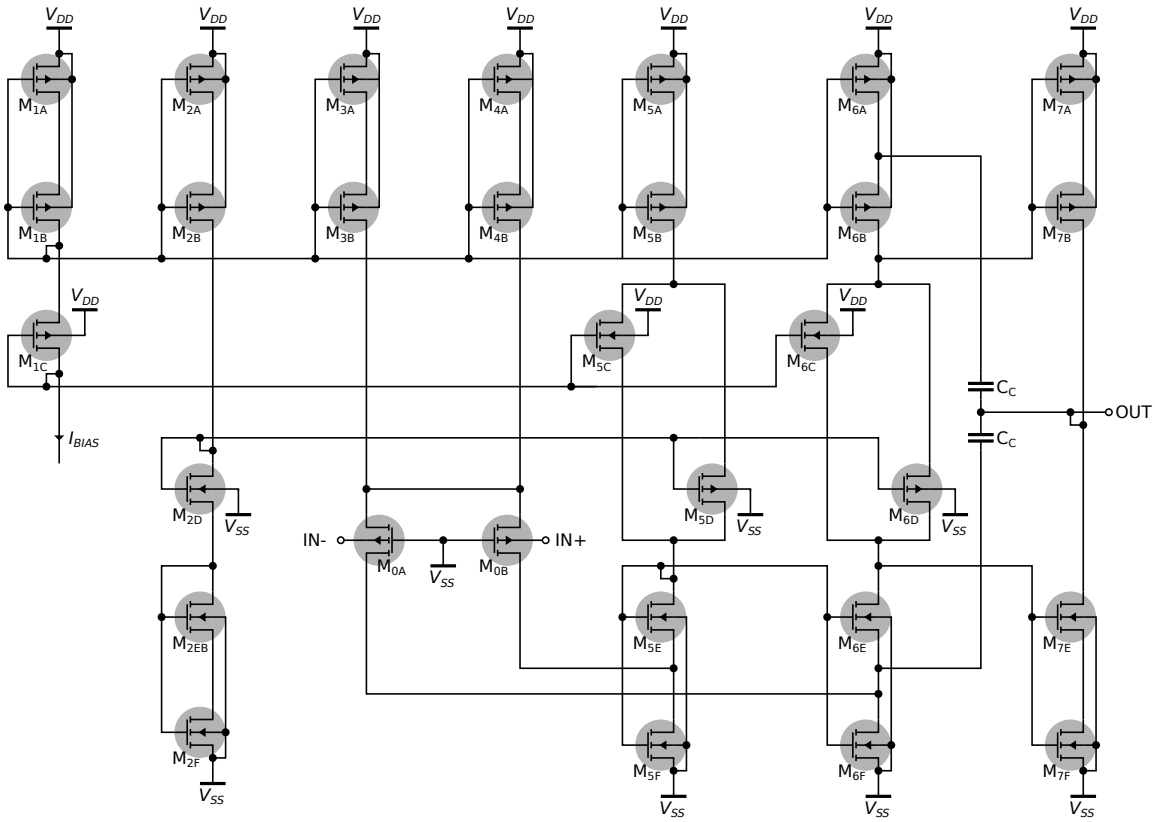


Fig. 7: Proposed bulk-driven rail-to-rail class AB operational amplifier with trapezoidal transistor arrays (TTA)

Table 2: Proposed bulk-driven rail-to-rail class AB operational amplifier transistor dimensions (TTA)

	k × $(m:n)$	W/L (µm/µm)		k × $(m:n)$	W/L (µm/µm)		k × $(m:n)$ -	W/L (µm/µm)
$M_{0A,B}$	4 × (8:1)	2.0/0.5	$M_{1\text{-}6A}$	4 × (2:4)	2.0/0.5	$M_{1\text{-}6B}$	4 × (4:2)	2.0/0.5
$M_{2,5,6E}$	4 × (1:8)	2.0/0.5	$M_{2,5,6F}$	4 × (2:4)	2.0/0.5	M_{1C}	4 × (4:4)	2.0/0.5
$M_{5,6C}$	4 × (2:4)	2.0/0.5	M_{2D}	4 × (2:8)	2.0/0.5	$M_{5,6D}$	4 × (1:8)	2.0/0.5
M_{7A}	4 × (4:2)	2.0/0.5	M_{7B}	4 × (8:1)	2.0/0.5	M_{7E}	4 × (2:4)	2.0/0.5
M_{7F}	4 × (4:2)	2.0/0.5						

As explained in the last section, the trapezoidal transistor array (TTA) based current mirror outputs a greater resistance as a function of the output voltage than the Rectangular Transistor Array. Yet it can be further increased by using the Improved Composite Transistor (ICT) technique, as shown in Figure 8. In this amplifier version, the bulk terminals of the PMOS transistors $M_{1\text{-}7B}$ are indirectly connected to the gate terminal of the transistor M_{1B}, similarly to the current mirror shown in Figure 5c, by using the protection transistor M_{8A}. The same technique is applied to the NMOS transistors. This greatly enhances the amplifier differential voltage gain and common-mode rejection, as explained in the next section. Table 3 summarizes the transistor dimensions.

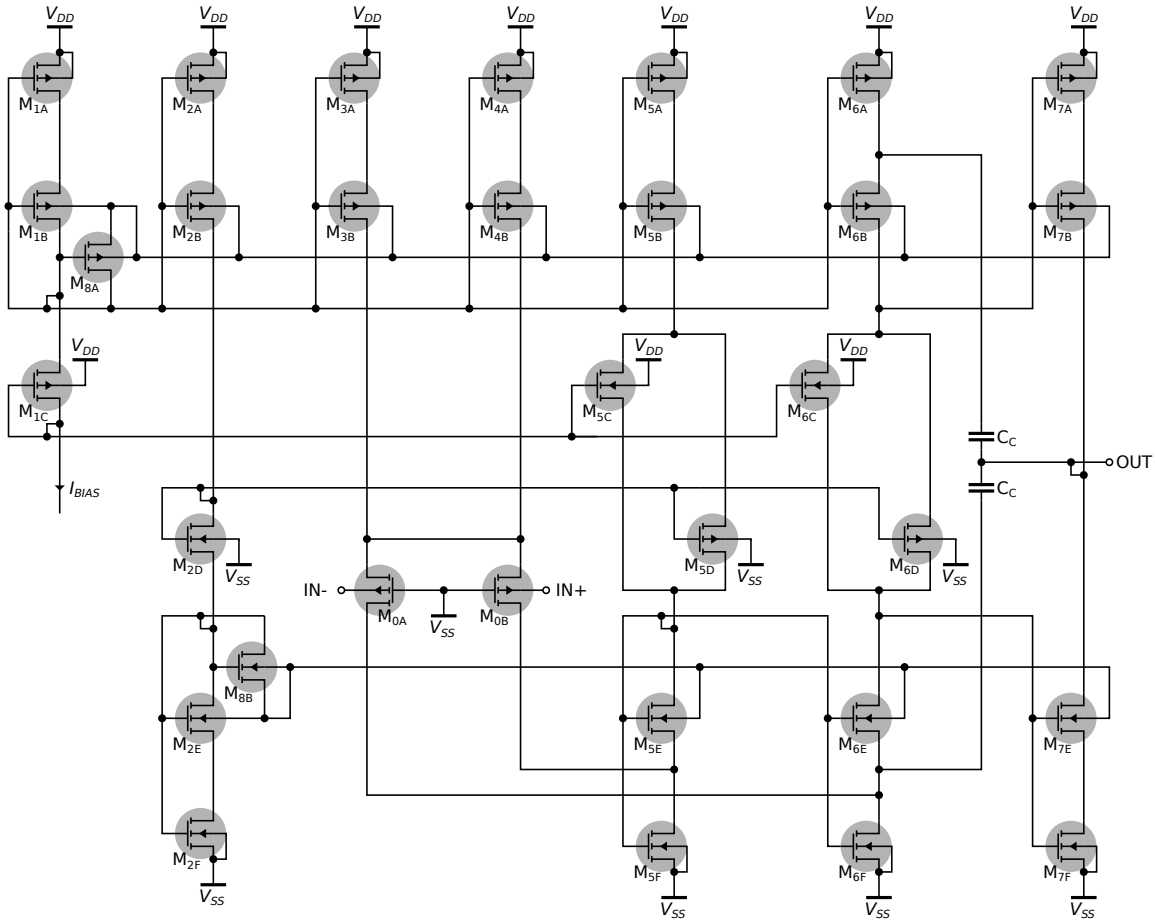


Fig. 8: Proposed bulk-driven rail-to-rail class AB operational amplifier with Improved Composite Transistors (ICT)

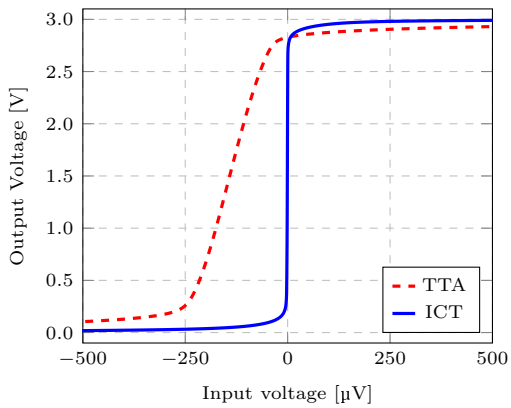
Table 3: Proposed bulk-driven rail-to-rail class AB operational amplifier transistor dimensions (ICT)

	k × $(m:n)$	W/L (µm/µm)		k × $(m:n)$	W/L (µm/µm)		k × $(m:n)$ -	W/L (µm/µm)
$M_{0A,B}$	4 × (8:1)	2.0/0.5	$M_{1\text{-}6A}$	4 × (2:4)	2.0/0.5	$M_{1\text{-}6B}$	4 × (4:2)	2.0/0.5
$M_{2,5,6E}$	4 × (1:8)	2.0/0.5	$M_{2,5,6F}$	4 × (2:4)	2.0/0.5	M_{1C}	4 × (4:4)	2.0/0.5
$M_{5,6C}$	4 × (2:4)	2.0/0.5	M_{2D}	4 × (2:8)	2.0/0.5	$M_{5,6D}$	4 × (1:8)	2.0/0.5
M_{7A}	4 × (4:2)	2.0/0.5	M_{7B}	4 × (8:1)	2.0/0.5	M_{7E}	4 × (2:4)	2.0/0.5
M_{7F}	4 × (4:2)	2.0/0.5	M_{8A}	4 × (8:1)	2.0/0.5	M_{8B}	4 × (4:2)	2.0/0.5

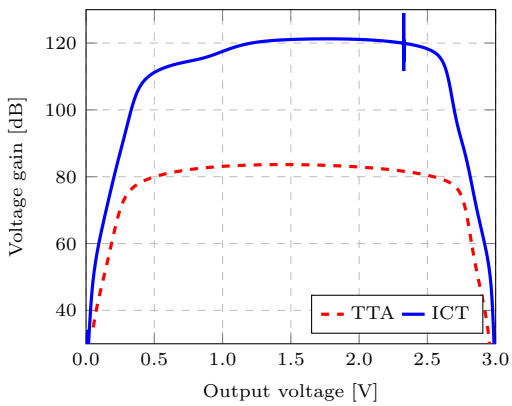
5 Simulation Results

The previously discussed OTA topologies were designed using the Skywater 130 nm process technology and simulated with a 4 µA biasing current, 3.0 V power supply, and room temperature.

Fig. 9a shows both OTAs' input-output DC characteristic curves for a differential input. As can be seen, the ICT OTA has a much steeper slope, while maintaining the same voltage excursion. This aspect is made evident in Fig. 9b, which shows the DC output voltage gain as a function of the output voltage, as the RTA OTA voltage gain is limited to over 80 dB for output voltages from 0.3 to 2.7 V, while the ICT OTA has voltage gains over 110 dB for about the same output excursion.

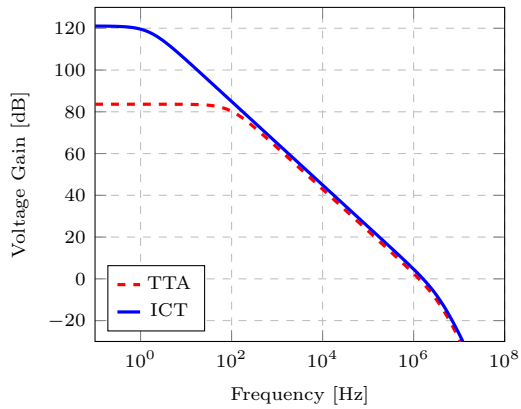


(a)

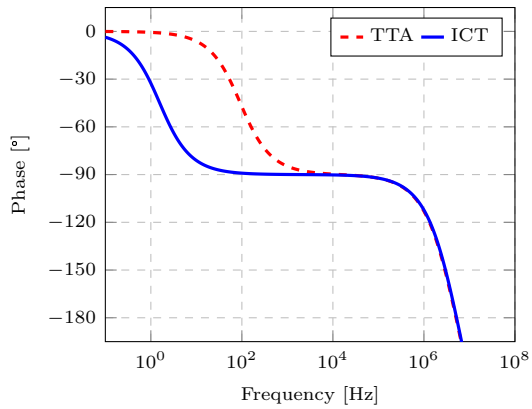


(b)

Fig. 9: Open-loop DC simulation results: (a) input-output voltage characteristic curve, and (b) voltage gain vs. output voltage



(a)



(b)

Fig. 10: Open-loop AC simulation results: (a) differential voltage gain, and (b) output phase

This large-signal DC voltage gain improvement is translated to a better small-signal AC gain. Figs. 10a and 10b show the open-loop differential voltage gain and phase AC simulation results for a 10 pF capacitive load, and 0.8 pF Miller capacitors C_C. Both RTA and ICT OTA versions have similar gain-bandwidth performance (GBW), achieving 13.1 and 16.1 MHz, and 60.2 and 55.0° phase margin, while consuming 122 and 121 µW power, respectively, for a 3.0 V supply voltage. The main difference, as expected, is the DC voltage gain, as the ICT achieves 121 dB, while the RTA one is 84 dB, resulting in a 37 dB improvement.

Also, as can be seen in Figs. 11 and 12, there is a significant increase of Common-Mode and Power Supply Rejection Ratio, as a direct result of the current mirror improvement, mostly as consequence of the differential pair common-mode rejection, on top of the improved differential voltage gain.

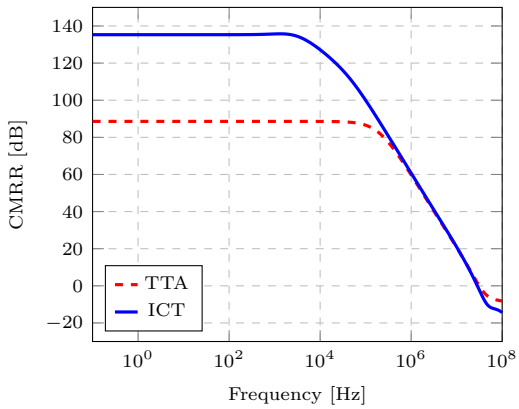


Fig. 11: Open-loop AC Common-Mode Rejection Ratio (CMRR) simulation results

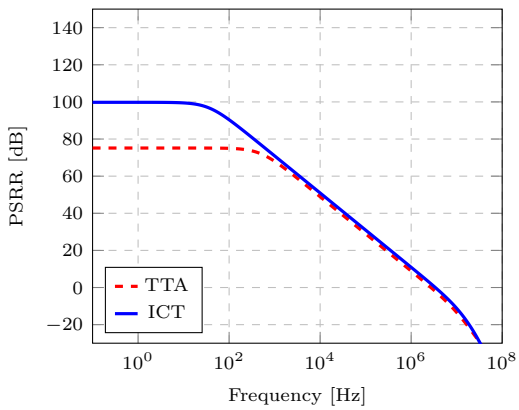


Fig. 12: Open-loop AC Power Supply Rejection Ratio (PSRR) simulation results

Fig. 13 shows the transient simulation results for rail-to-rail sinusoidal voltage input and a voltage follower amplifier configuration, with the output and inverting terminals connected to each other. As can be seen, both OTA versions have nearly identical output responses and follow the input without apparent distortion for a 100 kHz, 2.9 V peak-to-peak signal. Their output Total

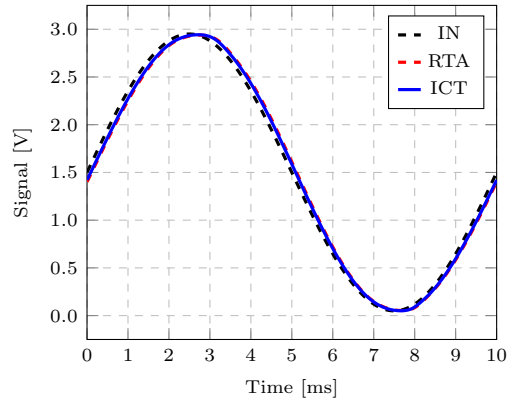


Fig. 13: Voltage follower transient simulation results for rail-to-rail sinusoidal input

Harmonic Distortion are 1.37 and 1.11 %, respectively.

Fig. 14 shows the amplifiers output response for a large 2.9 V peak-to-peak amplitude step signal. Both amplifiers show positive and negative slew rate of about 4.0 and 2.4 V/µs, respectively. Meanwhile, Fig. 15, shows the amplifiers output response for a small 100 mV peak-to-peak amplitude step signal. There is an small overshoot of 8 and 13% for the TTA and ICT versions, respectively, not present in the large signal output, which is a result of the amplifier phase margin being near 60°.

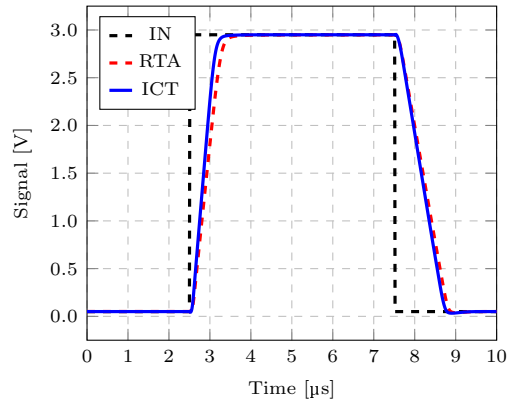


Fig. 14: Voltage follower transient simulation results for rail-to-rail step input

Both amplifiers have a quiescent current of about 40 µA, but can drive loads up to 1.2 mA in an almost symmetrical fashion, in the voltage follower configuration, as can be seen in Figure

16. However, the ICT version has a much higher voltage gain, which translates into a much smaller output resistance.

Table 4 shows the performance comparison table. The designs from [5] and [12, 15] are conventional class A two-stage Miller amplifiers, but the former uses composite transistors (CT), while the latter use improved composite transistors (ICT). The OTA proposed in [12] was designed to achieve high-speed performance instead of DC voltage gain, so it has a much larger power consumption and GBW than the others. It also achieved a very high FoM, as it is very power efficient due to its cascoded-Miller frequency stabilization circuit, which is slightly more complex than the simple Miller capacitor used in the other class A amplifiers.

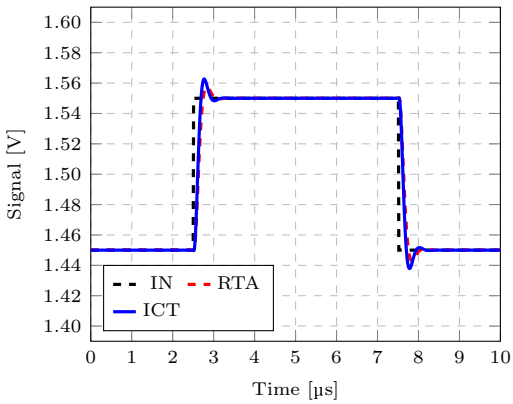


Fig. 15: Voltage follower transient simulation results for small-signal step input

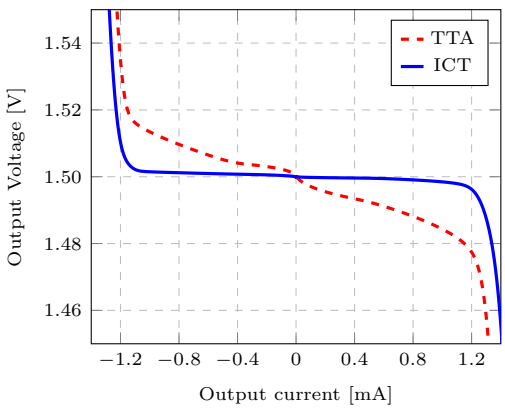


Fig. 16: Voltage follower DC simulation results for varying current output load

The original amplifier with the compact class AB stage uses an older 1.0 µm process node. It is not as efficient as the other gate-driven topologies, as it needs extra biasing circuits for the rail-to-rail common-mode input technique. The bulk-driven OTA [18] was designed for ultra-low-voltage supplies and ultra-low-power, and also uses composite transistors. It has a very low power efficiency, as its, the bulk-to-drain transconductance is a fraction of the gate-to-drain one, and it uses the simples Miller frequency stability compensation.

The proposed amplifiers, as compared to the original bulk-driven amplifier, are much more efficient, as it uses cascode-Miller compensation. Their voltage gain is also superior by orders of magnitude, as it uses the improved composite transistors. Nonetheless, their minimum supply voltage is limited by the compact AB output-stage biasing circuit.

6 Conclusion

This paper explores the use of the transistor bulk terminal the operational amplifier design. In particular, the forward-body-biasing can be used in a safe way for typical supply voltages, and how it can be used to improve an amplifier voltage gain without decreasing output swing by using improved self-biased current mirrors. The same technique can be applied to many other applications, as current mirrors are found everywhere in analog circuit design.

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Table 4: Performance Comparison

	[5]+ CT	[12]* ICT	[15]* ICT	[17]+ -	[18]+ TTA	This work* TTA	This work* ICT	Unit
Technology	250	180	180	1000	350	130	130	nm
Supply Voltage (VDD)	2.0	1.8	3.3	3.3	0.6	3.0	3.0	V
Power	110	720	6.5	594	0.55	122	121	µW
Voltage Gain (A_V)	117	96	155	82	69	83	121	dB
CMRR	-	-	-	70	75	89	136	dB
PSRR	-	-	-	-	54	75	100	dB
Total Harmonic Distortion	-	-	-	-	62	37	39	dB
	-	-	-	-	@ 0.52	@ 2.9	@ 2.9	$V_{p\text{-}p}$
Slew Rate +/-	0.27/0.43	-	-	-	0.015	4.0/2.5	5.0/2.6	V/µs
Gain-Bandwidth (GBW)	1.2	146	0.198	6.4	0.011	13.1	16.1	MHz
Phase Margin	43	70	59	53	65	60	54	°
Capacitive load (C_L)	100	15	10	10	15	10	10	pF
FoM	218	546	102	36	18	32	40	V^{-1}

+ Measured, * Simulated, FoM: 100 × GBW × C_L/I_T, CT: Composite Transistor, RTA: Rectangular Transistor Array, ICT: Improved Composite Transistor.

Statements and Declarations

Data Availability Statement All data generated or analysed during this study are included in this published article.

Conflict of Interest There are no conflicts of interest.

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