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A Unified Model of Drain Current Local Variability due to Channel Length Fluctuation for an n-channel EδDC MOS Transistor

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Abstract A drain current local variability compact model due to random fluctuation of channel length induced by line edge roughness/line width roughness (LER/LWR) is derived here. The random fluctuation of channel length leads to correlated fluctuations of threshold voltage and effective mobility of the current carriers. Therefore, an unified compact model is required to combine all the causes. Our model is based on the principle of propagation of variance. For the model verification purpose, calibrated technology computer aided design (TCAD) simulation platform is extensively used for all possible bias regions and several LER profile parameters. Channel profile optimization is critically studied aiming reduction of I_D variability.

The model is further extended for SOI (Silicon-on-insulator) transistor and validated with literature data of threshold voltage and on-current variability.

Keywords Epitaxial delta doped channel · line edge roughness · channel length fluctuation · propagation of variance · roughness amplitude · correlation length.

1 Introduction

In nano-scale CMOS analog circuits, mismatch between the drain currents of two identical transistors placed adjacent to each other is attributed to few

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major causes like random discrete dopant effect (RDD), line edge/line width roughness (LER/LWR), metal gate granularity etc [1]. The line edge roughness (LER) phenomenon arises due to i) sub-wavelength lithography and/or ii) intrinsic non-uniformity of the photoresist used in the process technology [2]. LER leads to variation in critical dimension of the feature size. The amplitude of roughness (σ_{LER}) remains almost same and does not scale down with technology. Therefore, as the device dimensions, especially the channel length and width becomes comparable with this magnitude, LER/LWR-induced performance variability of a device/circuit appears to be quite critical [3].

1.1 Literature Survey and Motivation

In literature, the LER phenomenon has been studied primarily from two perspectives, i) its process level mitigation and ii) its impact on device performance. Several alternative patterning methods like extreme ultra violet lithography (EUVL), electron beam lithography (EBL), mask-less lithography, nanoimprint lithography etc. are being considered for enhanced resolution of the device dimension [4]. On the other hand, modeling and simulation of roughness and its impact on MOSFET, DGFET, FinFET etc. device performances have also been widely studied and reported. The variability impact of LER on sub 32 nm FinFET technologies is investigated from both device and circuit level perspectives using computer-aided design simulations in [5]. In [6] impact of LER along with other variability sources are reported for a Tunnel FET. A 3-D quasi-atomistic simulation methodology for LER in nonplanar devices, like FinFETs and gate-all-around (GAA) FETs, is proposed in [7]. The work reported in [8], describes the LER induced V_T variability for 14 nm underlap FinFET using 3-D numerical simulations. For a better understanding of the performance variability induced by LER, modeling of the performance variability becomes indispensable. A tapered fin percolation model (TFPM) for evaluation of V_T variability due to fin edge roughness (FER) of a FinFET is formulated in [9]. The model is based on a number of stochastically generated tapered fin structure with a minimum, maximum and average fin width. It can accurately capture the impact of associated physical parameters on V_T variability. The model is extended for the formulation of drain current variability due to FER for a FinFET in [10]. On-current, off-current and sub-threshold slope variability due to FER are reported as well. Another model for V_T variability formulated for a double gate MOSFET is reported in [11]. Unlike the previous one this model is physics-based and premises on the solution of 2D Poisson's equation. Here LER induced fluctuation occurs in the silicon body thickness. However neither of the above works give any compact model of V_T or I_D variability.

The major motivation behind undertaking the present research work is the lack of a suitable physics based compact drain current local variability model which incorporates the effect of line edge roughness on statistical fluctuation of the channel length.

1.2 Outline and Contribution of our Work

An $E\delta DC$ transistor is a device structure proposed by us which is reported to be a low-power, low-cost transistor, suitable for SoC applications with controlled process variability effects due to random discrete dopant effects [12], [13], [14], [15], [16], [17]. In the present work, we derive a physics based local drain current variability model of an epitaxial delta doped channel MOS ($E\delta DC$) transistor, caused due to random fluctuation of channel length, attributed to the LER/LWR phenomenon. The theoretical formulation of the model is based on the principle of propagation of variance. Assuming small fluctuation, first order Taylor's series is considered. The process varying parameters are i) channel length , ii) threshold voltage (V_T), and iii) effective mobility. V_T variability is induced due to channel length fluctuation and effective mobility varies due to fluctuating velocity saturation effect. The model predicted results are verified through calibrated technology computer aided design (TCAD) simulation platform. The model is verified for all possible bias regions and several LER profile parameters. Channel profile optimization is critically studied aiming reduction of drain current variability. The model is further extended for SOI (Silicon-on-insulator) transistor and validated with literature data of threshold voltage and on-current variability.

The local drain current variability is high when the transistor operates in the weak inversion mode (WI), compared to when operates in the strong inversion (SI) mode. In WI mode, local drain current variability depends on two factors, i) on channel length variability itself and ii) correlated V_T variability. In SI mode, correlated effective mobility fluctuation component is also present apart from the components present in WI mode. As velocity saturation effect is more pronounced at high drain bias it contributes to the increased drain current variability at high drain bias apart from V_T variability component.

The major salient features of our variability compact model are: (i) The formulation of the model is based upon the principle of propagation of variance, which is a formal theory of mathematical statistics. Our model encapsulates the device architecture through the use of appropriate compact model of the device architecture. By re-definitions of few device parameters, the model may thus easily be extended to other device structures such as SOI structures, which we have shown in this work. (ii) The present model of local drain current variability being a compact model gives an insight on the minimization approaches of variability through device design and optimization. (iii) The model does not involve purely empirical parameters.

1.3 Organization of the Work

The model of the σ_{I_D} is derived in Section II, where we recall σ_{V_T} formulation from previous work in brief. The verification the model with calibrated TCAD simulation results and the approaches for reduction of σ_{I_D} is discussed in Section III. The extension of the model for SOI transistors and its validation with

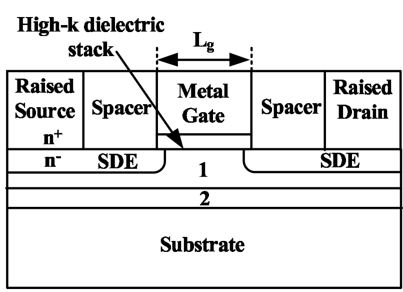

Fig. 1 Schematic diagram of an Epitaxial δ doped n-channel MOS transistor used for design purpose.

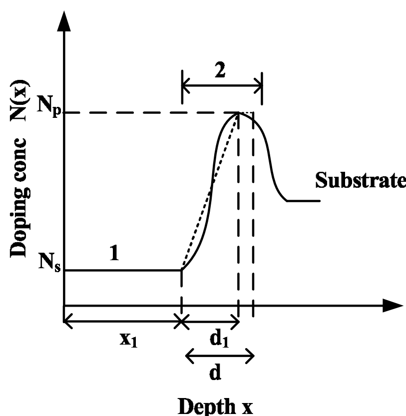

Fig. 2 Graded retrograde approximation of the channel profile of EδDC transistor.

reported data are also mentioned in Section IV. Finally Section V concludes the paper.

2 Theoretical Formulation of the Model

2.1 Background Information

The cross-section and channel doping profile of the n-channel EδDC transistor are as shown in Fig. 1 and Fig. 2. The significance of the various symbols used to represent the channel doping profile are as used in [18].

The threshold voltage for a short channel transistor, in the presence of the applied drain bias is written as [19],

$$V_T = V_{Tl} - \frac{2\left(V_{bi} - \psi_S\right) + V_{DS}}{2\cosh\left(\frac{L}{2l_t}\right) - 2} \tag{1}$$

where V_{Tl} is the long channel threshold voltage, V_{bi} is the built-in potential across the S/D junctions, $\psi_s = 2\Phi_F$ is the surface potential at strong inversion and l_t is the characteristic length.

Using the principle of propagation of variance, random V_T variability due to channel length fluctuation is given by [18],

$$\sigma_{V_T} = \sqrt{\left(\frac{\partial V_T}{\partial L}\right)^2}\sigma L \tag{2}$$

where threshold voltage sensitivity w.r.t. channel length is obtained using (1) as follows.

$$\frac{\partial V_T}{\partial L} = \frac{2\left(V_{bi} - \psi_S\right) + V_{DS}}{4l_t\left[\cosh\left(\frac{L}{2l_t}\right) - 1\right]^2}\sinh\frac{L}{2l_t} \tag{3}$$

Due to the presence of LER/LWR, the average channel length of a transistor, becomes a random variable. σ_L represents the variability of average channel of a transistor. Line edge roughness, and hence, σ_L induced by LER is defined by correlation length Λ and the rms roughness amplitude σ_{LER}, as follows [20], [21], [22]. Here we assume uncorrelated edge variation, which gives channel length variability as follows [6], [23],

$$\sigma_L = \frac{\sigma_{LWR}}{\sqrt{1 + 0.75\frac{W}{\Lambda}}} = \sqrt{\frac{2}{1 + 0.75\frac{W}{\Lambda}}}\sigma_{LER} \tag{4}$$

2.2 Formulation of Drain Current Variability

The drain current I_D of a MOS transistor is related to several process parameters, which is mathematically represented by

$$I_D = f(\bar{P}) \tag{5}$$

where $\bar{P}$ represents the vector of process parameters. Also we assume that the deviation/fluctuation in a certain parameter, symbolized as δP_i is much smaller than the value of the parameter P_i itself. Therefore, we employ first order Taylor's series expansion to write

$$\frac{\delta I_D}{I_D} \approx \frac{1}{I_D}\frac{\partial I_D}{\partial P_1}.\delta P_1 + \frac{1}{I_D}\frac{\partial I_D}{\partial P_2}.\delta P_2 + ... \tag{6}$$

The distribution of drain current samples for large number may be approximated to be a normal distribution, characterized by sample mean and standard deviation. The dispersion characteristics being more important in characterizing the variability aspect, we work with this parameter in our present work. From (6) the variance for three input parameters is written as

$$\begin{aligned}\frac{\sigma_{I_D}^2}{I_D^2} &= \left(\frac{1}{I_D}\frac{\partial I_D}{\partial P_1}\right)^2.\sigma_{P_1}^2 + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial P_2}\right)^2.\sigma_{P_2}^2 + \\ &\left(\frac{1}{I_D}\frac{\partial I_D}{\partial P_3}\right)^2.\sigma_{P_3}^2 + \frac{2}{I_D^2}\frac{\partial I_D}{\partial P_1}\frac{\partial I_D}{\partial P_2}.\rho_{12}\left(P_1, P_2\right).\sigma_{P_1}.\sigma_{P_2} + \\ &\frac{2}{I_D^2}\frac{\partial I_D}{\partial P_2}\frac{\partial I_D}{\partial P_3}.\rho_{23}\left(P_2, P_3\right).\sigma_{P_2}.\sigma_{P_3} + \\ &\frac{2}{I_D^2}\frac{\partial I_D}{\partial P_3}\frac{\partial I_D}{\partial P_1}.\rho_{31}\left(P_3, P_1\right).\sigma_{P_3}.\sigma_{P_1}\end{aligned} \tag{7}$$

Here the factor ρ characterizes the correlation between the input parameters. For perfect correlation, which occurs when the parameters are analytically related, the value of the correlation coefficient may be assumed to be unity.

The choice of each of the process parameter P_i is based upon physics of the transistor. The sensitivity of the drain current with respect to these process parameters may be evaluated either through simulation method or through analytical method. In our work, we prefer the later and select appropriate compact model to describe the relationship between the drain current and the chosen process parameters.

2.3 Drain Current Fluctuation through Charge based Model

EKV drain current model, which smoothly describes the device operation in all the modes of operation is used to analyze drain current variability induced by LER/LWR [24], [25]. The average value of drain current is given as,

$$I_D = I_S\left(i_f - i_r\right) \tag{8}$$

where, $I_S = 2n\mu_{eff}C'_{ox}\frac{W}{L}\phi_t^2$ is called the specific current, and i_f and i_r are normalized forward and reverse currents with the normalization factor as I_S. n, C'_{ox}, μ_{eff} and ϕ_t are the slope of gate-to-body voltage versus surface potential graph, the gate oxide capacitance per unit area, the effective mobility and the thermal voltage respectively. $i_{f/r}$ is as follows.

$$i_{f/r} = \left[\ln\left\{1 + \exp\left(\frac{V_P - V_{S/D}}{2\phi_t}\right)\right\}\right]^2 \tag{9}$$

Here V_P is the pinch-off voltage, approximately written as,

$$V_P = \frac{V_G - V_T}{n} \tag{10}$$

Here, source being the reference terminal, $V_S = 0$. Normalized fluctuation of drain current due to L fluctuation and correlated V_T and μ_{eff} fluctuations thus becomes,

$$\begin{aligned}\frac{\delta I_D}{I_D} &= \frac{1}{I_D}\frac{\partial I_D}{\partial \mu_{eff}}\delta\mu_{eff} + \frac{1}{I_D}\frac{\partial I_D}{\partial L}\delta L + \frac{1}{I_D}\frac{\partial I_D}{\partial V_T}\delta V_T \\ &= \frac{\delta\mu_{eff}}{\mu_{eff}} - \frac{\delta L}{L} + \frac{1}{i_f - i_r}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)\delta V_T\end{aligned} \tag{11}$$

The forward and reverse current derivatives w.r.t. V_T referred in (11) are evaluated as follows.

$$\frac{\partial i_f}{\partial V_T} = \frac{\ln\left[1 + \exp\left(\frac{V_P}{2\phi_t}\right)\right]}{1 + \exp\left(\frac{V_P}{2\phi_t}\right)}.\frac{1}{\phi_t}\frac{\partial V_P}{\partial V_T} \tag{12}$$

$$\left.\frac{\sigma_{I_D}^2}{I_D^2}\right|_{WI} = \frac{\sigma_L^2}{L^2} + \frac{1}{(i_f - i_r)^2}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)^2 \sigma_{V_T}^2 - 2\frac{\sigma_L}{L}\frac{1}{(i_f - i_r)}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)\sigma_{V_T} \tag{16}$$

$$\frac{\partial i_r}{\partial V_T} = \frac{\ln\left[1 + \exp\left(\frac{V_P - V_{DS}}{2\phi_t}\right)\right]}{1 + \exp\left(\frac{V_P - V_{DS}}{2\phi_t}\right)} . \frac{1}{\phi_t}\frac{\partial V_P}{\partial V_T} \tag{13}$$

where, $\frac{\partial V_P}{\partial V_T} = -\frac{1}{n}$. In (11) both μ_{eff} and V_T fluctuation roots from channel length fluctuation. Hence they are correlated.

If we now investigate (11), we see that the second term is independent of the bias region. The third term consisting of interpolation function, takes the corresponding limiting forms in different bias regions. The first term, i.e., mobility fluctuation needs a close inspection w.r.t. the nature of inversion region.

2.4 Drain Current Variability in Weak Inversion (WI) Mode

Velocity saturation effect being insignificantly small, can be neglected here. Hence, $\mu_{\text{eff}} = \mu_s$, where, μ_s is the surface mobility. In WI mode, surface mobility is solely dependent on Coulomb scattering of the carriers. i) The ionized impurity atoms present in the channel and ii) the remote fixed charges existing inside the high-k dielectric (Remote Coulomb Scattering or RCS effect) act as the scattering centers. For low normal electric field, the inversion carriers experience surface mobility as follows [26]

$$\frac{1}{\mu_s} = \frac{1}{\mu_B} + \frac{1}{\mu_{RCS}} \approx \frac{1}{\mu_{00}} + \alpha_d.Q_{imp} \tag{14}$$

Here, RCS effect is embedded in μ_{00} and it is termed as the zero field mobility. Coulomb scattering with the impurity atoms is represented by the term $\alpha_d.Q_{imp}$, α_d being the Coulomb scattering parameter. However, channel length of the transistor does not have any impact on the scattering phenomena. Hence surface mobility fluctuation term on R.H.S. of (11) vanishes.

$$\frac{\delta\mu_{\text{eff}}}{\mu_{\text{eff}}} = \frac{\delta\mu_s}{\mu_s} = 0 \tag{15}$$

Thus normalized variance of drain current in weak inversion mode is thus given by (16).

The last term in (16) is the correlation coefficient. The current sensitivities are calculated using (12) and (13).

$$\left.\frac{\sigma_{I_D}^2}{I_D^2}\right|_{SI} = \frac{\sigma_{\mu_{eff}^2}}{\mu_{eff}^2} + \frac{\sigma_L^2}{L^2} + \frac{1}{(i_f - i_r)^2}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)^2 \sigma_{V_T}^2 - 2\frac{\sigma_{\mu_{eff}}}{\mu_{eff}}\frac{\sigma_L}{L} - 2\frac{\sigma_L}{L}\frac{1}{(i_f - i_r)}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)\sigma_{V_T} + 2\frac{\sigma_{\mu_{eff}}}{\mu_{eff}}\frac{1}{(i_f - i_r)}\left(\frac{\partial i_f}{\partial V_T} - \frac{\partial i_r}{\partial V_T}\right)\sigma_{V_T} \tag{21}$$

2.5 Drain Current Variability in Strong Inversion (SI) Mode

In strong inversion (SI) mode, The effective mobility is [25]

$$\mu_{\text{eff}} = \frac{\mu_s}{1 + \frac{\mu_s V_{DS}}{L v_{\text{sat}}}} \tag{17}$$

here μ_s represents the surface carrier mobility and v_{sat} represents the saturation velocity of the inversion carriers.

To evaluate fluctuation of μ_{eff}, in SI mode, we refer to (17), which on partial differentiation w.r.t. L, gives,

$$\delta\mu_{eff} = \mu_{eff}^2 \frac{V_{DS}}{v_{sat}L^2}\delta L = \left(\frac{\mu_s}{1 + \frac{\mu_s V_{DS}}{L v_{\text{sat}}}}\right)^2 . \frac{V_{DS}}{v_{sat}L^2}\delta L \tag{18}$$

In this mode of operation, surface roughness scattering and lattice vibration dominates surface mobility [27]. An efficient surface mobility model which includes the mobility degradation effect is as follows.

$$\mu_s = \frac{\mu_0}{1 + \theta_1 (V_{GS} - V_T) + \theta_2 (V_{GS} - V_T)^2} \tag{19}$$

Here θ_1 and θ_2 are the parameters to account for the mobility degradation effect [28], [29]. μ_0 represents low field mobility of the inversion carriers, which includes both the Coulomb scattering effects as mentioned in the previous section. In presence of the series source/drain (S/D) resistance mobility degradation parameter θ_1 is modified as [28]

$$\theta_1 = \theta_1^* + \frac{C_{ox} R_{SD} W \mu_0}{L} \tag{20}$$

Here, θ_1^* is the coefficient of mobility degradation in absence of source/drain resistance and R_{SD} is the source/drain series resistance. The values of the mobility degradation coefficients are extracted from extensive TCAD simulation.

The normalized drain current variability due to channel length fluctuation in SI mode is thus given by (21).

The last three terms in (21) represent the corresponding correlation coefficients. The current sensitivities are calculated using (12) and (13). Effective mobility variability is derived using (18) as,

$$\frac{\sigma_{\mu_{eff}^2}}{\mu_{eff}^2} = \left(\frac{\mu_s}{1 + \frac{\mu_s V_{DS}}{L v_{\text{sat}}}}\right)^2 \cdot \left(\frac{V_{DS}}{v_{sat}L^2}\right)^2 \sigma_L^2 \tag{22}$$

3 Model Implementation and Validation

3.1 Device Simulation

The n-channel EδDC MOS transistor parameters are selected for high performance applications according to the International Technology Roadmap for Semiconductors 2010 version. The models for different physical effects are included in the simulation as discussed in [13], [17]. The channel length varaibility due to LER is simulated using monte carlo simulation for 200 samples. The channel length of 200 EδDC transistors are normally distributed around its nominal value (here 16 nm) with a spread of σ_L. The value of σ_L is calculated for a particular set of Λ and σ_{LER} values using 4.

3.2 Model Parameter Calculation

The analytical model incorporates various empirical parameters like, μ_0, θ_1 and θ_2. The extraction methods of these parameters are reported in [17]. Their extracted values are, $\mu_0 = 202cm^2/V.s$, $\theta_1 = 0.845/V$ and $\theta_2 = 2.07/V^2$ following [30].

3.3 Variation of Local Drain Current Variability with Bias

As the transistor moves from weak inversion (WI) mode to strong inversion (SI) mode, the variability gradually decreases, as can be seen from Fig. 3. This is due to the fact that the deterministic drain current (I_D) is less by several orders in WI mode compared to SI mode. This leads to the nature of variation of normalized drain current variability even for similar fluctuation σI_D over the entire gate bias range.

As evident from (16) In the weak inversion mode (WI), the local drain current variability depends upon three factors: the channel length variability, the threshold voltage variability and the correlation factor. Since the channel length variability term is bias independent, the drain bias dependence comes from the remaining two components. Moreover, we observe that higher drain current variability is more pronounced in WI mode compared to strong inversion (SI) mode. Though σ_{V_T} is independent of the bias mode (weak or strong), the higher drain current variability for high drain bias at WI mode, compared to SI mode results from exponential drain bias dependence of inversion charge at drain end in WI mode compared to its linear drain bias dependence in SI mode [25].

However, as we can see from (21) , in SI mode, correlated effective mobility fluctuation component is also present apart from the components present in WI mode. As velocity saturation effect is more pronounced at high V_{DS} , it contributes to the increased drain current variability at high drain bias apart from V_T variability component. An important point for EδDC transistor may

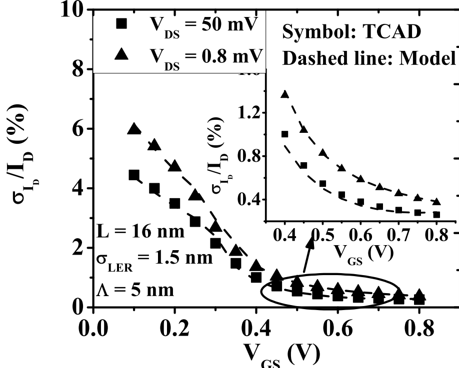

Fig. 3 Variation of the normalized drain current variability with V_{GS} for L = 16 nm at low and high drain biases.

be noted here. We reported in our earlier works [13], [17], that the threshold voltage variability at high drain bias is not much significant. The excellent agreement between TCAD simulation and analytical results confirms perfect capture of bias dependence of the model.

3.4 Local Drain current Variability for different LER profile parameters

In Fig. 4(a), the variation of normalized local drain current variability due to random variation of channel length is reported for low drain bias and for a range of σ_{LER} values. For this observation Λ is kept fixed at 5 nm. With increasing σ_{LER}, channel length variability increases linearly following (4). Increased channel length variability induces increased V_T variability and hence normalized drain current variability due to channel length variability enhances. A similar variation is reported in Fig. 4(b) for high value of drain-to-source voltage. As discussed in a previous subsection, we see here that nature of the graphs remaining similar to those at low V_{DS}, variability values are higher for high V_{DS}, which is a consequence of higher σ_{V_T} for high V_{DS}.

The nature of graphs given in Fig. 4(a) and Fig. 4(b) are not only physically justified, but also this physics is perfectly incorporated in the model. This is evident from the very close agreement of the simulation and the model predicted results.

Fig. 5(a) represents the variation of normalized local drain current variability due to random variation of channel length for low drain bias and for a range of Λ values. For this observation σ_{LER} is kept fixed at 1 nm. With increasing Λ, channel length variability increases following (4). Increased channel length variability induces increased V_T variability and drain current variability. However, this enhancement is significant in WI mode of operation. A similar variation is reported in Fig. 5(b) for high value of V_{DS}. Here also σ_{I_D} values

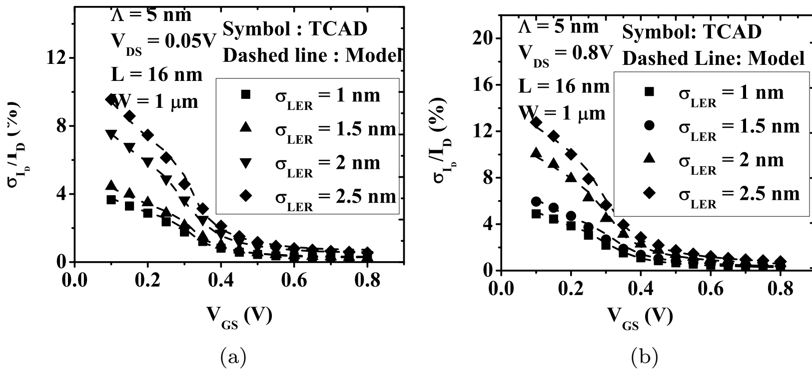

Fig. 4 Variation of normalized drain current variability with applied gate bias for various edge roughness amplitude at $L = 16nm$ at (a) Low V_{DS} and (b) High V_{DS}.

are higher for high V_{DS} as correlated σ_{V_T} increases with increasing drain bias. Here the scalability of model is verified with LER correlation length Λ.

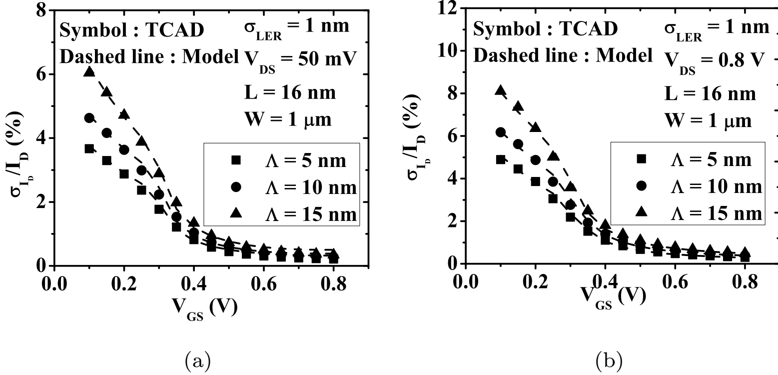

Fig. 5 Variation of normalized drain current variability with applied gate bias for various correlation lengths at $L = 16nm$ at (a) Low V_{DS} and (b) High V_{DS}.

3.5 Reduction of Drain Current Local Variability through Channel Engineering

σ_{I_D} due to variability of channel length induced by LER can be controlled in an EδDC transistor using channel engineering technique. This technique involves the study of variability performance with variation in the profile parameters using analytical model. Here we make all the observations for high drain bias and for a fixed LER profile (Λ=5 nm & σ_{LER}=3 nm), hence for a fixed channel

length variability. If we have a close look at (16) and (21), profile parameter dependence of the normalized drain current variability is only associated with the V_T variability component. In the following discussion we would refer to our observation obtained in [18].

3.5.1 Variation with x_1

In Fig. 6(a), we observe the variation of σ_{I_D}/I_D with gate bias for several epitaxial layer thickness x_1. As we are studying this section for fixed channel length variability, correlated V_T variability differs with change of profile parameter values. With increasing thickness of the low doped layer x_1, depletion depth, W_{dm} increases. Increased W_{dm}, worsens short channel effect (SCE) [15]. Poor SCE is manifested by larger V_T. Hence V_T will be more sensitive to variation in channel length, leading to higher $\frac{\partial V_T}{\partial L}$. Hence, σ_{V_T} increases with increasing x_1. Consequently the contribution of V_T variability associated component of normalized drain current varibility increases and hence σ_{I_D}/I_D goes up. It is observed that as x_1 increases from 5 nm to 15 nm, σ_{I_D}/I_D becomes three times larger for V_{GS}=0.1 V. However this increment lowers as the transistor approaches SI mode of operation.

3.5.2 Variation with N_s

Fig. 6(b) shows the variation of σ_{I_D}/I_D with gate bias for several epitaxial layer doping N_s. With increase of epitaxial layer doping, the short channel effect is controlled, hence the maximum depletion depth and consequently σ_{V_T} is restricted. Lowering of σ_{V_T} in-turn lowers σ_{I_D}/I_D with increasing N_s. The maximum improvement of σ_{I_D}/I_D is by 8.5% which occurs for $V_{GS} = 0.1V$. The improvement gradually diminishes with increase of gate bias and becomes insignificant as the transistor enters in SI mode.

3.5.3 Variation with N_p

Fig. 6(c) shows the variation of $\sigma_{I_D}/\bar{I}_D$ with gate bias for several screening layer doping N_p. Increase in N_p restricts the spread of depletion region beneath the channel. Controlled channel depletion makes SCE better. Hence V_T variability and drain current variability with random variation of channel length is reduced with increasing N_p. However, minimum value of channel depletion is limited by x_1, SCE and hence variability due to random variation of channel length cannot be reduced indefinitely. Consequently, we see in Fig. 6(c), σ_{I_D}/I_D does not reduce significantly, for $N_p \geq 5 \times 10^{19} cm^{-3}$.

In the above observations we find that the impact of all the three profile parameters on drain current variability becomes insignificant as we enter in SI mode. This is because, in SI mode correlated effective mobility fluctuation plays a key role which is independent of channel profile.

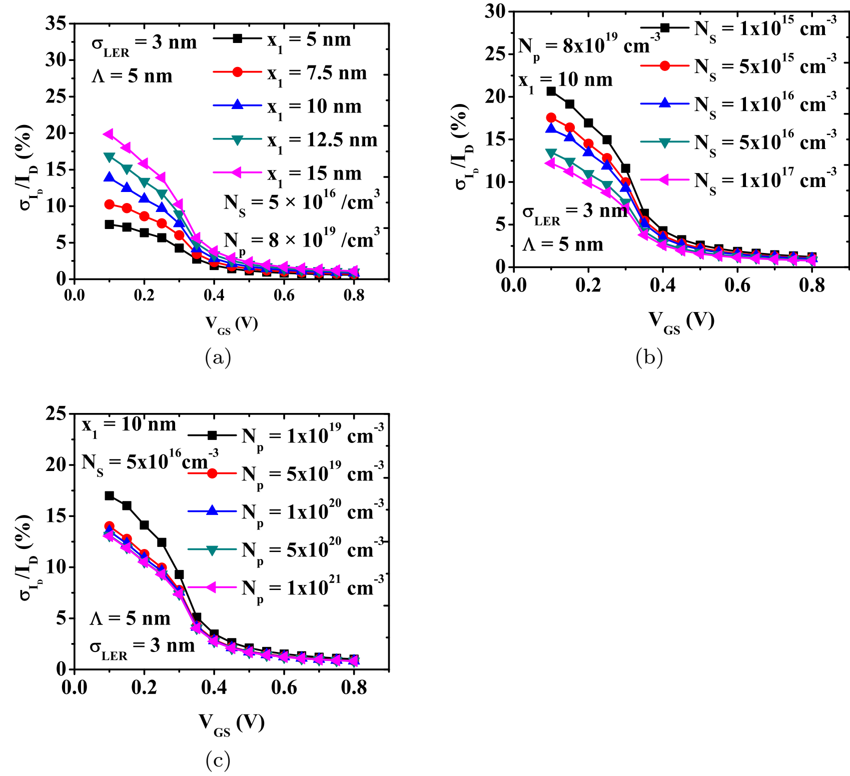

Fig. 6 Effect of channel profile parameters on normalized drain current variability for different values of (a) x_1, (b) N_s and (c) N_p

4 Application of the model for FD-SOI Transistor

The model derived in the present work, can be extended for UTB-FD-SOI MOSFET, with the definition of depletion depth as described in [31]. The results obtained from the extended model for SOI structure are compared with the reported results [32] of atomistic simulation results for V_T variability and local ON current variability due to LER. The comparison is made for all three reported structures with different gate-oxide and body thickness. LER parameters are $3\sigma_{LER}$=2 nm and Λ=25 nm. The model parameters are suitably selected to match the corresponding nominal performances. The validity of the extended model is depicted in Fig. 7, where appreciable accuracy is observed for both V_T and I_{ON} variability. Hence the extended model is verified for the SOI structures.

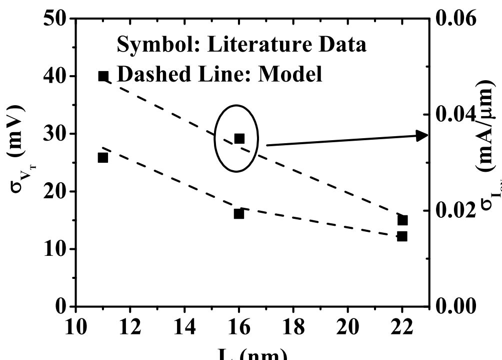

Fig. 7 Verification of the model predicted local ON-current variability result due to LER with atomistic simulation results for a UTB-FD-SOI MOSFET [32].

5 Conclusion

An unified model of drain current local variability due to channel length fluctuation caused by LER phenomenon is reported. The channel length variation leads to correlated variation of threshold voltage and effective mobility of the charge carriers. The drain current variability is significant in weak inversion mode compared to strong inversion mode. The variability is higher for higher drain bias (due to the presence of DIBL) irrespective of mode of operation. In the strong inversion mode, the correlated fluctuation due to effective mobility of the carriers plays an important role. Validation of the model is established by the close agreement between the model predicted results and those obtained from calibrated TCAD results. Further, extensive channel engineering approach prescribes the way for designing an optimal channel profile for the EδDC transistor with minimum V_T and I_D local variability due to channel length fluctuation.

Fine tuning of the correlation components may be included in the model by introducing a general correlation parameter, value of which may be determined from a set of measured data. We have shown the extension of our model to SOI structure. With appropriate use of compact model of nominal drain current and redefinition of some parameters, the model may be extended to tri-gate devices also.

Conflict of interest

The authors declare that they have no conflict of interest.

Author contributions

Both the authors contributed to the conception and formulation of the model. Calibration of the simulator, simulation, model formulation, processing and simulation of the simulated data were done by the corresponding author. Problem formulation, model development and its physical analysis was performed by the second author. The first draft of the manuscript was written by the corresponding author and was critically checked and modified by the second author. Both the authors read and approved the final manuscript.

Availability of data and material

Not Applicable

Compliance with ethical standards

Not Applicable

Consent to participate

Not Applicable

Consent for Publication

Not Applicable

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Figures

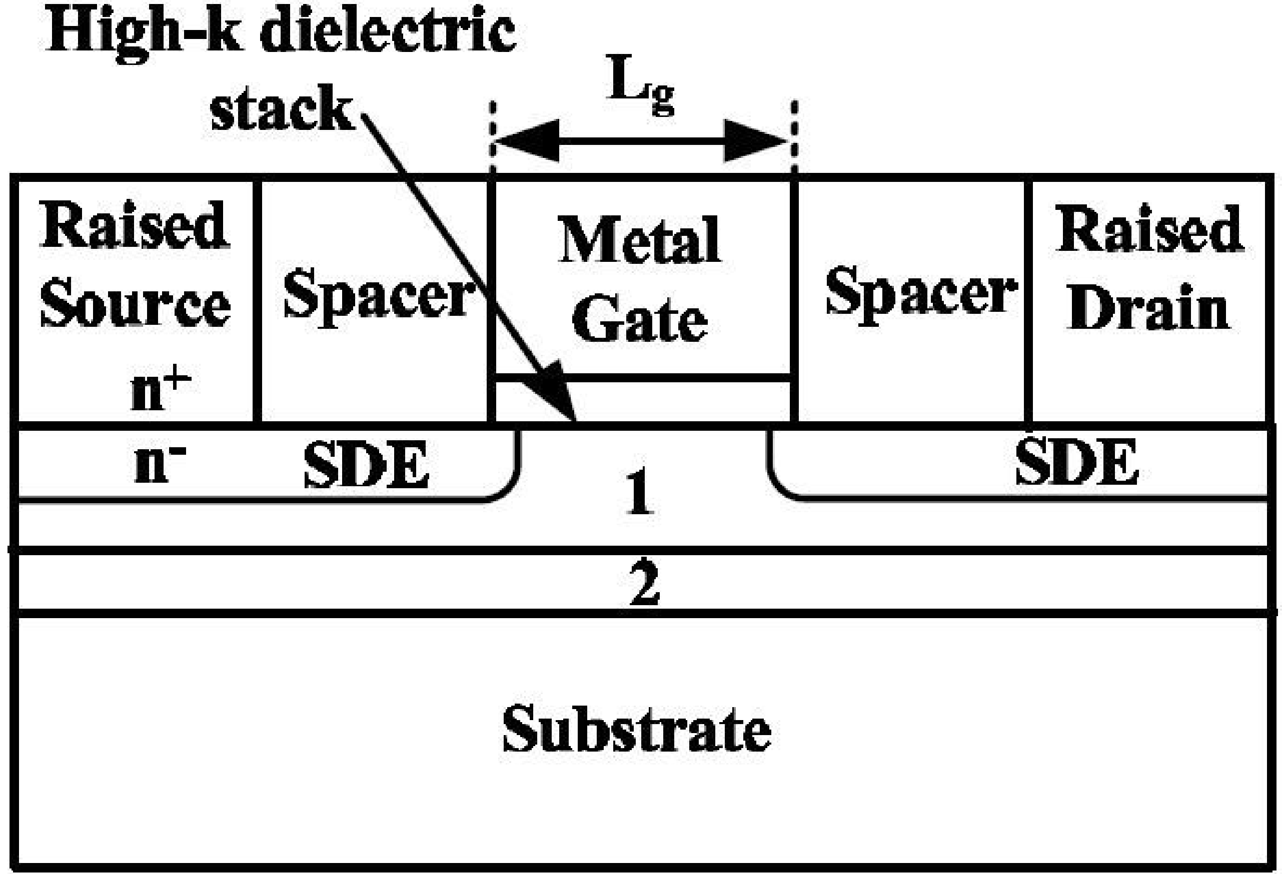

Figure 1

Schematic diagram of an Epitaxial δ doped n-channel MOS transistor used for design purpose.

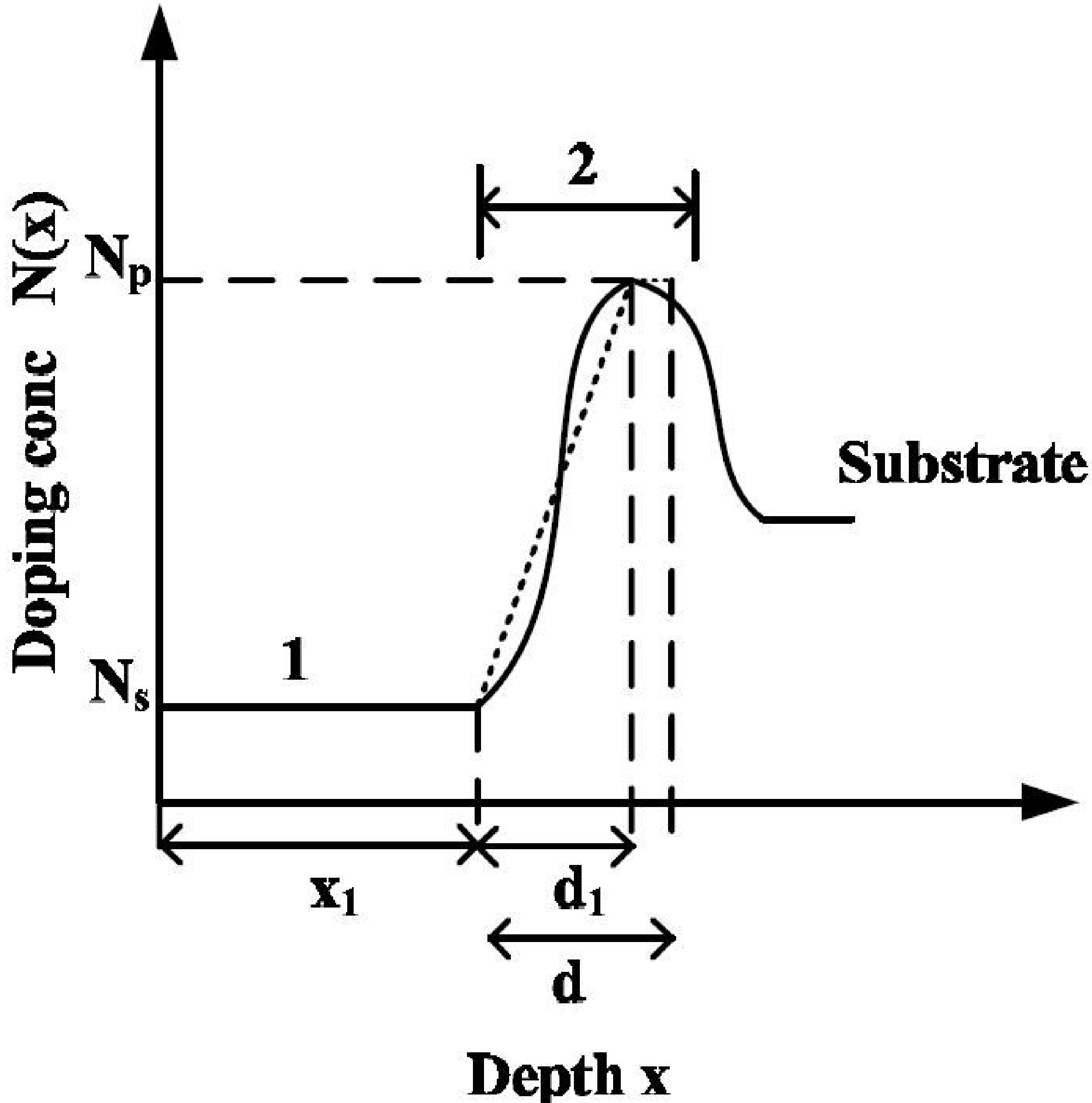

Figure 2

Graded retrograde approximation of the channel profile of EδDC transistor.

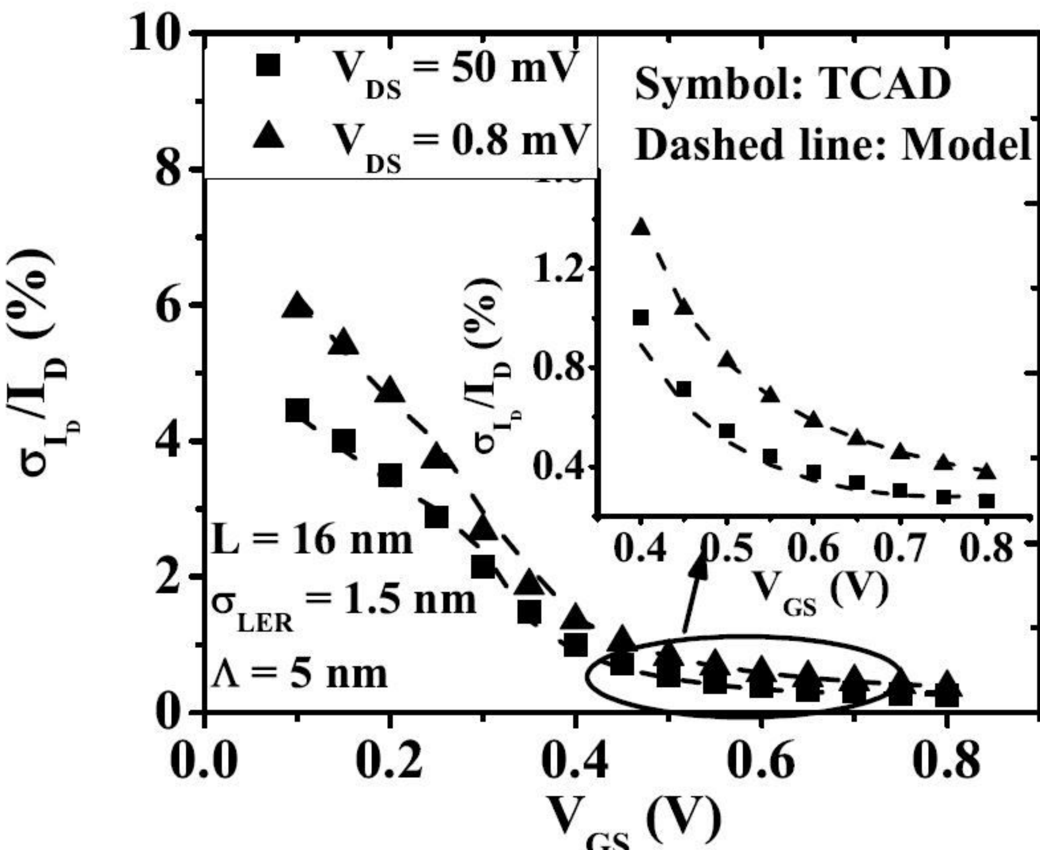

Figure 3

Variation of the normalized drain current variability with VGS for L = 16 nm at low and high drain biases.

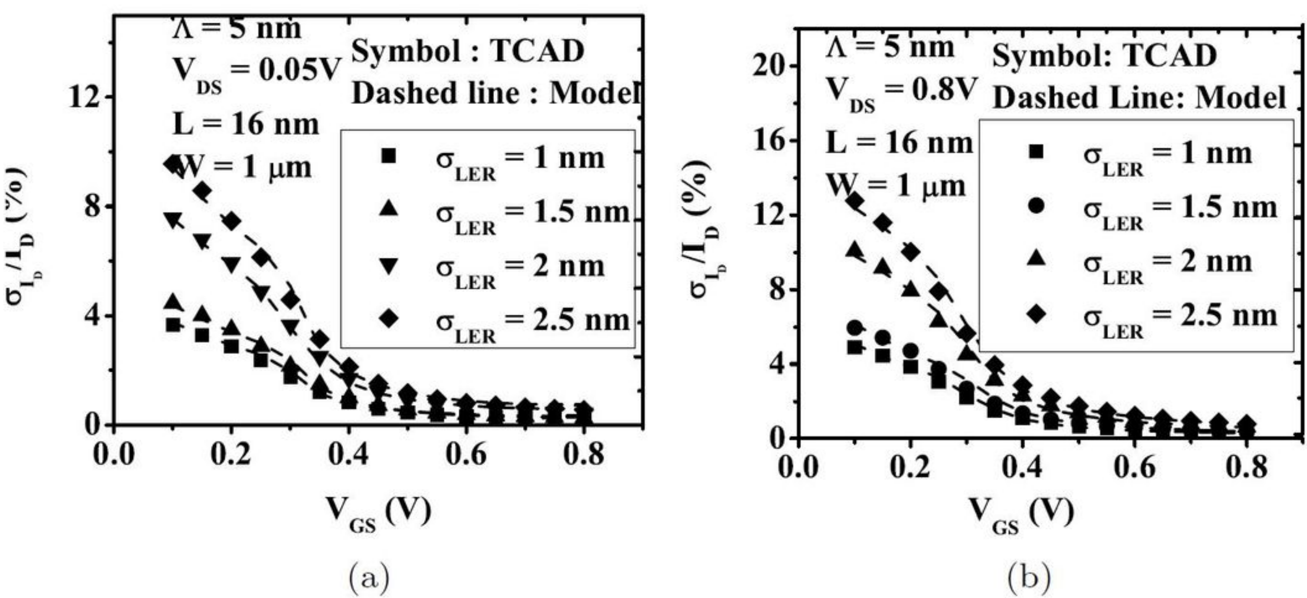

Figure 4

Variation of normalized drain current variability with applied gate bias for various edge roughness amplitude at L = 16nm at (a) Low VDS and (b) High VDS.

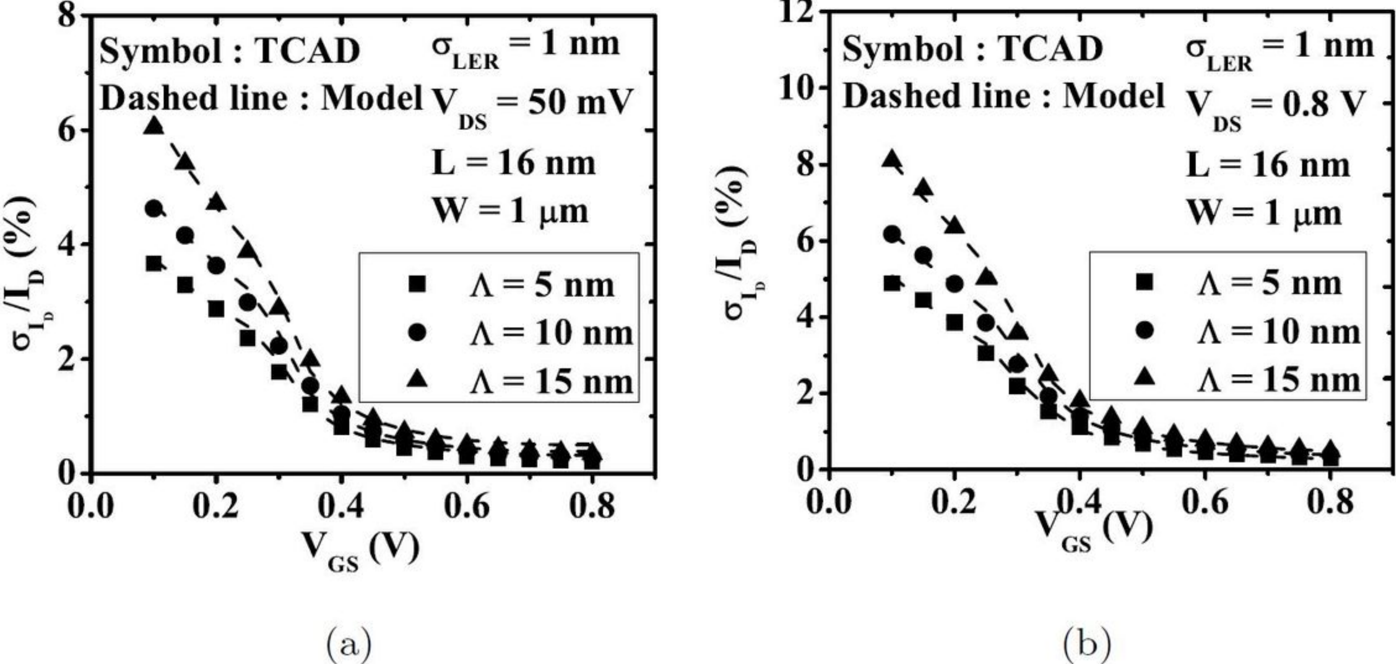

Figure 5

Variation of normalized drain current variability with applied gate bias for various correlation lengths at L = 16nm at (a) Low VDS and (b) High VDS.

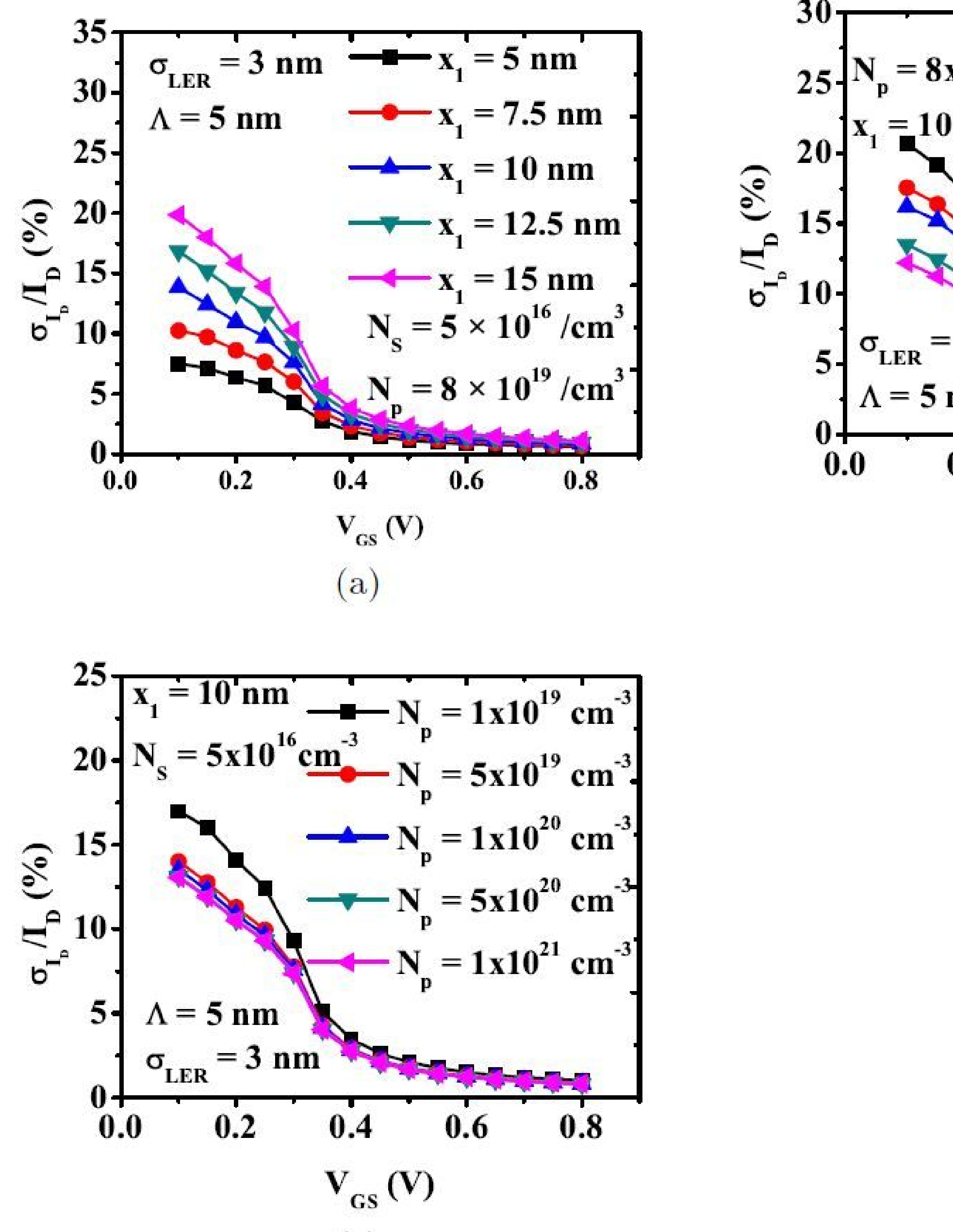

Figure 6

Effect of channel profile parameters on normalized drain current variability for different values of (a) x1, (b) Ns and (c) Np

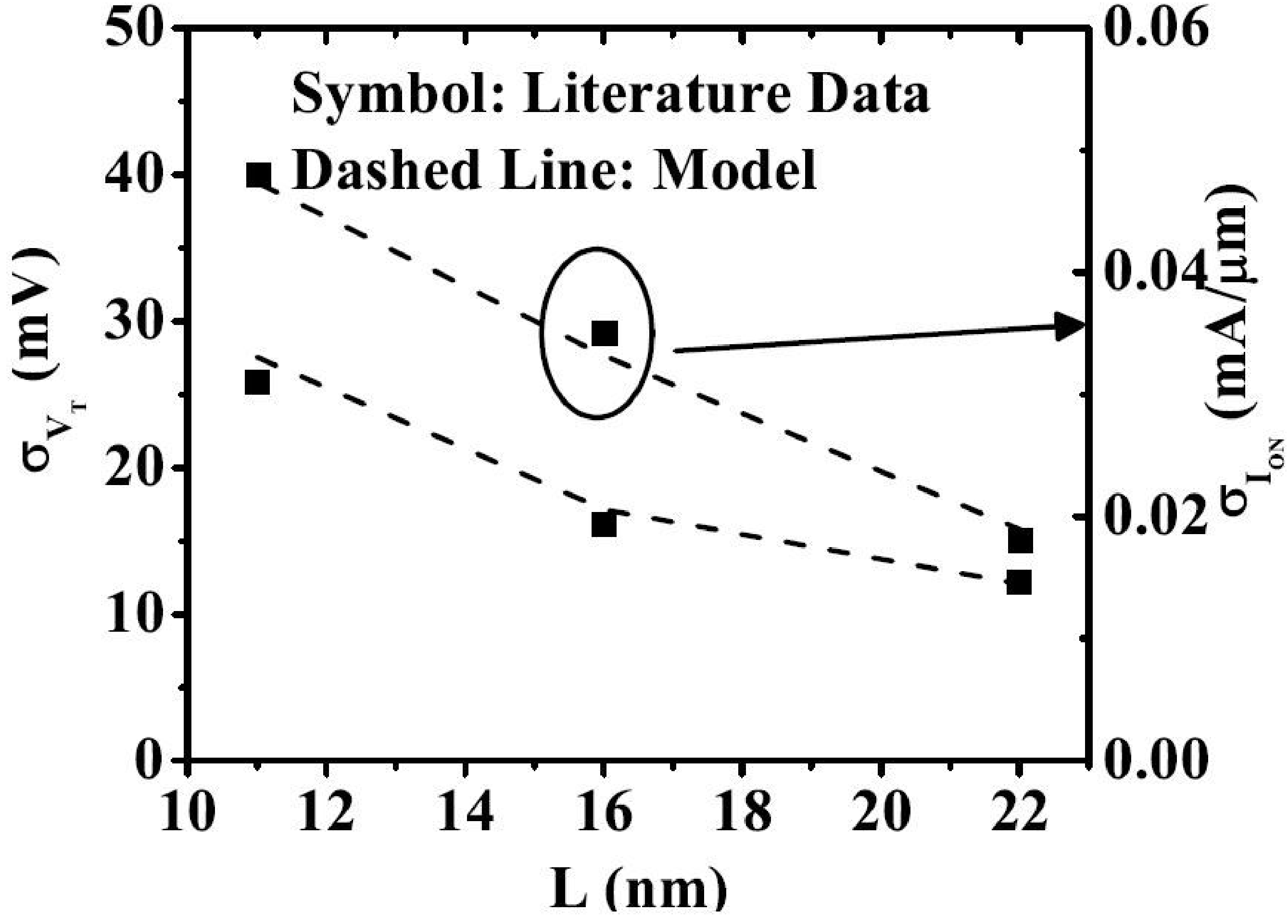

Figure 7

Verification of the model predicted local ON-current variability result due to LER with atomistic simulation results for a UTB-FD-SOI MOSFET [32].