Impact of the geometric parameters on the performance of silicon TG SOI N FinFET 5nm

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Impact of the geometric parameters on the performance of silicon TG SOI N FinFET 5nm

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Abstract. Semiconductor device dimensions have been downsized to nanoscale dimensions to upgrade the driving capacity and increasing speed. At the lower technology node, the performance of conventional CMOS circuits degrades because of the short channel effects (SCEs). the researchers expect to identify new solutions for different design issues as a result, the FinFET device has been introduced as an alternative to MOSFET for advanced scalability which allows the use of multi gates in order to dissipate lower power.
This paper presents an analysis of TG N SOI (Semiconductor On insulator) FinFET 5 nm using Hafnium Dioxide and the Non-Equilibrium Green Function (NEGF) formalism to study the quantum effect. The different parameters such as leakage current, the ON current, the performance ratio I_{ON}/I_{OFF} which are calculated and optimized. The aim and the novelty of this simulation is to present novel geometric parameters that improve the performance of the device, and hence to have optimized CMOS circuits.
Keywords: FinFET, CMOS, Quantum effect, Leakage current.

1. Introduction

Advancement in the semiconductor industry has transformed modern society with the availability of high-performance IC (Integrated Circuit) devices for faster communication system. The Miniaturization of silicon MOSFET transistor is continuing fifty years later after the Gordon Moore produced his famous rule. The scaling of MOSFET has reached its limits due to the increase in leakage current I_{OFF} and the threshold voltage V_{TH}. However, current challenges in MOSFET are expected to change the device design for the 5-nm node and beyond technologies.
The gate oxide thickness has been reduced, unfortunately, this leads to a high leakage current I_{OFF} due the quantum tunneling effect and the continuous use of low dielectric SiO_2 generate a high leakage current.
To counter this effect, the industry uses a new material with the high-k gate dielectrics constants. Various alternative devices have emerged to overcome these issues and the FinFET device is the one mostly studied recent years due to its improvement of the performance of integrated circuits [3].
FinFET offers the best electrostatic control of the channel for different configuration such as the Tri-gate, pi gate FinFET and Gate All Around GAA FinFET.
N.P. Maity et *al* in 2017 [25] have explored the application of the promising high-k dielectric material HfO_2 on MOS devices. They observed that the tunneling current is inversely proportional to the dielectric constant of the oxide material.
Bourahla et *al* [30] have demonstrated that the Ta_2O_5 material of gate with high permittivity (k = 27) turns out better values for performance parameters such as (V_{TH}, SS, I_{ON}, I_{OFF} current and I_{ON}/I_{OFF} ratio current, g_m, and electrical field (E)) in comparison with other dielectrics such as SiO_2, SnO_2, ZrO_2 which improve the performance of the device.
Lazzaz et *al* [1] have demonstrated the impact of the metal gate work function on the

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performance of the DG FinFET 10 nm with SILVACO TCAD tools.
Lazzaz et *al* [26] have simulated a theoretical model based on the Bohm Quantum Potential (BQP) theory and compared it with experimental data. The theory fits with the experiment after optimization and correction using the right values of the geometric parameters.
Sanghamitra Das et *al* in 2021 [27] have studied the effect of FinFET geometry parameters (channel length and fin height) on the RF figures of merit by using TCAD simulations. Their results confirm that decreasing the channel length or increasing the fin height improves the RF parameters.
Mostak Ahmed et *al* in 2021 [28] have simulated the electrical characteristics of a 3-D silicon on insulator (SOI) triple gate (TG) n FinFET with a channel length of 5 nm using different gate dielectric materials. The results of their simulation confirm that the high k dielectric materials have a better option in the fabrication of TG FinFET device.
Unopa Matebesi et *al* in 2021 [29] have studied the IGZO FinFET characteristics and then compared with ZnO FinFET and the Si FinFET. The results of their simulation confirm that IGZO has a large performance than of Si device by two orders of magnitude.
Asharani Sama et *al* [31] have demonstrated the effect of symmetric and asymmetric variation of underlap regions both on source and drain side of 3D SOI n-FinFET. The results of the simulation show that the underlap length is a crucial parameter for the performance of the device. The simulation result shows that L_{ud} variation has greater effect on I_{ON}/ I_{OFF} as compared to L_{us} and L_{un} variation, however, the latter two variations have similar effect on the switching ratio.
Qamar-ud-din Memon et *al* [32] have presented a technique to predict the I-V characteristics of TG Si FinFET using NEGF method. The results of this simulation demonstrate that the proposed model has the ability to predict FinFETs characteristics having T_{fin}=3-35 nm.
So, the above literature survey indicates the importance of using high-k dielectrics in FinFET devices and the importance of the underlap length which can be used to reduce the short-channel effects.
This paper is divided into four different sections: Section I is the introduction, section II: the device structure, section III: 3.the physical model used in this simulation, IV: the effect of geometric parameters and finally a conclusion.

2. Device structure

Tri Gate (TG) FinFET technology is based on the vertical Fin represented by the Fin length (L), oxide thickness (t_{ox}) and Fin width (W_{fin}) as show in the figure 1, the dioxide used in this simulation is the HfO_2 with dielectric constant of 24.
Figure 1 illustrates the horizontal cross section along transistor gate.

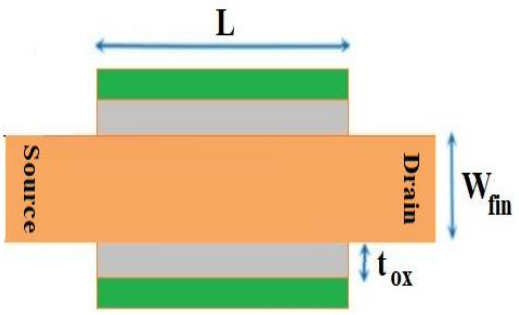

Fig. 1. horizontal cross-section along transistor gate [1]

A numerical device simulator has been used to simulate the structure of the proposed TG N FinFET 5 nm, it consists of two steps: i) The structure creation which includes the setting of the different geometric parameters and ii) the Doping concentration and the numerical solution that includes the choice of the physical model which uses the method of the Non-Equilibrium Green Function (NEGF).

Table 1 represents the different geometric parameters used in this simulation [17]:

Parameter	Channel Length L	Gate Length L_G	Oxide thickness: t_{ox}	Fin Height H_{fin}	Fin Width W_{fin}	Supply Voltage: V_{dd}
Value	5 nm	14 nm	2 nm	20 nm	20 nm	0.8 V

Table 1.

To overcome the undesirable effect of the miniaturization in a Nano transistor such as Short Channel Effect (SCE). The development of the silicon FinFET has been one of the most important creations in recent Ultra Large-Scale Integration (ULSI) technology as it improves the gate controllability.

Figure 2 illustrate the different geometric parameters of TG FinFET 5 nm. Unilateral length L_{UL} is the regions between the source/drain extensions and the region covered by the gate electrode.

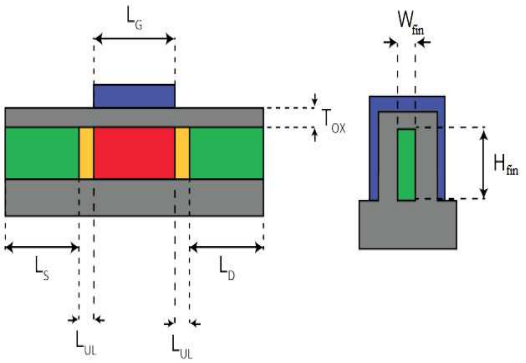

Fig. 2. Different geometric parameters of TG N FinFET 5 nm

3. Physical model used in this simulation

In FinFET devices, quantum effects have a large impact on their performance therefore, the simulation and modeling of quantum transport is important for many reasons like the tunneling current through ultra-thin gate oxide and the increase of threshold voltage.

As the channel length is reduced, the quantum effects along the channel, such as the tunneling through the source/drain (S/D) barrier becomes non-negligible therefore, 3 D quantum mechanical mode is preferred.

The NEGF function provides conceptual basis to solve the Schrodinger equation with open boundary conditions (BC).

The Poisson equation is solved to have the electrostatic potential in the channel and it is represented in the following equation [35]:

$$\frac{d^2\Phi(x,y,z)}{dx^2} + \frac{d^2\Phi(x,y,z)}{dy^2} + \frac{d^2\Phi(x,y,z)}{dz^2} = \frac{qn(x,y,z)}{\varepsilon_{Si}} \qquad (1)$$

Φ: Electrostatic potential; q: electron charge; ε_{Si}: silicon permittivity, n(x,y,z) :electron density.

The Schrödinger equation is a linear partial differential equation that governs the wave function of a quantum-mechanical system. It is a key result in quantum mechanics and it is represented by the following equation:

$$E\Psi = H\Psi \qquad (2)$$

E: energy; **Ψ**: wave function.

Figure 3 represents the parameters used in the Non-Equilibrium Green Function (NEGF) formalism such as, $\Sigma_{1,2}$is self-energy matrices.

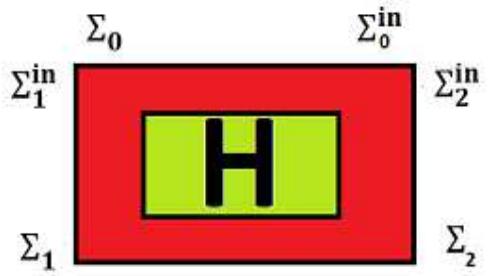

Fig. 3. NEGF parameters of Green's function

After introducing the scattering effect, we found a novel Schrodinger equation represented as the follow [34]:

$$\mathbf{E}\{\Psi\} = [\mathbf{H}]\Psi + |\Sigma|\{\Psi\} + \{\mathbf{s}\} \qquad \mathbf{(3)}$$

:H: Hamiltonian matrix whose eigenvalues represent the allowed energy levels and describe the quasiparticle dynamics around the equilibrium state, Σ : self-energy and it illustrate the disturbance from the open boundary conditions, it is included as part of the system Hamiltonian. $|\Sigma|\{\Psi\}$ **and** $\{\mathbf{s}\}$ represent the out flow and inflow respectively.

Using this modified Schrodinger, the wave function can be represented by the following equation:

$$\{\Psi\} = [\boldsymbol{EI} - \boldsymbol{H} - \Sigma]^{-1}\{\boldsymbol{s}\} \qquad \mathbf{(4)}$$

I: is an identity matrix of the same size as the rest.

In order to remove the coherent in the source and to suppose multiple source, we define the following products as [8][16]:

$$\boldsymbol{G^R} = [\boldsymbol{EI} - \boldsymbol{H} - \Sigma]^{-1} \qquad \mathbf{(5)}$$

$$\boldsymbol{G^A} = [\boldsymbol{G^R}]^{+} \qquad \mathbf{(6)}$$

Therefore, we can write the wave function by the following equation:

$$\{\Psi\} = [\boldsymbol{G^R}]\{\boldsymbol{s}\} \qquad \mathbf{(7)}$$

So, we can define the NEGF equations as follows:

$$\{\Psi\}\{\Psi\}^{+} = [\boldsymbol{G^R}]\{\boldsymbol{s}\}\{\boldsymbol{s}\}^{+}[\boldsymbol{G^A}] \qquad \mathbf{(8)}$$

$$\boldsymbol{G^n} = \boldsymbol{G^R}\Sigma^{\boldsymbol{in}}\boldsymbol{G^A} \qquad \mathbf{(9)}$$

$\Sigma^{\boldsymbol{in}}$: in-scattering function.

The current equation of FinFET structure using NEGF formalism can be represented by the following equation:

$$\boldsymbol{I^{op}} = \frac{\Sigma \boldsymbol{G^n} - \boldsymbol{G^n}\Sigma^{+}}{\boldsymbol{i}\hbar} + \frac{\Sigma^{\boldsymbol{in}}\boldsymbol{G^A} - \boldsymbol{G^R}\Sigma^{\boldsymbol{in}}}{\boldsymbol{i}\hbar} \qquad \mathbf{(10)}$$

ħ: plank constant.

The threshold voltage V_{TH} is a very important parameter for obtaining the ON current. The threshold voltage is represented by the following equation [9][1]:

$$\boldsymbol{V_{TH}} = \boldsymbol{\Phi_{ms}} + \mathbf{2}\boldsymbol{\Phi_F} + \frac{\boldsymbol{Q_D}}{\boldsymbol{C_{OX}}} + \frac{\boldsymbol{Q_{SS}}}{\boldsymbol{C_{OX}}} + \boldsymbol{V_{in}} \qquad \mathbf{(11)}$$

Q_{SS}: Charge in the gate dielectric, C_{OX}: gate capacitance, Q_D: depletion charge, Φ_F : fermi potential with respect to the conduction band minimum ,V_{in} : input voltage.

The Fermi potential for N type silicon is [12]:

$$\boldsymbol{\Phi_F} = \left(\frac{\boldsymbol{k_B T}}{\boldsymbol{q}}\right)\mathbf{ln}\left(\frac{\boldsymbol{N_A n}}{\boldsymbol{n_i}}\right) \qquad \mathbf{(12)}$$

k_B : Boltzmann constant, T: temperature ,N_A : Donor concentration ;n_i :intrinsic carrier concentration, n : minority electrons concentration.

The subthreshold slope (SS) is a major parameter to calculate the leakage current and is calculated as [11][12]:

$$\boldsymbol{SS} = \frac{\boldsymbol{dV_{GS}}}{\mathbf{d}(\mathbf{log}_{\mathbf{10}}\boldsymbol{I_{DS}})} \qquad \mathbf{(13)}$$

The value of the Drain Induced Barrier Lowering (DIBL) is calculated by the following relation

[2]:

$$\mathbf{DIBL} = \frac{\mathbf{dV_{TH}}}{\mathbf{dV_{DS}}} \qquad \mathbf{(14)}$$

4. Results:

4.1 Device simulation

Figure 4 represents the output characteristics of FinFET 5 nm, the drain current is swept from 0 to 0.8 V. We note that the drain current saturation I_{DSAT} of this simulation is $2.1x10^{-4}$A when V_{DS}=0.8 V and V_{GS}=1V. The choice of V_{DD}=0.8 V is extracted from Predictive Technology Model (PTM-SPICE model).

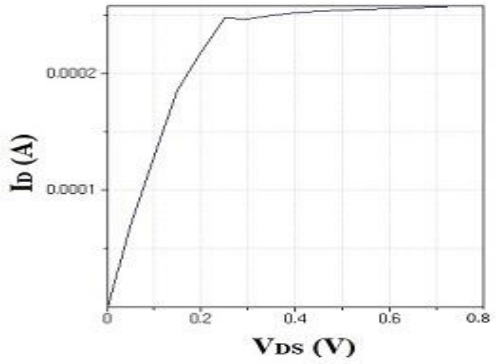

Fig .4 Output characteristics of N FinFET 5nm

Figure 5 represents the transfer characteristic of FinFET 5 nm, the gate voltage swept from 0 to 0.8V. The maximum value of drain current represents the ON current when V_{GS}= V_{DD}=0.8V and the value of the ON current is $4.25x10^{-4}$A. We note that the ON current increases due to the minimum strain effect [33].

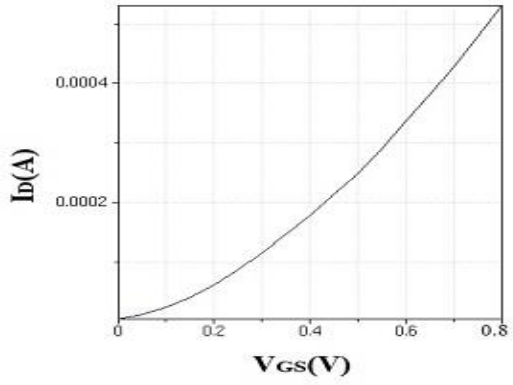

Fig 5. Transfer characteristics of N FinFET 5nm

The ON current obtained in this simulation is higher than the one calculated by Sreenivasulu et *al* [25] and Mahmood Uddin Mohammed et *al* [21].

Figure 6 represents the drain current with logarithm scale. The gate voltage is swept from 0 to 0.8V. We note that the leakage current is $5.47x10^{-6}$A when V_{GS}=0V.

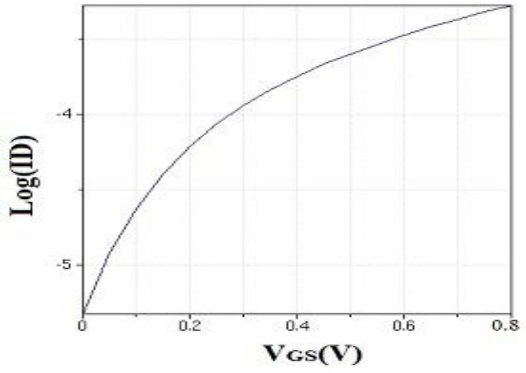

Fig 6. Log (I_D) of TG SOI N FinFET 5nm

Table 2 represents the calculated performance parameters of the device understudy [18][20]:

Table 2. Performance parameters of TG FinFET 5 nm

Parameters	I_{ON}	I_{OFF}	$I_{ON}N/I_{OFF}$	V_{TH}	SS
Values	$5.73x10^{-4}$A	$5.47x10^{-6}$A	104.75	0.25 V	186.85 mV/dec

Figure 7 represents the variation of transconductance of FinFET 5 nm, we note that the maximum value is $5.25x10^{-4}$ A/V.

The larger value of the transconductance can be explained by the higher strain in the short channel device, we can reduce the peak value of transconductance by the reduction of the channel length. Shorter gate length L_G provides less resistance and lower surface-roughness scattering which leads to a higher transconductance and mobility.

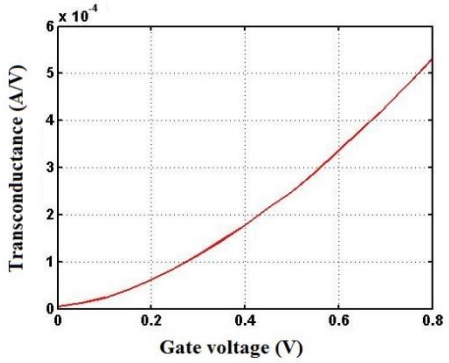

Fig 7. Transconductance of FinFET 5 nm

Figure 8 represents the gate capacitance of FinFET 5nm, we note that the maximum value of total gate capacitance is $8.5x10^{-14}$ F.

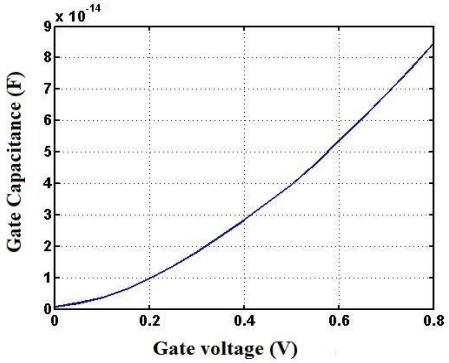

Fig 8. Gate capacitance variation of FinFET 5 nm

Various low static power technologies require higher threshold voltages but the miniaturization of the integrated circuits and the channel length reduces the threshold voltage [14].

The threshold voltage decreases with the reduction of channel length, but the opposite is observed for the subthreshold slope (SS) because the FinFET with 5 nm node technology is more immune to short Channel Effect (SCE)[6][19].

We note that the result obtain in this simulation for the performance ratio I_{ON}/I_{OFF} is higher than that calculated by Yu Ding et *al* [5] and the result of threshold voltage obtained is better than that calculated by Vinay Vashishtha [4].

According to the results obtained in the different characterizations, we note that the performance ratio must be more that 10^6 [10].In this simulation, we note that the performance ratio is less that 10^6 therefore, we need to optimize the different parameters to improve the performance of the device [10].

We think that the problem of the increase of leakage current is due to quantum confinement therefore,the choice of geometric parameters like the gate oxide length can lead to the raising of the conduction band, and hence, we need more potential to create an inversion layer [13][15].

We can control and minimize the leakage current by optimizing the geometric parameters like Fin height (H_{fin}), Fin width (W_{fin}) , gate oxide thickness (t_{ox}) ,Gate length (L_G) and Underlap length (L_{UL}). The next work is to study the effect of geometric parameters on the performance

of the device.

4.2 Impact of the Fin width

Figure 9 represents the effect of Fin width, we note that the increase of fin width increases the leakage current from 5.47µA to 11.5 µA because the direct tunneling current will be more important than the Trap Assisted Tunneling (TAT).

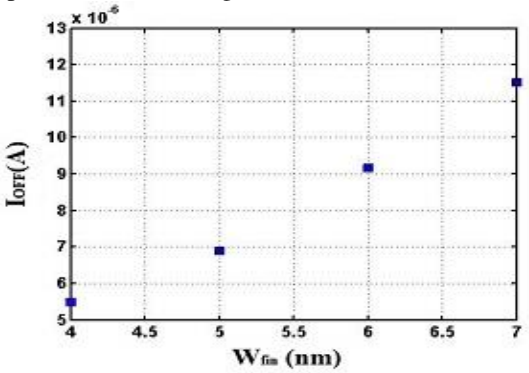

Fig 9. Effect of fin width variation on I_{OFF} current.

Figure 10 represents the effect of Fin width on the ON current, we note that the Fin width is swept from 4 nm to 7 nm. The ON current decreases at 5 nm due to strain effect.As the fin width is scaled from 7 nm to 4 nm, the ON current degrades due to the reduction of channel volume and the device with higher width has large transconductance and minium gate capacitance.

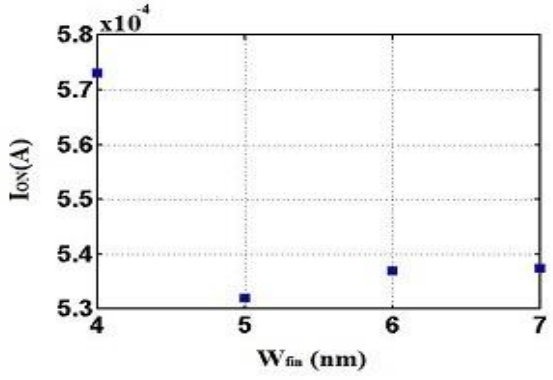

Fig 10. Effect of Fin width variation on I_{ON} current.

Leakage current I_{OFF} is the current at the gate voltage V_{GS}=0. The ON current is the maximum current at a gate voltage $V_{GS}=V_{DD}$.

Figure 11 represents the effect of Fin width on the performance ratio I_{ON}/I_{OFF}. We note that the increase of the fin width decreases the performance of the device due to the quantum confinement and the increase of the leakage current.

The optimal value of this simulation is W_{fin}=4 nm because it has the better performance ratio.

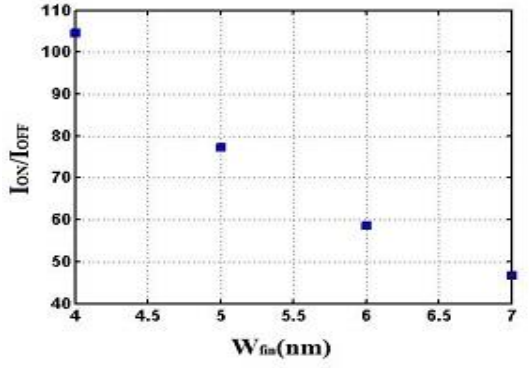

Fig 11. Effect of Fin width variation on I_{ON} current.

In short channel length, the leakage current becomes one of the most important parameters that requires more attention.

4.3 Impact of the Fin height

Figure 12 represents the effect of the Fin height on the leakage current. We note that the leakage current starts to decreases at H_{fin}=21 nm because the quantum effect decreases.
Non-equilibrium green function (NEGF) formalism demonstrates that the increase of Fin height increases the energy contact, so the leakage current increases with the high values of Fin height.

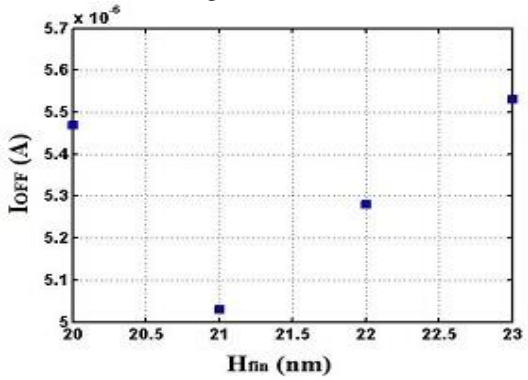

Fig 12. Fin height effect on leakage current.

FinFET has emerged as a promising candidate to replace conventional MOSFET in CMOS based digital circuits for low power consumption hence, optimizing the device is to maximize ON current.
Figure 13 represents the effect of Fin height on the ON current, we note that the ON current decreases at H_{fin} =21 nm because the strain effect are enhanced and parasitic resistance is reduced.
The device delivers much improved driving current and thereby enhances the transconductance of device.

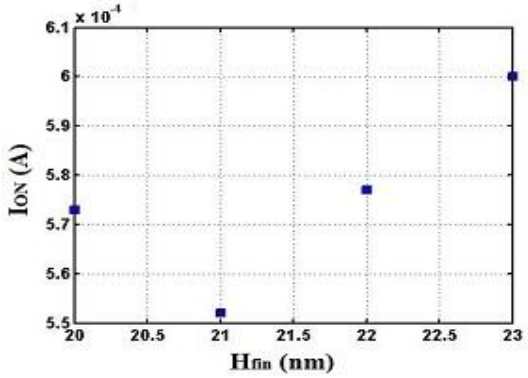

Fig.13: effect of Fin width variation on I_{ON} current

Figure 14 represents the effect of Fin height on the performance ratio. We note that the performance ratio starts to decrease due to the increase of the leakage current. The degradation of the performance ratio allows the increase the static power dissipation and switching time of CMOS circuits.
The optimal value is H_{fin}=21nm because it has a better performance ratio.

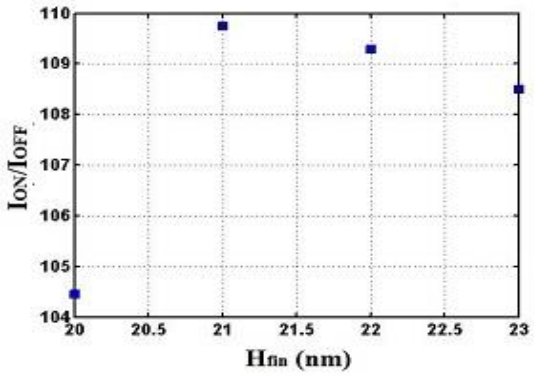

Figure.14: Height Fin effect on performance ratio

Quantum mechanical effects occur in FinFET devices at lower technology nodes and cannot be ignored. FinFET is developed with multi gates to overcome this issue and to minimize the leakage current and maximize the ON current.

The threshold voltage decreases because of: i) The increase of Fin width, ii) The increase of source/fin region. Consequently, the capacitance will be decreases and the surface potential coupling increases [22][24].

4.4 Impact of oxide thickness

We know that the device parameters have significant influences on the SCE and the device electrical characteristics.

Figure 15 illustrates the effects of gate oxide thickness on the ON current, the decrease of the ON current is due of strain effects.

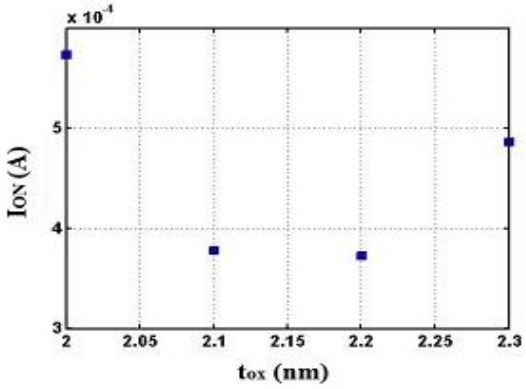

Figure.15: Height Fin effect on the ON current.

Figure 16 illustrates the oxide thickness effect on the performance ratio. We note that the performance ratio decreases at 2.2 nm due to the increase of the leakage current and quantum confinement. The optimal value of this simulation is t_{ox}=2.3 nm because it's has better ratio I_{ON}/I_{OFF} [23].

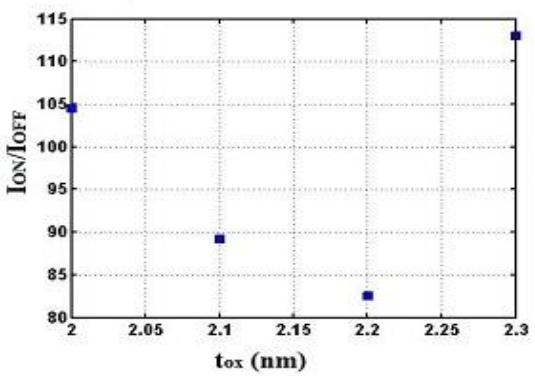

Fig.16: oxide thickness effect on performance ratio.

4.5 Impact of symmetric underlap lengths

Planar transistors have reached their limits due to undesirable problems. To overcome performance limitations of this structure, 3D like structure are used the geometry allows a higher contact between the gate and the dielectric material.

Figure 17 illustrates the impact variation of underlap length on the ON current, the underlap length is swept from 0 nm to 2.1 nm.

We note from this results that the ON current decreases due to the increase of the total resistance and strain effects.

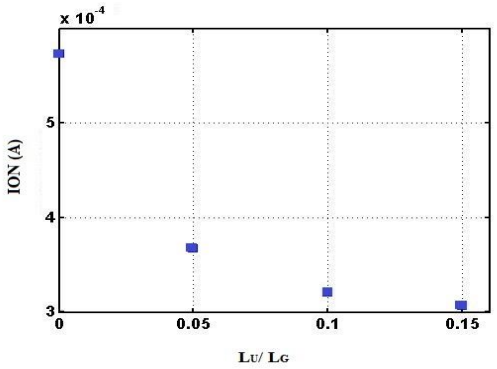

Fig.17: Impact of underlap length on the ON current.

Figure 18 illustrates the impact of the underlap length on the I_{OFF} current. The results of this simulation show that the leakage current decreases because of the larger tunneling current. When we increase the underlap length, the Trap Assisted Tunneling (TAT) will be larger than the direct current (DC).

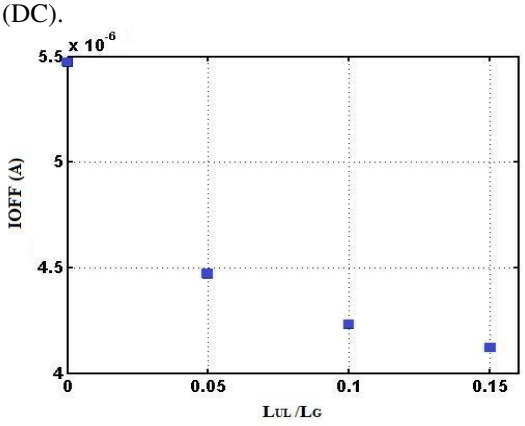

Fig.18: Impact of the underlap length on the OFF current.

Figure 19 represents the impact of the underlap length on the performance ratio I_{ON}/I_{OFF}. The ratio L_{UL}/L_G is swept from 0 to 0.15. We note from the results of this simulation that the performance of the device decreases when the underlap length increases. The optimal value of this simulation is L_{UN}=0 nm (No underlap).

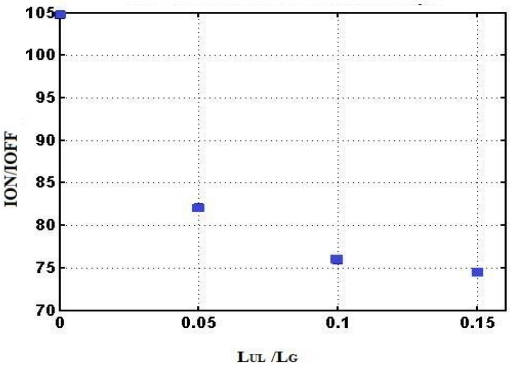

Fig.19: Impact of underlap length on the performance ratio ION/IOFF.

4.6 Impact of gate length (L_G)

Figure 20 illustrate the impact of the gate length on the ON current. As the gate length scales down from 16 nm to 15 nm, the ON current of the device tends to increase due to the increase of the electrostatic interaction of the gate over the channel and consequently the effective area of the channel is reduced.

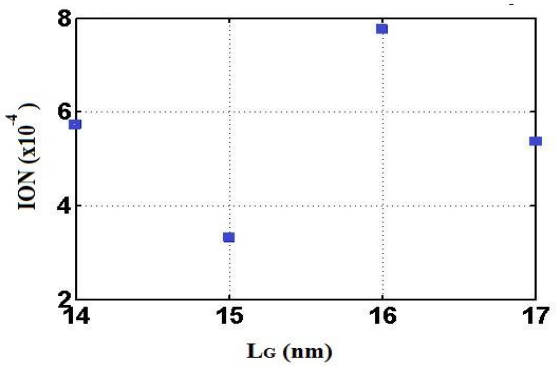

Fig.20: Impact of the gate length on the ON current.

Figure 21 illustrates the impact of the gate length on the leakage current. We note from the results of this simulation that increasing of gate length decreases the leakage current and decreases the tunneling current.

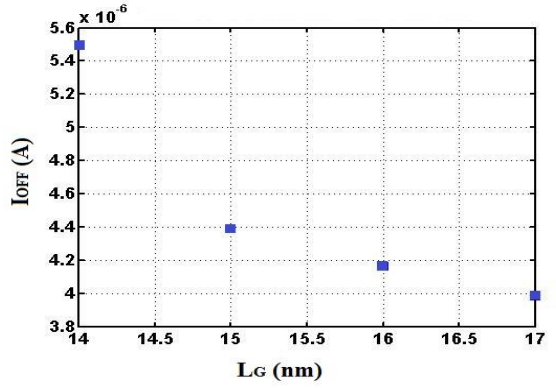

Fig.21: Impact of the gate length on the leakage current.

Figure 22 represents the impact of gate length on the performance ratio. We note that the fluctuations in the results are due to the ON current. The optimal value of gate length is 16 nm because it's has a higher performance ratio.

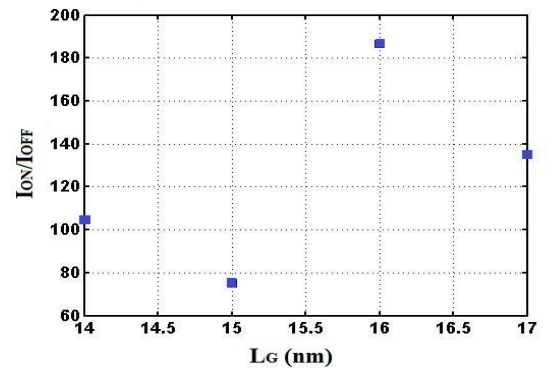

Fig.22: Impact of gate length on the performance ratio.

Conclusions

In this simulation, we have performed a quantum simulation of FinFET tri gate (TG) with 5nm node technology using Hafnium dioxide. The miniaturization of FinFET behind 10 nm node technology demonstrates that the performance and the characteristics of the device are

sensitively linked to the channel length scaling however, the results in this simulation confirm that the FinFET with NEGF formalism exhibits a good performance and overcomes the problems due to scaling. We confirm in this paper that Fin height with 21 nm, Fin width with 4 nm oxide thickness with 2.3 nm, gate length with 16 nm and no underlap length can reach a good performance ratio hoping that the studied device CMOS circuit exhibits a good VTC curve and higher switching speed.

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Conflict of Interest:
The authors declare that they have no conflict of interest.

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