Research Square

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A Novel Design of Low Power, Modified Pre-charge free Binary CAM Array with Pre-computation for Search-Intensive Applications

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Abstract

Memory is a storage space that is essential for storing the repetitive data and the instructions to perform an operation. In modern processors speed has been increased significantly but memory enhancements are mainly focusing on the ability to store more data in less space and to reduce the latency. Content Addressable Memory (CAM) cells are preferred over SRAM cells as they are faster and gives the address of the matched data whereas SRAM uses address to access particular data. The circuit of Modified Pre-charge free CAM cell proposed in this paper is made up of basic 6T SRAM cell (2 cross-coupled inverters and 2 access transistors) and separate comparison circuit (1 PMOS and 1 NMOS transistor). The 8X8 memory array consists of memory cells, row and column decoders, encoder, pre-charge circuits, sense amplifiers and write driver circuits. The various parameters like delay, dynamic power and power delay product are measured and compared with other CAM cells. CADENCE Virtuoso Tool is used for designing the various circuits in 90 nm technology. The simulation results demonstrate that the suggested CAM cell outperforms other cells, hence it is employed to create the array structure. The 8X8 CAM array based on MPF CAM cell has less power and less delay when compared with other array structures.

1. Introduction

Very Large Scale Integration (VLSI) is a method of fabricating integrated circuits (ICs) by packing millions of transistors onto a single silicon chip and this technology emerged in late 1970s. ICs are classified based on the number of transistors or gates used in a single chip into SSI, MSI, LSI and VLSI. CMOS are used in VLSI because of its low static power consumption and high immunity to noise. Before the development of VLSI technology, most ICs could only execute a restricted range of functions. VLSI allows IC designers to combine all the functions into a single chip. System on chip architecture is used in VLSI to design ICs. VLSI technology has made the devices handheld by minimizing the size of circuits since it takes up less space, improving operating speed, lowering power consumption, and reducing device cost. The number of transistors used in such devices is very high and it has made them work efficiently. Gordan Moore predicted that the number of transistors that can be integrated on a chip, doubles in every 1–2 years and it is called as Moore's law. This is possible by scaling down to various nm technology by reducing the size of components used. Nowadays IOT based devices are in the trend and they require long battery life without recharging and their memory should be fast.

Memory is the storage unit which stores the data that needs to be processed and also the instructions that should be followed for processing the data. Memory cell is the fundamental block of computer memory and it has unique address. Memory cells placed along the row and column constitute the memory array. Memory cells store one bit either 0 or 1. They are constructed using MOS transistors. Random Access Memory (RAM) is a short-term memory that stores the programs and data that the CPU is now using in real time. The data stored in the RAM may be read, written, and wiped indefinitely. RAM enables the CPU to retrieve data more rapidly and perform several tasks at once. By adding extra RAM, the CPU strain may be lowered. Modern CPUs have substantially boosted their speed, while memory improvements have mostly focused on the capacity to store more data in less space and lower latency.

Content addressable memory (CAM)[1] also known associative memory is a special kind of memory. CAM[6][7][23] is constructed using transistors, it is a volatile memory, it doesn't require regular refreshing to store the data. CAM consists of basic 6T SRAM cell (2 cross coupled inverters connected back-to- back, and 2 access transistors) and separate comparison circuit (extra transistors). The operations performed in a CAM [13][20] cell are write and compare. The comparison operation is done in a single cycle.[2] In SRAM address is given as input and the data stored in that particular address is obtained as output. But in a CAM [29][32][33] cell data is given as input and the address where it is stored is obtained as output. CAM [10][31][34] acts as a hardware for extremely fast search operations. It consists of a table of stored data and a specific search input data is given and it is compared with that to get the location of the matching data.[16] CAM is commonly used in networking devices to accelerate the operations in the routing table and also forwarding of information. In data search applications CAM [15] outperforms RAM. Data search words in a binary CAM [8][21][28] are made up of 1s and 0s whereas in a ternary CAM [9][19] [24] it consists of don't care (X) along with 1s and 0s. The various parameters that can be measured in a CAM cell are power, delay, power delay product and stability.

Power dissipation is classified into Dynamic Power, Static or Leakage Power and Short Circuit Power [26]. Delay is the time period at which input is given and when the output is obtained. It is the average of the rise and fall time. Power Delay Product or energy consumption of the cell is product of delay and dynamic power consumption. The Static Noise Margin (SNM) is used to determine the cell's stability; the larger the SNM, the more stable the cell. The noise margin is computed by first drawing a butterfly curve for the inverters that are coupled back-to-back, then calculating the diagonal of the largest square that can fit inside.

The paper is structured as follows: The different CAM cells that exists are discussed in section 2. In Section 3 the details of the new proposed cell and memory array structure for proposed CAM cell is given. Then Section 4 covers the simulation results and comparison of various performance parameters. Finally, Section 5 gives summary and conclusion of this work.

2. Existing Methodologies Of Cam Cell

2.1 NOR CAM CELL

NOR CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. NOR CAM cell uses ten MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 4 NMOS transistors (N5, N6, N7, N8) form the comparison circuit. NOR CAM cell has parallel discharge path in the comparison circuit. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The NOR CAM cell with pre-charge circuit illustrated in Fig. 1 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. Pre-charge circuit consists of 1 more PMOS transistor with its gate connected to control input CTRL, source connected to VDD and drain connected to ML. It requires pre-charging circuit to pre-charge ML[17]. During write operation WL is

enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare operation, the info in CAM is evaluated to the search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are identical, match condition occurs and if the stored info and search info are different mismatch condition occurs. ML is pre-charged to VDD. During match state, ML remains at VDD and during mismatch state, ML discharges to GND. WL is disabled during comparison operation.

2.2 NAND CAM CELL

NAND CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. NAND CAM cell uses nine MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 3 NMOS transistors (N5, N6, N7) form the comparison circuit. NAND CAM cell has series discharge path in the comparison circuit. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The NAND CAM cell with pre-charge circuit illustrated in Fig. 2 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. MLn is connected to previous CAM cell and MLn + 1 is connected to the next CAM cell. Pre-charge circuit consists of 1 more PMOS transistor with its gate connected to control input CTRL, source connected to VDD and drain connected to ML. It requires pre-charging circuit to pre-charge ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare operation, the info in CAM is evaluated to the search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are identical, match condition occurs and if the stored info and search info are different mismatch condition occurs. ML is pre-charged to VDD. During match state, ML discharges to GND and during mismatch state, ML remains at VDD. WL is disabled during comparison operation.

2.3 XOR CAM CELL

XOR CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. XOR CAM cell uses eight MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 2 PMOS transistors (P3, P4) form the comparison circuit. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The XOR CAM cell circuit illustrated in Fig. 3 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. It doesn't require pre-charging of ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info During compare operation, the info in CAM is evaluated to search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match condition occurs and if the stored info and search info are different mismatch condition occurs. During match state, ML remains low and during mismatch state, ML goes high. WL is disabled during comparison operation.

2.4 XNOR CAM CELL

XNOR CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. XNOR CAM cell uses eight MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 2 PMOS transistors (P3, P4) form the comparison circuit. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The XNOR CAM cell circuit illustrated in Fig. 4 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. It doesn't require pre-charging of ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info During compare operation, the info in CAM is evaluated to search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match condition occurs and if the stored info and search info are different mismatch condition occurs. During match state, ML goes high and during mismatch state, ML remains low. WL is disabled during comparison operation.

2.5 PF CAM CELL

Pre-charge free (PF)[4][14][18] CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. PF CAM cell uses ten MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 2 NMOS transistors (N5, N6) form the comparison circuit. The PMOS transistor P3 and the NMOS transistor N7 form the charge control circuit and controls the output ML based on charge on node S and control bit (CB) for match and mismatch case. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The PF CAM cell circuit illustrated in Fig. 5 has inputs BL, BLB, WL, SL, SLB, CB and outputs Q, QB, ML. It doesn't require pre-charging of ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare or search operation, the info stored in CAM is compared with the search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match condition occurs and if the stored info and search info are different mismatch condition occurs. During match state, ML goes high and during mismatch state, ML remains low. WL is disabled during comparison operation.

CB is used to reset the ML for two consecutive search operation. Before search operation, CB is made high, which makes pull-up transistor P3 OFF and pull-down transistor N7 ON and drains ML regardless of stored and search input word. During the search operation, CB is made low, which makes pull-up transistor P3 ON and the pull-down transistor N7 OFF and value at node S comes to ML through P3. If there is a match, node S has high value and ML is charged to 1 through P3 transistor. If there is a mismatch, node S has low value and ML is discharged to 0 through P3 transistor.

2.6 SCPF CAM CELL

Self-controlled pre-charge free (SCPF)[11][30] CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. SCPF CAM cell uses ten MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 2 NMOS transistors (N5, N6) form the comparison circuit. The PMOS transistor P3 and the NMOS transistor N7 form the charge control circuit and controls the output ML based on charge on node S for match and mismatch case. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The SCPF CAM cell circuit illustrated in Fig. 6 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. It doesn't require pre-charging of ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare or search operation, the info stored in CAM is compared with the search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match condition occurs and if the stored info and search info are different mismatch condition occurs. During match state, ML goes high and during mismatch state, ML remains low. WL is disabled during comparison operation. If a match is found, node S has high value and allows ML to charge through N7 transistor. If there is a mismatch, node S has low value and makes ML discharge through P3 transistor.

The existing CAM cells are made up of 6T SRAM with additional transistors in the comparison circuit. The count of transistors in the existing methods is high and consumes more power and has high delay. PF CAM overcomes the short circuit path, charge-sharing problem and minimizes the overall power. But there is delay because of cascading of CB. SCPF has high power but has better delay when compared to PF CAM. Among the existing methods SCPF CAM Cell is more efficient. New designs of CAM structures can be made by combining CAM cells of single bit to form a word of particular length and reducing the count of transistors in charge control circuit. The following chapter discusses about the more efficient method than the existing methods.

3. Proposed Method

3.1 MPF CAM CELL

Modified pre-charge free (MPF) CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. MPF CAM cell uses ten MOSFETs, in that 2 NMOS act as access transistors (N3, N4). The cell can be accessed using these transistors. The 2 NMOS transistors (N5, N6) form the comparison circuit. The PMOS transistor P3 and the NMOS transistor N7 form the charge control circuit and controls the output ML based on charge on node S for match and mismatch case. The other 4 transistors (P1, P2, N1, N2) form the cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2). Cross coupled inverters constitute the storage unit of the CAM cell. The MPF CAM cell circuit illustrated in Fig. 7 has inputs BL, BLB, WL, SL, SLB and outputs Q, QB, ML. Tool View of MPF CAM Cell is given by Fig. 8. It doesn't require pre-charging of ML. During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare or search

operation, the info stored in CAM is evaluated to the search input data SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match state occurs and if the stored info and search info are contrasting mismatch condition occurs. During match state, ML goes high and during mismatch state, ML remains low. WL is disabled during comparison operation. If there is a match, node S has low value and ML is charged to 1 through P3 transistor. If there is a mismatch, node S has high value and ML is discharged to 0 through N7 transistor.

3.2 MHSCPF CAM CELL

Modified hybrid self-controlled pre-charge free (MHSCPF)[25] CAM cell consists of the basic 6T SRAM cell and along with that separate comparison circuit. MHSCPF CAM cell uses twenty-seven MOSFETs, in that 6 NMOS act as access transistors (N3, N4, N11, N12, N17, N18). Each SRAM cell has two access transistors. The cell can be accessed using these transistors. The 6 NMOS transistors (N5, N6, N13, N14, N19, N20) form the comparison circuit. The PMOS transistor P3, NMOS transistor N7, N8 are used for charge controlling circuit. The other 12 transistors (P1, P2, N1, N2, P4, P5, N9, N10, P6, P7, N15, N16) form the 3 cross coupled inverters. 1 NMOS and 1 PMOS form an inverter (P1, N1 and P2, N2 and P4, N9 and P5, N10 and P6, N15 and P7, N16). Cross coupled inverters constitute the storage unit of the CAM cell. The MHSCPF CAM cell circuit illustrated in Fig. 9 has inputs BL1, BLB1, SL1, SLB1, BL2, BLB2, SL2, SLB2, BL3, BLB3, SL3, SLB3, WL and outputs Q1, QB1, Q2, QB2, Q3, QB3, ML. Tool View of MHSCPF CAM Cell is given by Fig. 10. It doesn't require pre-charging of ML.

During write operation WL is enabled, data to be written is given for BL and its complement for BLB. Then the CAM cell stores the info. During compare or search operation, the info stored in CAM is evaluated to search input info SL and SLB. There are two states of output for the comparison operation. They are match and mismatch. When both the stored info and search info are same, match state occurs and if the stored info and search info are contrasting mismatch condition occurs. During match state, ML goes high and during mismatch state, ML remains low. WL is disabled during comparison operation. Node S3 is connected to the gates of transistors N7, N8 and P3. Node S2 is linked to source of transistor N8. Node S1 is linked to source of transistor N7. ML output is controlled by charge at node S1,S2 and S3 for high or low in the charge control circuit. In all the three CAM cells if the search info and stored info are matched then charge at nodes S1, S2 and S3 becomes high and charge ML through N7 and N8 transistor. If in any of the CAM cells the search data and stored data are mismatched then ML becomes 0. CAM word is formed using three CAM cells.[12]

3.3 PRE-COMPUTATION IN CAM

Parameter Extractors are used to perform pre-computation[3][22] in CAM cells by reducing operation time and power. In pre-computation method a particular feature is extracted from the input data and is compared with stored data which has the same feature, instead searching the entire memory and wasting power and increasing the delay. The various methods like Bit counting (counting number of 1s), Block XOR, Gate Block Selection, Parity bit extractor, Reminder function parameter extractor can be used.

3.4 STRUCTURE OF MEMORY ARRAY

CAM cells, sense amplifiers, decoders, encoder, write drivers and pre-charge circuits make up a memory array[5]. Decoders are used for accessing a particular CAM cell in the array and are placed along row as well as column. Sense amplifier is used for amplifying the data stored. Pre-charge circuit is used to charge ML to VDD during the compare operation. Encoder is used to give the address of the matched word as output for a particular search word. 8X8 Memory array shown in Fig. 11 is constructed using CAM cells.

The proposed CAM cells are 1-bit Modified Pre-charge free CAM and 3-bit Modified Hybrid Self-Controlled Pre-charge free CAM. The MPF CAM cell produces full swing output voltage and delay in the critical path is diminished. Leakage current is minimised; hence the power is saved. During mismatch ML is discharged completely which saves power. Removal of pre-charge circuits make CAM efficient during search operation. In the MHSCPF CAM cell 3 individual CAM cells are combined together to form a word and they have a common comparison circuit with 3 transistors. The transistor count is reduced in MHSCPF CAM because if individual CAMs are used, they have separate comparison circuit with 2 transistors for each. This reduces the power as well as delay significantly. Pre-computation can be done to improve the performance of CAM. Array structure can be developed using CAM cell, encoder, decoders, sense amplifiers and pre- charge circuits.

4. Results And Discussion

This gives the simulation[27] waveforms and results of different CAM cells and memory array. For numerous CAM cells and memory, parameters such as dynamic power, static noise margin, delay, and power delay product are measured. CADENCE Virtuoso tool is used for designing the various circuits in 90 nm technology. Cadence Design System's Spectre simulator is used to model the designs. All simulations are run at 27 degrees Celsius.

4.1 SIMULATION RESULTS OF CAM CELLS

The waveforms for various CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF, MPF and MHSCPF are given below. based PPN, PNN and KLECTOR based PPN, PNN are given below. Output waveform in Figure 12 displays the result of NOR CAM cell for ML when WL is disabled. In NOR CAM cell, match case has high value and mismatch case has low value. The input BL is 0100110011, BLB is 1011001100, SL is 0111000111, SLB is 1000111000 and the output ML is 1100001011.

Output waveform in Figure 13 displays the result of NAND CAM cell for ML when WL is disabled. In NAND CAM cell, match case has low value and mismatch case has high value. The input BL is 1100010011, BLB is 0011101100, SL is 1011010001, SLB is 0100101110 and the output ML is 0111000010. Output waveform in Figure 14 displays the result of XOR CAM cell for ML when WL is disabled. In XOR CAM cell, match case has low value and mismatch case has high value. The input BL is 0100110011, BLB is 1011001100, SL is 0111000111, SLB is 1000111000 and the output ML is 0011110100. Output

waveform in Figure 15 displays the result of XNOR CAM cell for ML when WL is disabled. In XNOR CAM cell, match case has high value and mismatch case has low value. The input BL is 1100010011, BLB is 0011101100, SL is 1011010001, SLB is 0100101110 and the output ML is 1000111101.

Output waveform in Figure 16 displays the result of PF CAM cell for ML when WL is disabled. In PF CAM cell, match case has high value and mismatch case has low value. The input BL is 0100110011, BLB is 1011001100, SL is 0111000111, SLB is 1000111000 and the output ML is 1100001011. Output waveform in Figure 17 displays the result of SCPF CAM cell for ML when WL is disabled. In SCPF CAM cell, match case has high value and mismatch case has low value. The input BL is 1100010011, BLB is 0011101100, SL is 1011010001, SLB is 0100101110 and the output ML is 1000111101.

Output waveform in Figure 18 displays the result of MPF CAM cell for ML when WL is disabled. In HSCPF CAM cell, match case has high value and mismatch case has low value. The input BL is 1100010011, BLB is 0011101100, SL is 1011010001, SLB is 0100101110 and the output ML is 1000111101. Output waveform in Figure 19 displays the result of MHSCPF CAM cell for ML when WL is disabled. In MHSCPF CAM cell, match case has high value and mismatch case has low value. The input BL1 is 0100100011, BLB1 is 1011011100, SL1 is 0101001000, SLB1 is 1010110111, BL2 is 1110010110, BLB2 is 0001101001, SL2 is 1011010110, SLB2 is 0100101001, BL3 is 0100101001, BLB3 is 1011010110, SL3 is 0101001011, SLB3 is 1010110100 and the output ML is 1010010100.

4.2 LAYOUT OF CAM CELLS

Layout Diagram of different CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF and MPF are given in the Figures 20, 21, 22, 23, 24, 25 and 26 respectively.

4.3 DYNAMIC POWER

Dynamic power is the amount of power utilised by the CAM cell during write or compare operation. Table 1 shows Dynamic Power in μW for different CAM cells of 1 bit like NOR, NAND, XOR, XNOR, PF, SCPF and MPF different voltages from 0.7 V to 1.2 V. Power consumed should be less. MPF CAM Cell has the dynamic power 94.7% less than NOR Type, 95% less than NAND Type, 46.8% less than XOR Type, 42.5% less than XNOR Type, 46.8% less than PF CAM Cell and 51.18% less than SCPF CAM Cell. The analysis outcome show that less power is utilised by MPF CAM cell when compared to all the cells. Dynamic power in μW for different CAM cells of word length 3 bit like NOR, NAND, XOR, XNOR, PF, SCPF and MPF at 1.2 V is given in Table 2. Power consumed should be less. MPF CAM Cell has the dynamic power 78.49% less than NOR Type, 64.82% less than NAND Type, 34.9% less than XOR Type, 17.2% less than XNOR Type, 48.27% less than PF CAM Cell and 52.6% less than SCPF CAM Cell. MHSCPF and MPF CAM cell have nearly equal power with a variation of 10%. From the both the results it is clear that less power is consumed by MPF CAM cell when compared to all the cells with 1 bit word length as well as 3-bit word length.

Table 1 Dynamic Power in μW for different 1 bit CAM cells for different voltages

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF
1.2	35.47	37.23	3.5	3.236	3.498	3.808	1.859
1.1	26.67	28.39	2.346	2.199	2.183	2.48	1.206
1	19.29	20.94	1.518	1.439	1.339	1.544	0.7441
0.9	13.26	14.79	0.9438	0.901	0.802	0.915	0.4322
0.8	8.554	9.857	0.5615	0.5362	0.4608	0.514	0.2347
0.7	5.098	6.048	0.3166	0.3006	0.2498	0.2709	0.118

Table 2 Dynamic Power in μW for different 3-bit CAM cells at 1.2 V

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF	MHSCPF
1.2	40.77	24.93	13.47	10.59	16.95	18.5	8.768	9.573

4.4 DELAY

Delay is the time at which input is given and when the output is obtained. It is defined as the average of the high-to-low (*tPHL*) and low-to-high (*tPLH*) delay.

Table 3 Delay in ns for different 1 bit CAM cells for different voltages

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF
1.2	20.385	0.5208	0.9776	1.7255	0.3972	1.5975	0.4598
1.1	20.34	0.5607	0.8518	1.7815	0.2868	1.6835	0.4336
1	20.345	0.5966	0.6959	1.86	0.2023	1.786	0.4014
0.9	20.405	0.6189	0.4954	1.9675	0.0853	1.9105	0.3613
0.8	20.495	0.6051	0.2103	2.117	0.0381	2.067	0.3118
0.7	20.63	0.5441	0.1060	2.347	0.0261	2.29	0.2489

Table 3 shows Delay in ns for different 1 bit CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF and MPF for different voltages from 0.7 V to 1.2 V. PF CAM cell has less delay when compared to all the other cells. MPF CAM cell has lowest value of delay after SCPF CAM cell. Delay for a cell should be less so that it can operate at a faster speed. Table 4 shows Delay in ns for different 3-bit CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF, MPF and MHSCPF at 1.2 V. All the CAM cells have less delay (below 10 ns) except NOR Type. From the both the results it is clear that MPF CAM cell and PF CAM cell has lowest delay when compared to all the cells with 1 bit word length as well as 3-bit word length.

Table 4 Delay in ns for different 3-bit CAM cells at 1.2 V

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF	MHSCPF
1.2	86.75	3.88	4.9928	7.345	1.191	7.065	1.397	6.522

4.5 POWER DELAY PRODUCT

The power delay product is the product of dynamic power with delay. PDP for a cell should be less. It is the energy consumed by all the cells. The PDP for XNOR CAM cell is less when analysed with all the other cells. Table 5 gives Power Delay Product in fJ for different 1 bit CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF and MPF for different voltages from 0.7 V to 1.2 V. MPF CAM Cell has the lowest PDP when compared to all the other cells. PDP of MPF CAM Cell is 38.44% less than PF CAM Cell, 95.59% less than NAND Type, 75% less than XOR Type, 84.67% less than XNOR Type, 85.94% less than SCPF CAM.

Table 5 Power Delay Product (Energy in fJ) in different 1 bit CAM cells for different voltages

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF
1.2	721.63	19.39	3.42	5.58	1.389	6.083	0.855
1.1	542.47	15.92	1.99	3.92	0.626	4.175	0.523
1	392.46	12.49	1.056	2.68	0.271	2.757	0.299
0.9	270.57	9.15	0.467	1.77	0.068	1.748	0.156
0.8	175.31	5.96	0.118	1.135	0.017	1.062	0.073
0.7	105.17	3.29	0.034	0.705	0.0065	0.620	0.029

Table 6 Power Delay Product (Energy in fJ) in different 3-bit CAM cells at 1.2 V

Voltage (V)	NOR Type	NAND Type	XOR Type	XNOR Type	PF	SCPF	MPF	MHSCPF
1.2	3536.79	96.7284	67.253	77.783	20.187	130.702	12.248	62.435

Power Delay Product in fJ for different 3-bit CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF, MPF and MHSCF at 1.2 V is shown in Table 6. MPF CAM Cell has lowest delay and PF CAM Cell is second lowest. PDP of MPF CAM Cell is 39.32% less than PF CAM, 87.752% less than NAND Type, 81.788% less than XOR Type, 84.25% less than XNOR Type, 90.62% less than SCPF CAM, 80.38% less than MHSCPF CAM. From the both the results it is clear that MPF CAM cell and PF CAM cell has lowest PDP when compared to all the cells with 1 bit word length as well as 3-bit word length.

4.6 STATIC NOISE MARGIN

Static noise margin is used for finding the stability of the cell. Higher the SNM then the cell is better stable. Butterfly curve is drawn for the inverters connected back-to-back. Then the diagonal of largest square which can fit in the butterfly curve gives the noise margin. Figure 27 shows the SNM Butterfly curve for MPF CAM Cell and SNM value of 518.35 mV is obtained.

4.7 8X8 MEMORY ARRAY USING MPF CAM CELLS

Figure 28 and Figure 29 displays the result of 8X8 CAM array made up of MPF CAM cells. MPF CAM Cell increases the performance of the CAM array and reduces the power and delay as there is no need for pre-charge circuit. In Figure 28, search word matches with stored word at 2^{nd} row as ML1 is alone high. Output of o3=0, o2=0 and o1=1 is obtained which is the address of 2^{nd} row. In Figure 29, search word matches with stored word at 5^{th} row as ML4 is alone high. Output of o3 = 1, o2 = 0 and o1 = 0 is obtained which is the address of 5^{th} row.

Table 7 gives the various factors such dynamic power, delay and power delay product that affect the performance for various 8X8 CAM array structures like NOR Type, PF, MPF at 1.2 V. It is obvious from the table that MPF CAM Array has less dynamic power, delay and PDP when compared to NOR Type and PF.

Table 7 Parameters of different 8X8 CAM Array at 1.2 V

Parameter	NOR Type	PF	MPF
Dynamic Power (μW)	449.5	194.4	104.7
Delay (ns)	125.3	20.749	11.864
Power Delay Product (pJ)	56.322	4.0336	1.2421

4.8 SUMMARY

The various parameter analysis like delay, power, power delay product reveal that in most cases the MPF CAM has better performance. MPF CAM has lowest dynamic power and it is 48.27% less than PF CAM Cell and 52.6% less than SCPF CAM Cell. Delay of MPF CAM is less than other cells but slightly higher than PF CAM Cell. PDP is 39.32% less than PF CAM, 90.62% less than SCPF CAM, 80.38% less than MHSCPF CAM. SNM of MPF CAM Cell is 518.35 mV. The 8X8 MPF CAM Array has dynamic power of 104.7 μW, delay of 11.864 ns and PDP of 1.2421 pJ. Dynamic power of MPF CAM Array is 46.14% less than PF CAM Array, and delay is 42.82% less and PDP is 69.206% less.

5. Conclusion

CAM cells used in routers should have less power, less area and high speed. MPF CAM cell was designed and compared with other CAM cells like NOR, NAND, XOR, XNOR, PF, SCPF, MHSCPF CAM cell for factors

like delay, power and power delay product. In MPF CAM cell, the dynamic power is 48.27% less than PF CAM Cell and 52.6% less than SCPF CAM Cell. Delay of MPF CAM cell is less and its nearly equal to the existing CAM cells but slightly higher than PF CAM Cell. PDP is 39.32% less than PF CAM, 90.62% less than SCPF CAM, 80.38% less than MHSCPF CAM. SNM of MPF CAM Cell is 518.35 mV. The 8X8 MPF CAM Array has dynamic power of 104.7 μW, delay of 11.864 ns and PDP of 1.2421 pJ. MPF CAM Array has lowest dynamic power, delay and PDP when compared to NOR CAM Array and PF CAM Array. Successful designing of 8X8 Memory array using sense amplifiers, pre-charge circuits, decoders and encoder has been done and parameters like delay, power and power delay product are measured for various voltages. Thus, a MPF CAM cell with 46.14% less power and with 42.82% less delay when compared to PF CAM cell has been designed as 8X8 memory array and can be used in routers and high-speed searching applications.

Declarations

Funding – Not Applicable

Conflicts of interest/Competing interests

The authors whose names are listed immediately certify that they have NO affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

Availability of data and material – Not Applicable

Code availability – Not Applicable

Authors' contributions – All authors are equally contributed

Ethics approval - Agreed

Consent to participate – Yes

Consent for publication - Yes

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current work.

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Figures

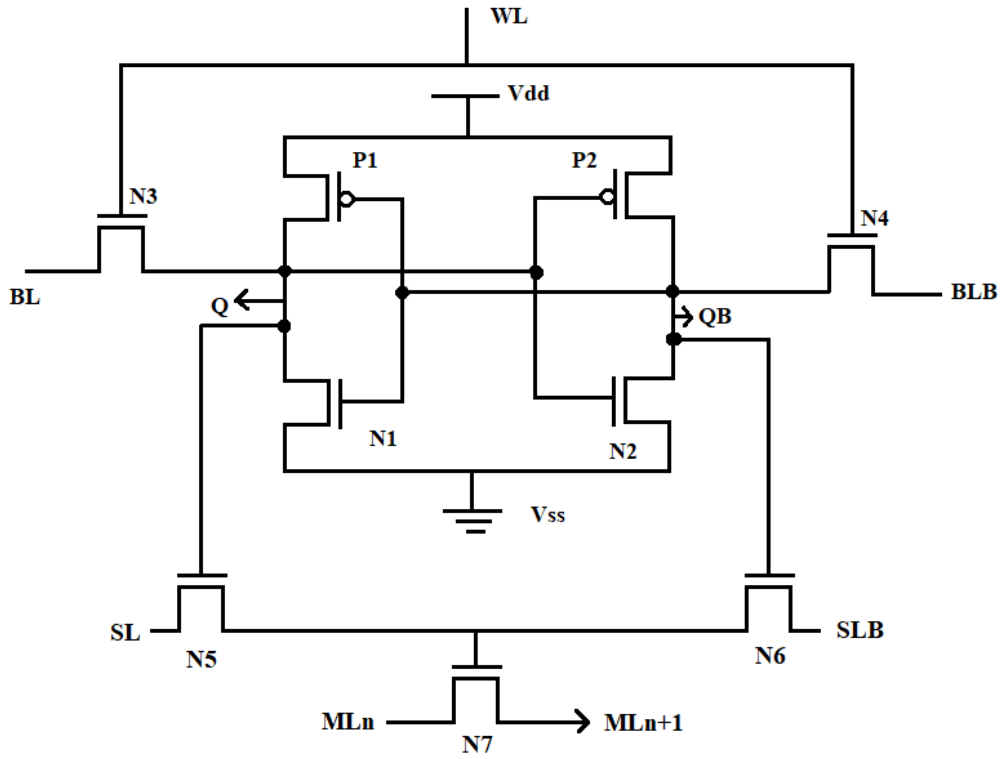

Figure 1

Circuit of NOR CAM Cell

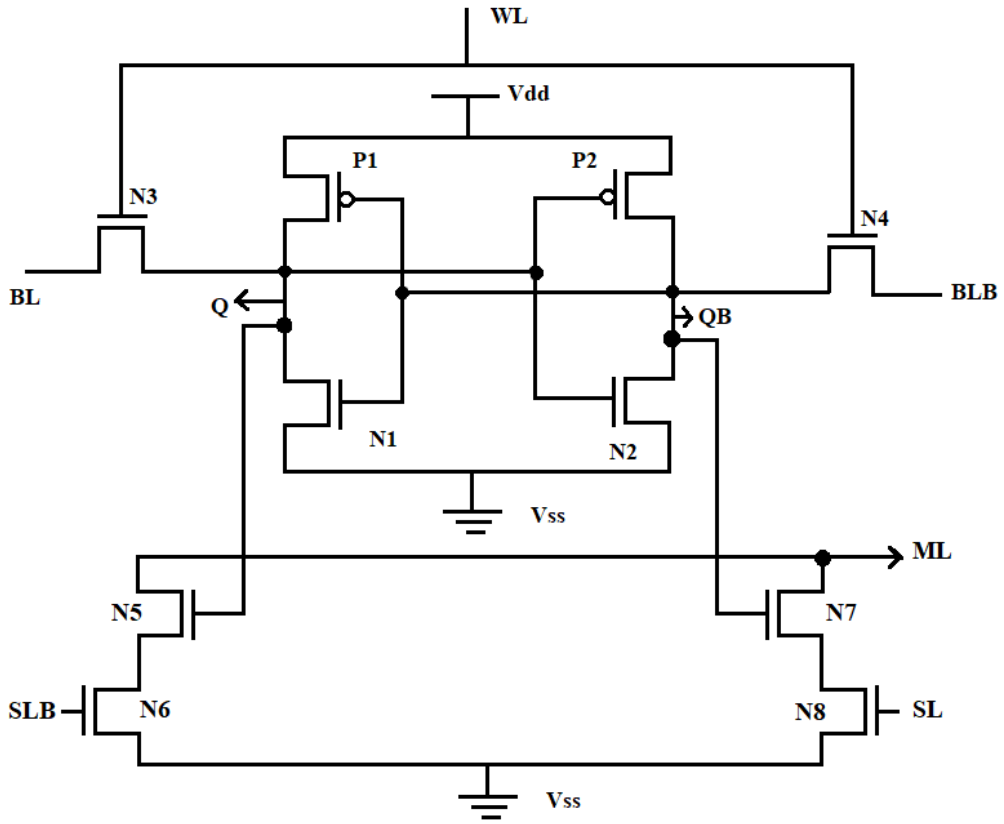

Figure 2

Circuit of NAND CAM Cell

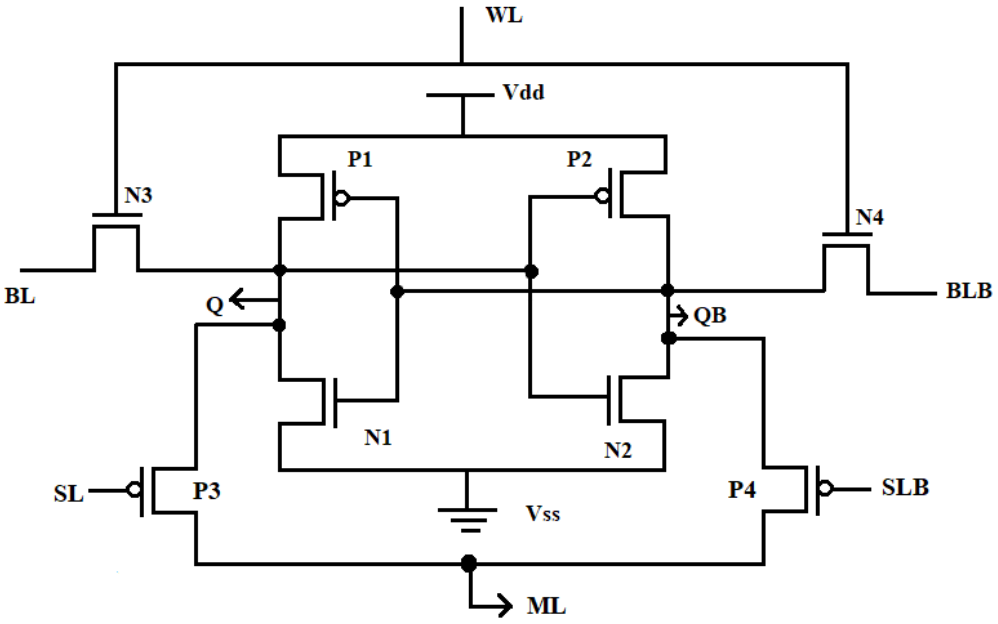

Figure 3

Circuit of XOR CAM Cell

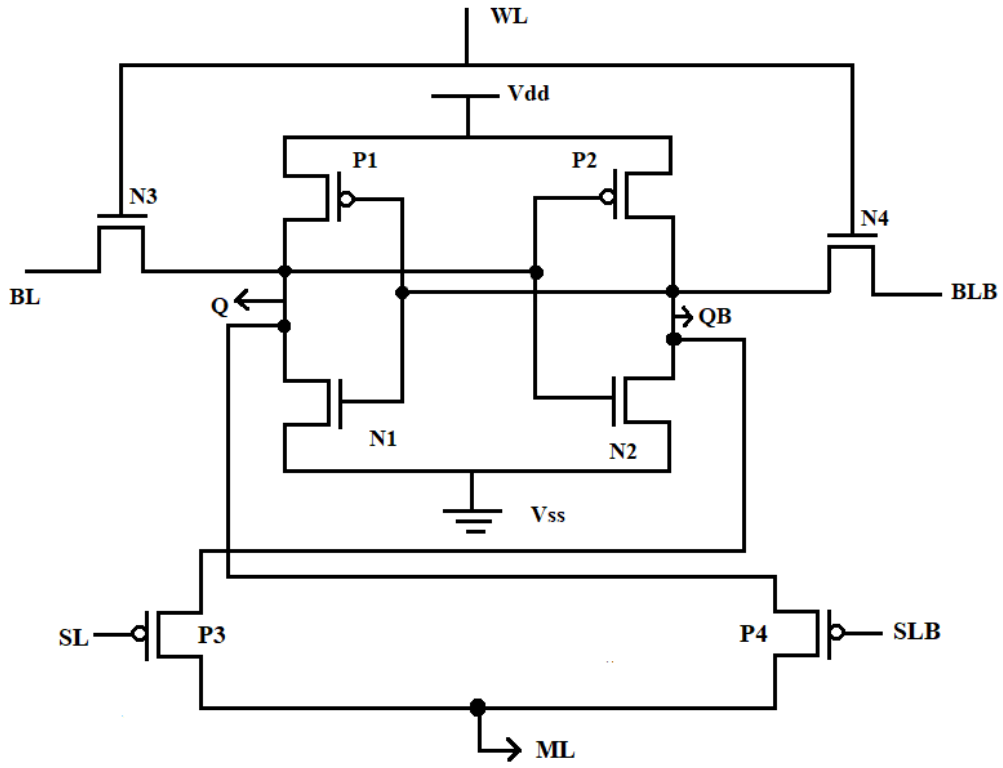

Figure 4

Circuit of XNOR CAM Cell

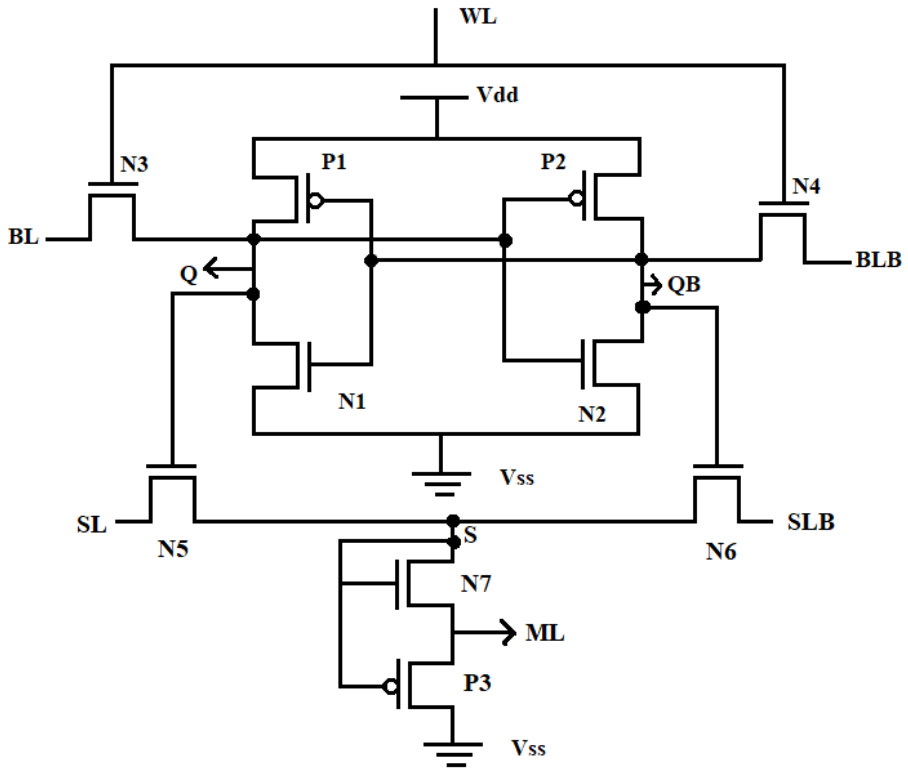

Figure 5

Circuit of PF CAM Cell

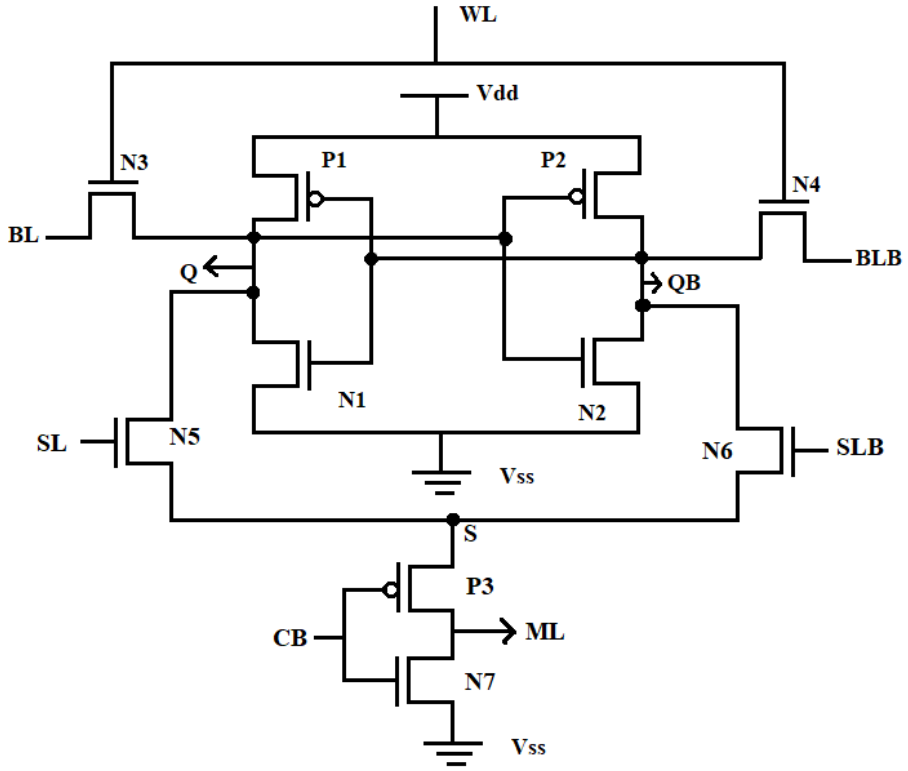

Figure 6

Circuit of SCPF CAM Cell

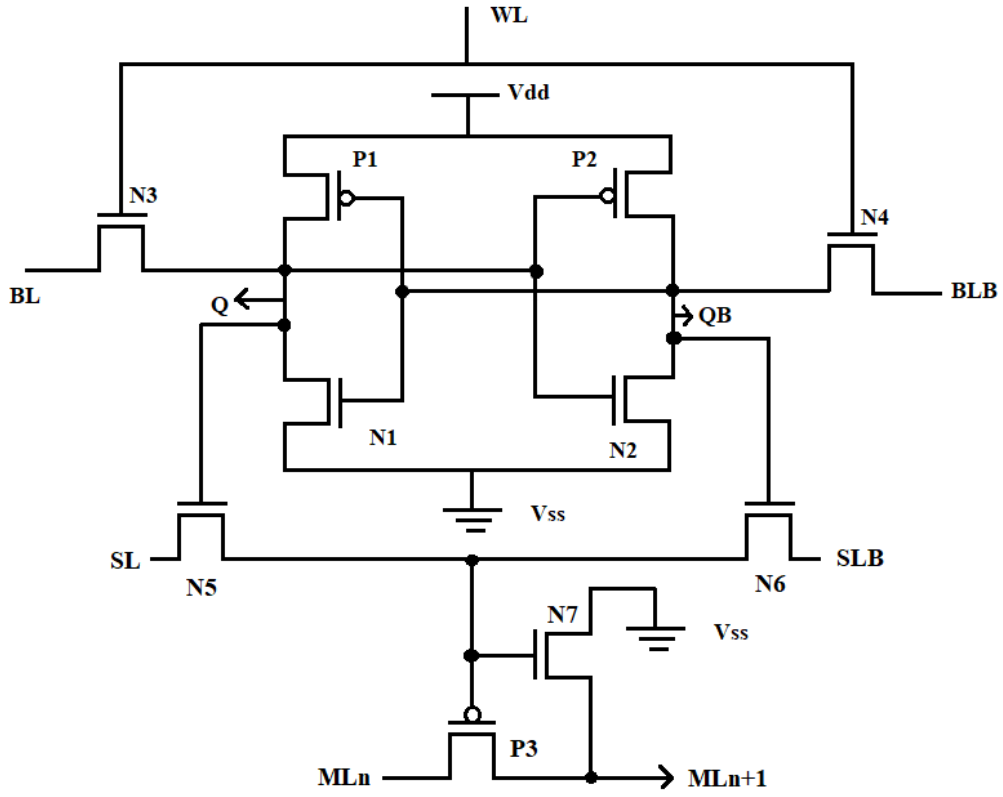

Figure 7

Circuit of MPF CAM Cell

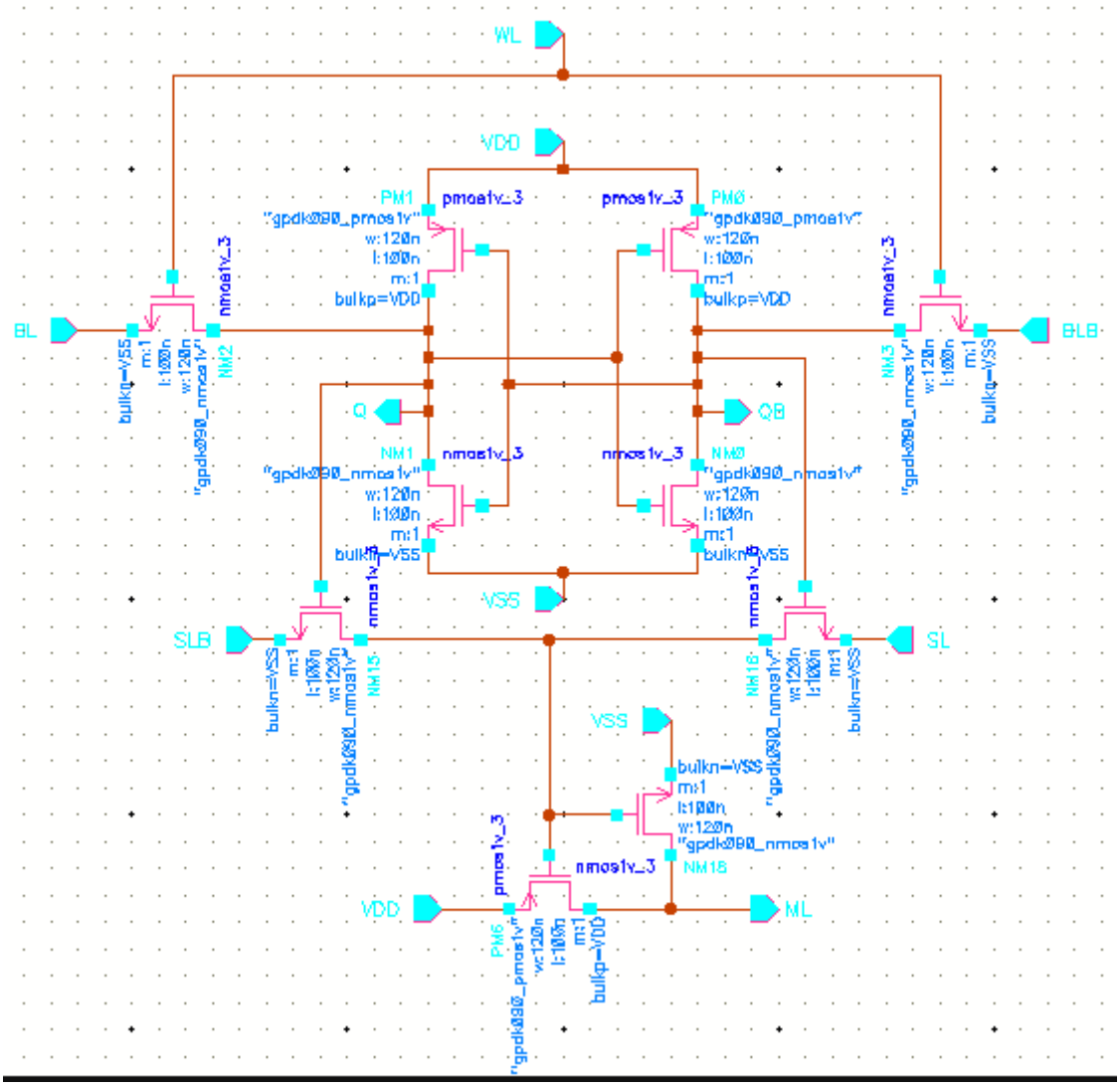

Figure 8

Tool View of MPF CAM Cell

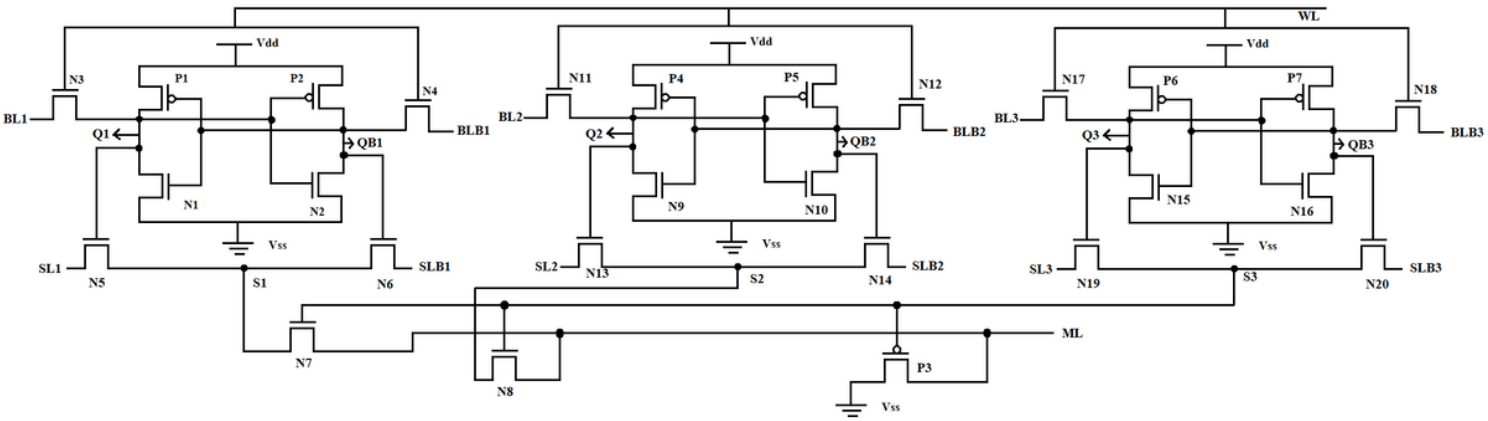

Figure 9

Circuit of MHSCPF CAM Cell

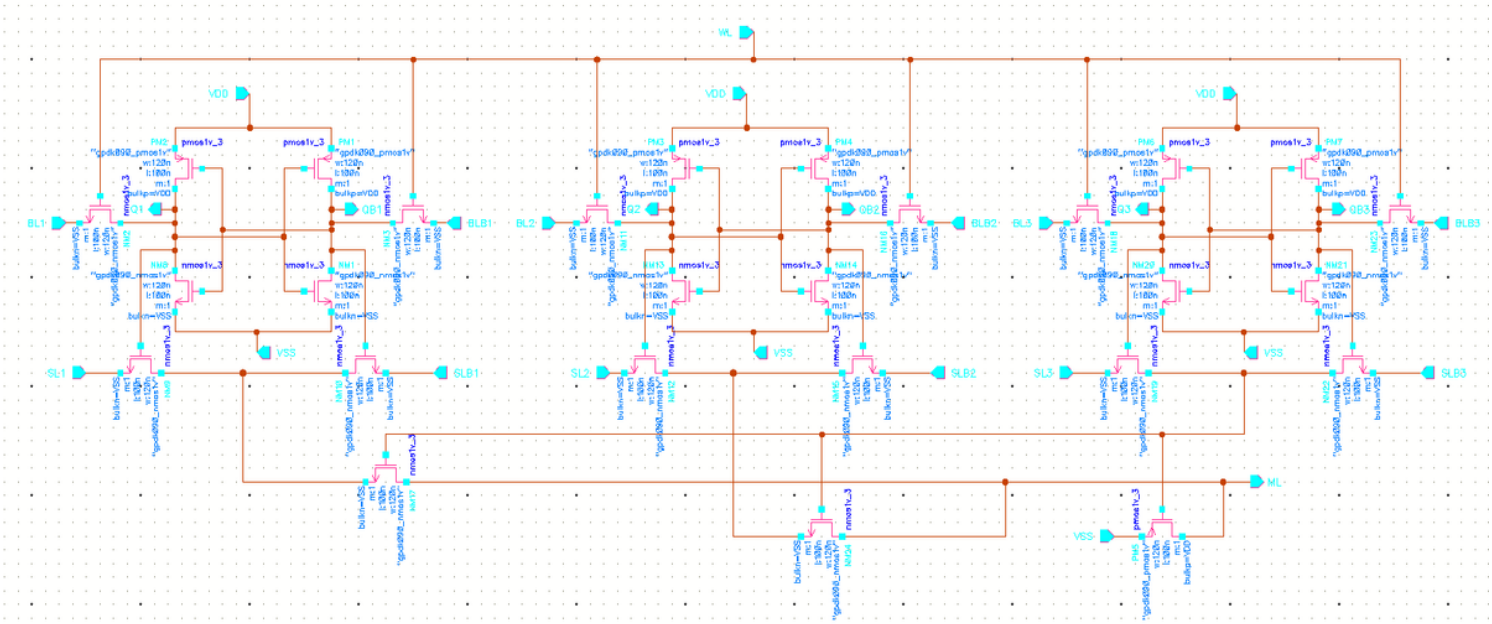

Figure 10

Tool View of MHSCPF CAM Cell

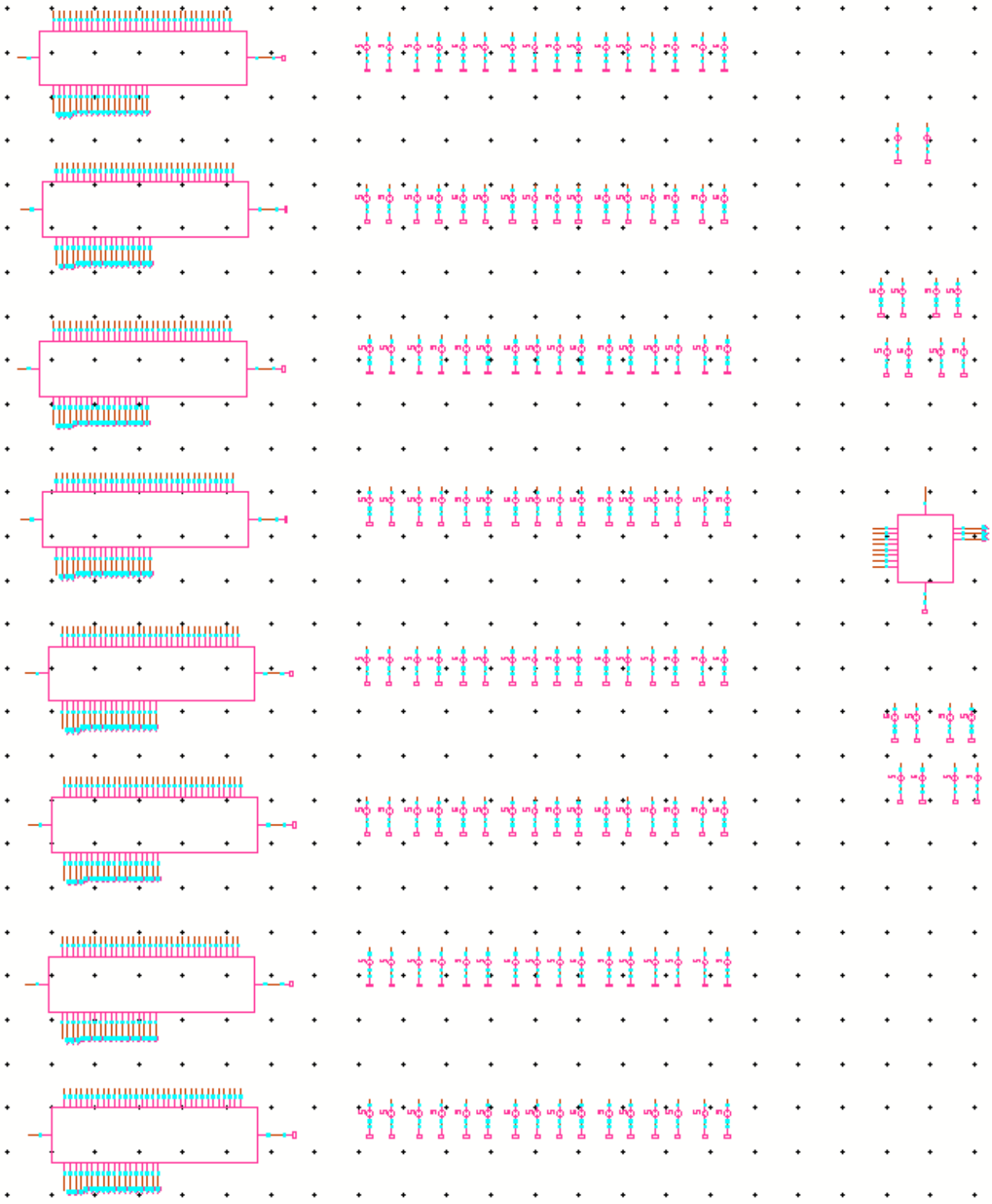

Figure 11

Schematic View of Memory Array

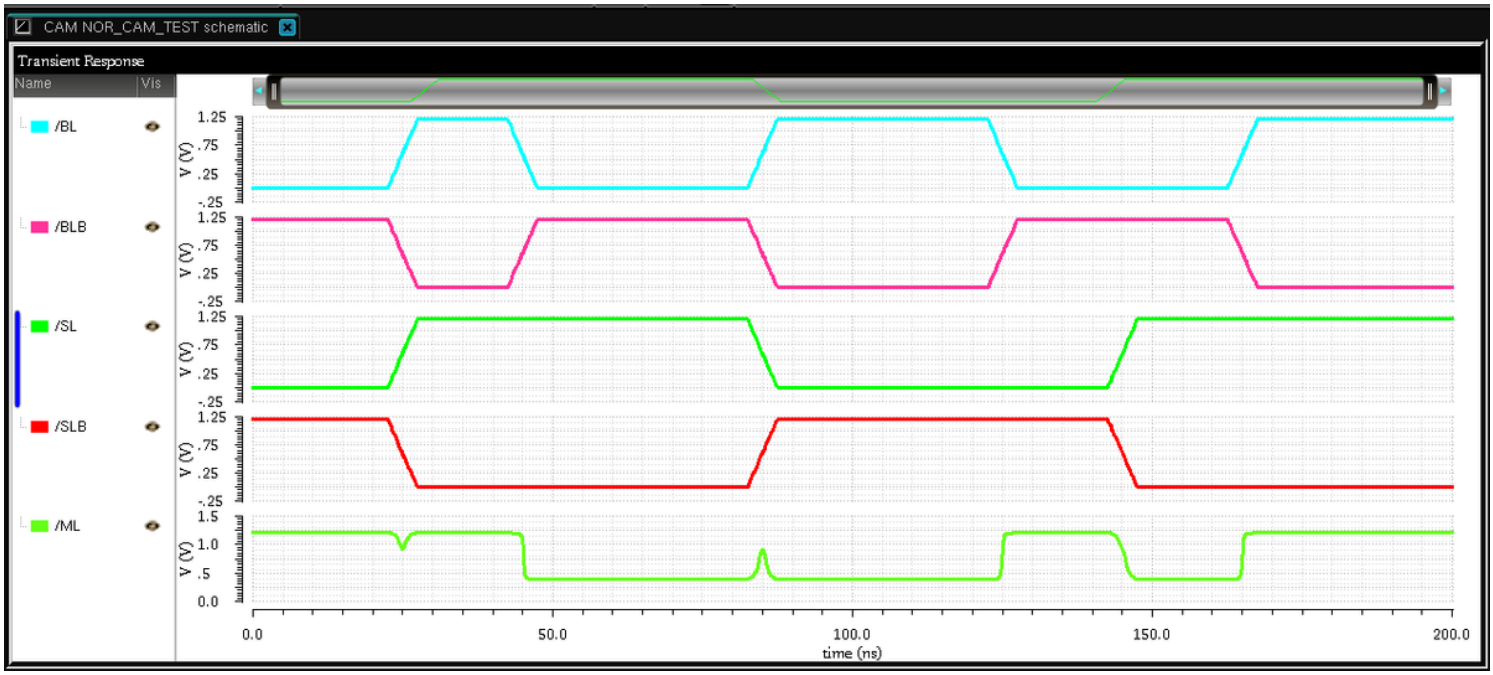

Figure 12

Waveform of NOR CAM Cell

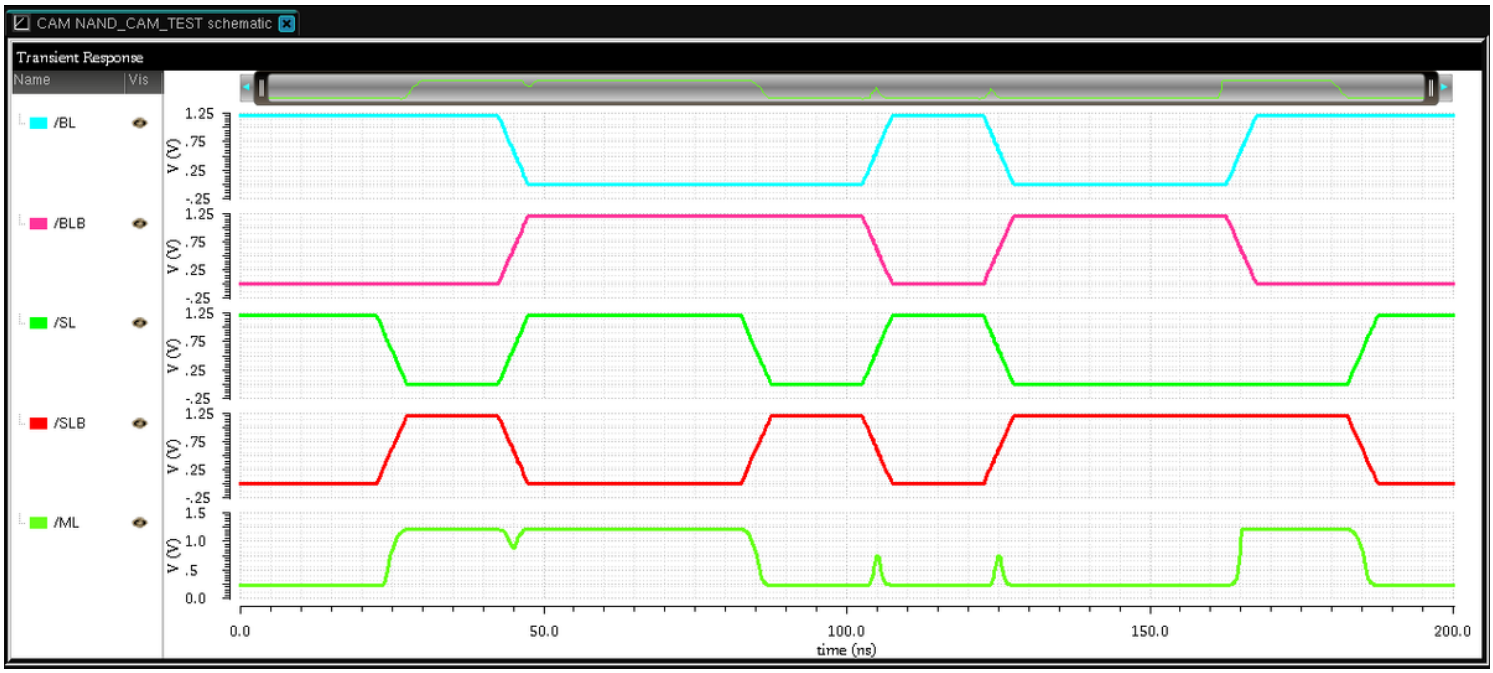

Figure 13

Waveform of NAND CAM Cell

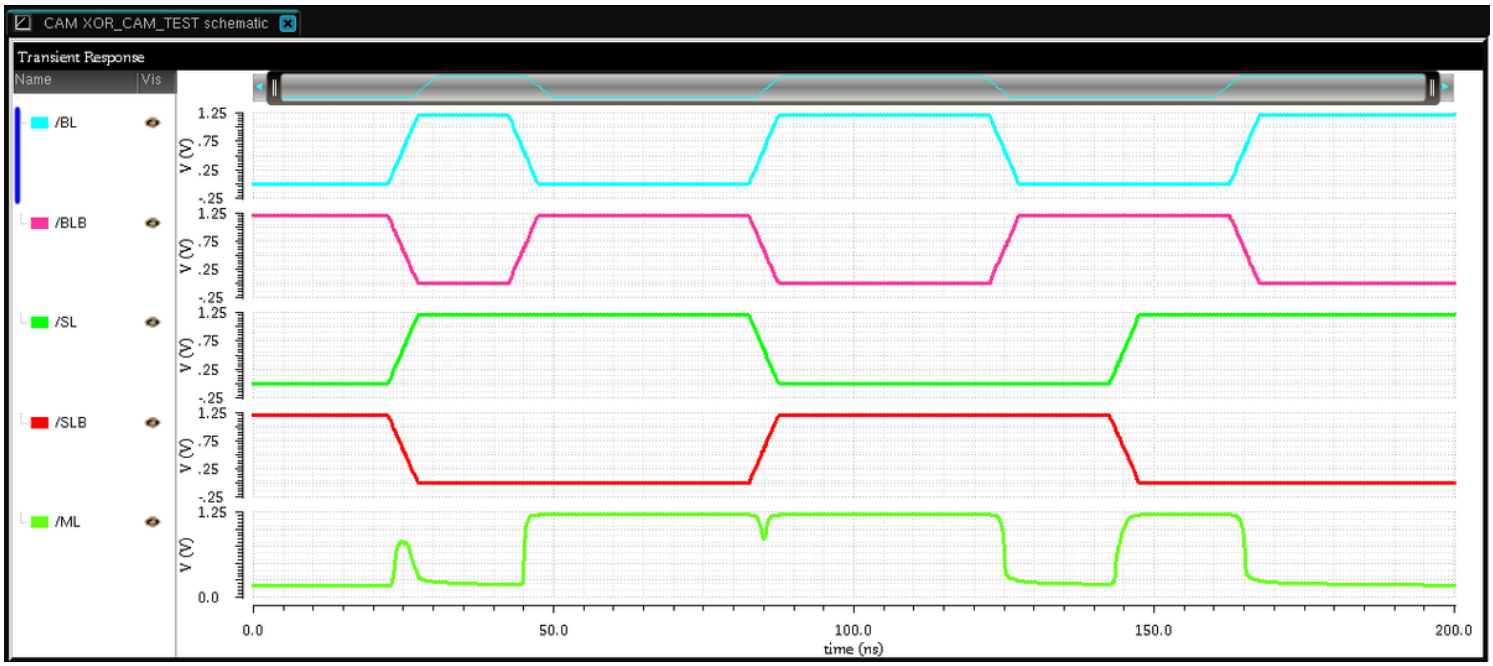

Figure 14

Waveform of XOR CAM Cell

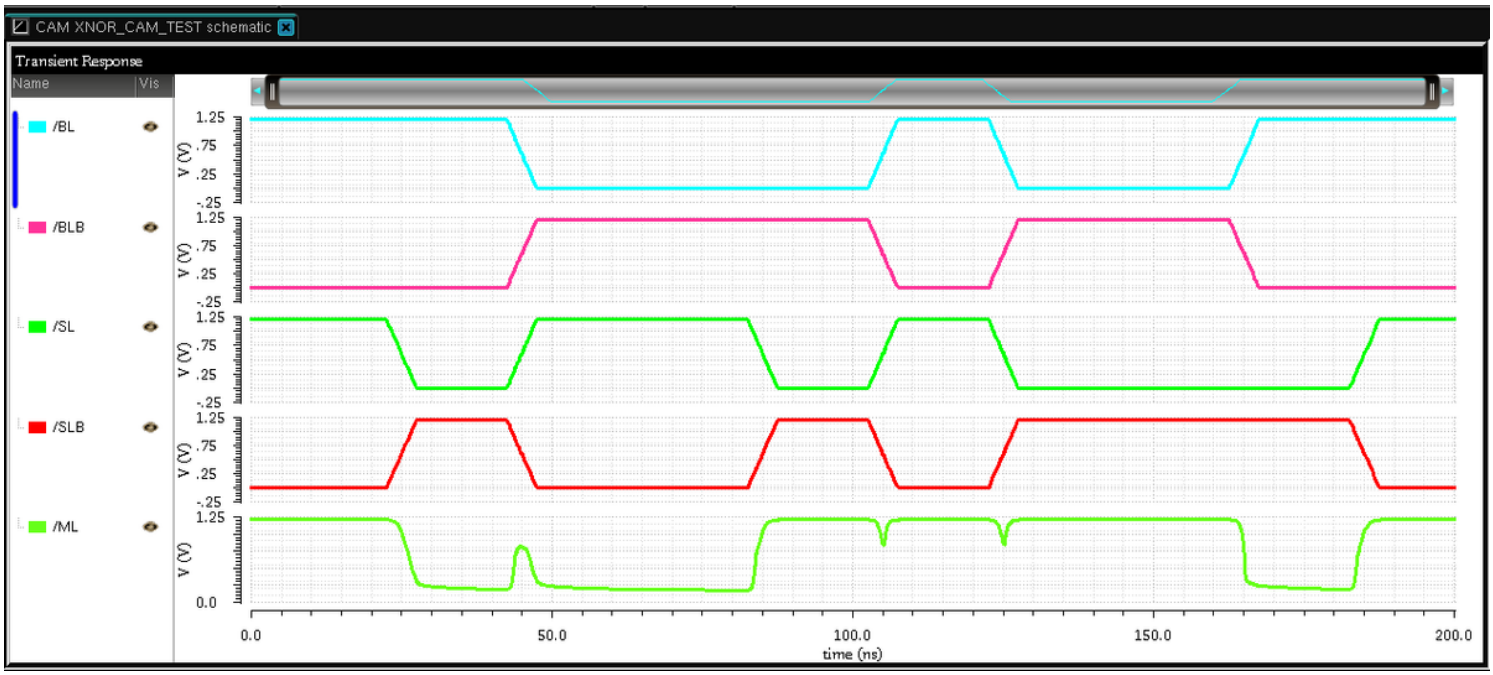

Figure 15

Waveform of XNOR CAM Cell

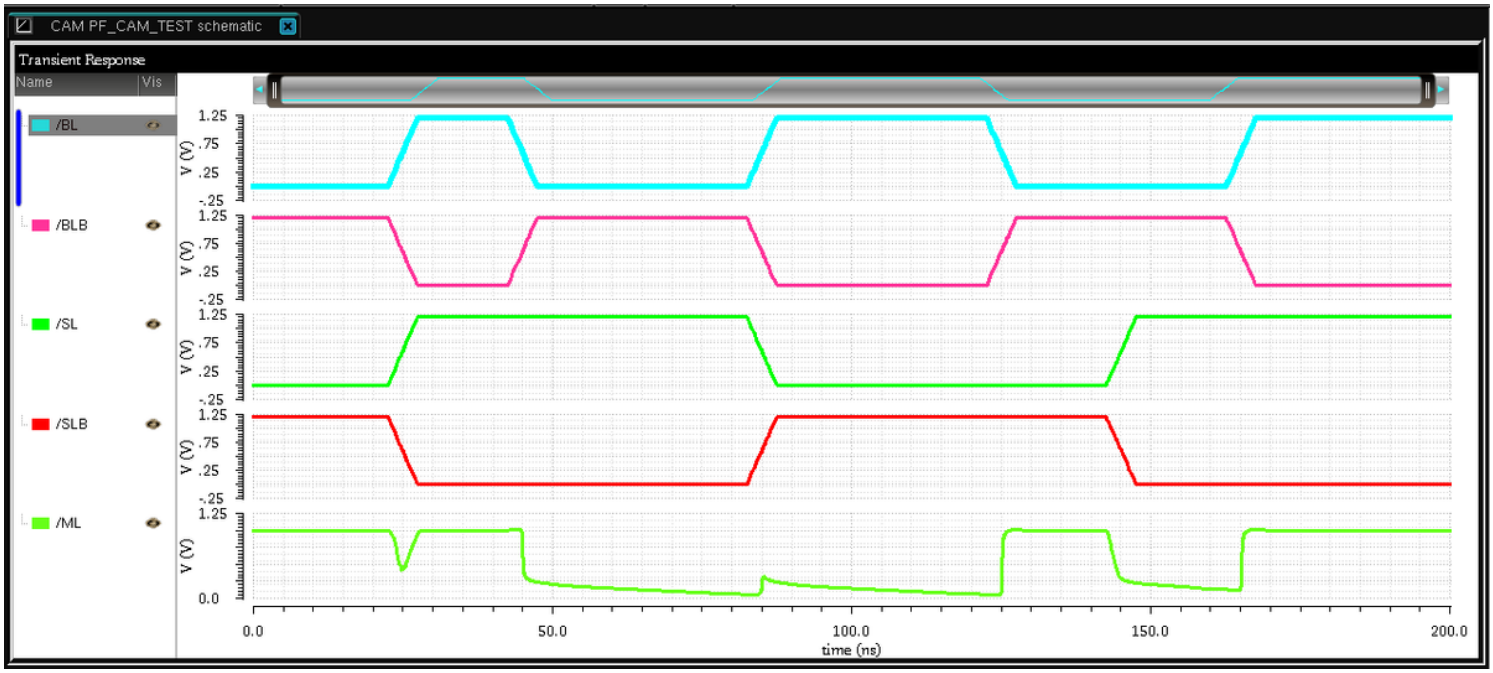

Figure 16

Waveform of PF CAM Cell

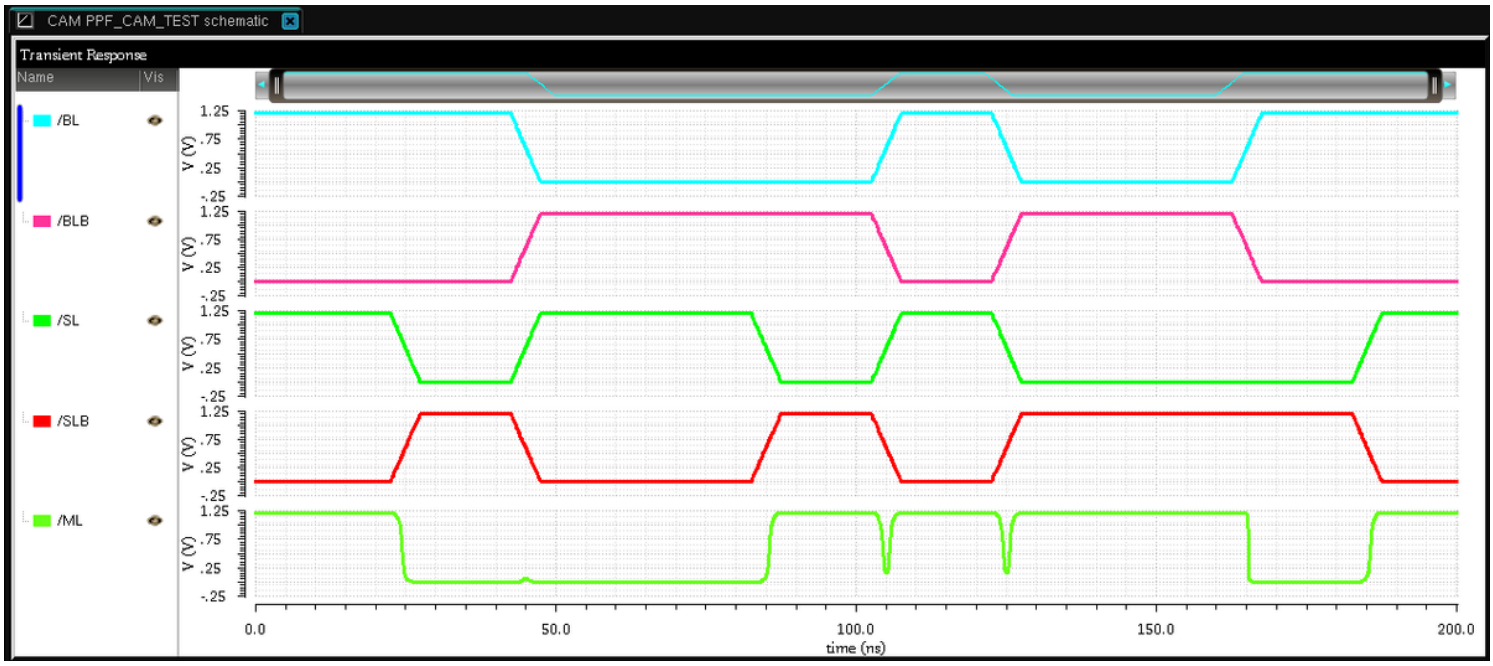

Figure 17

Waveform of SCPF CAM Cell

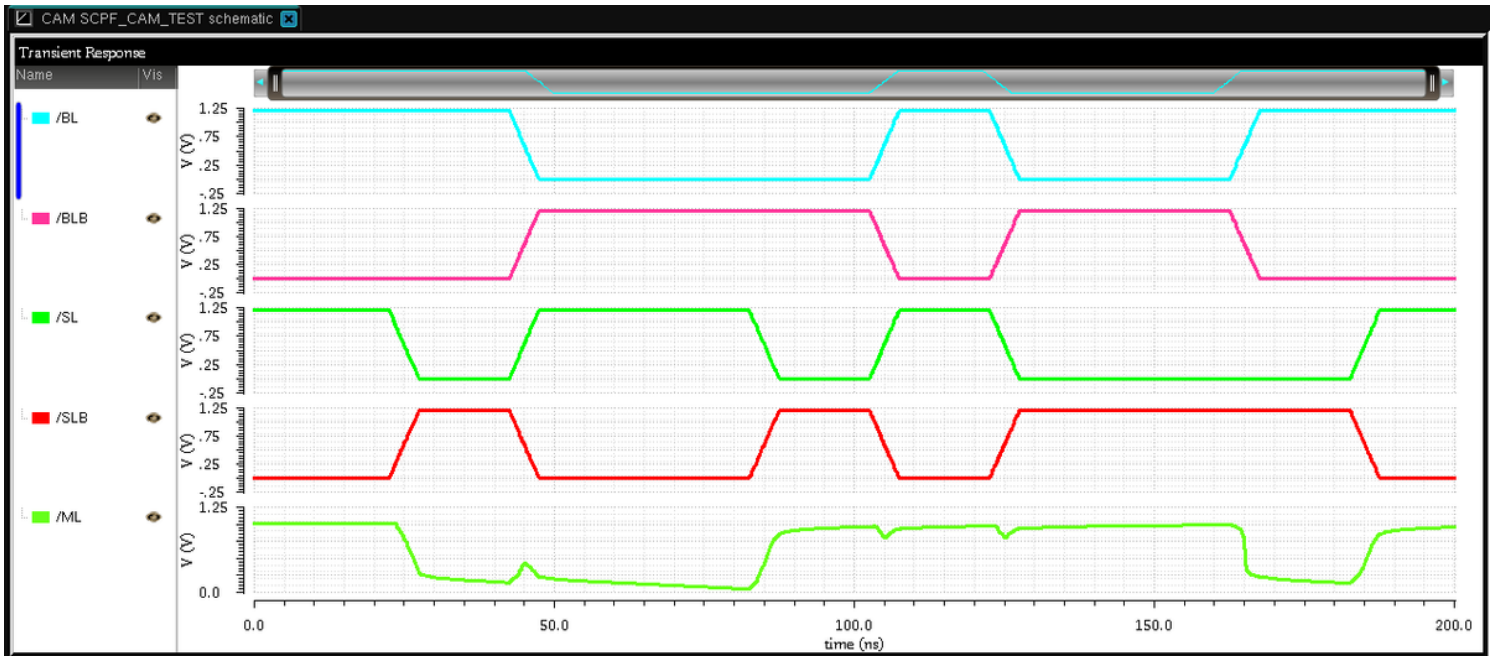

Figure 18

Waveform of MPF CAM Cell

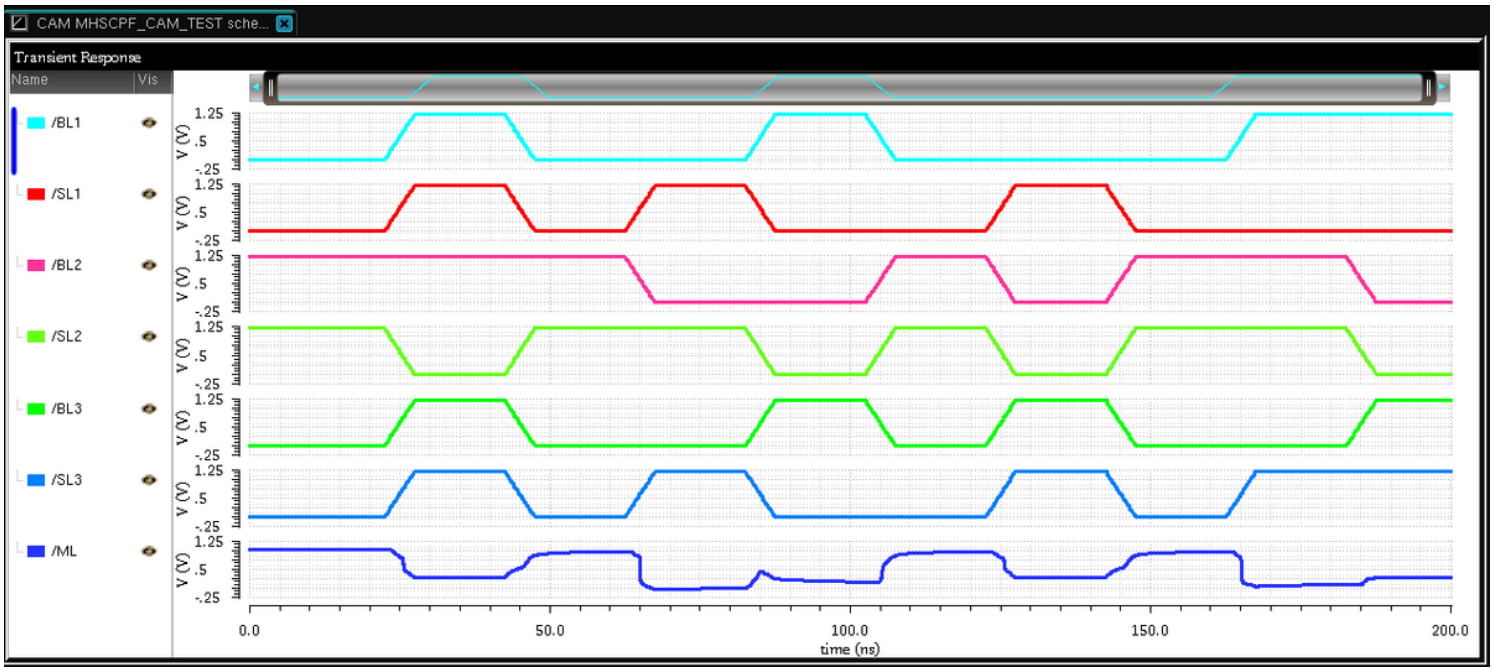

Figure 19

Waveform of MHSCPF CAM Cell

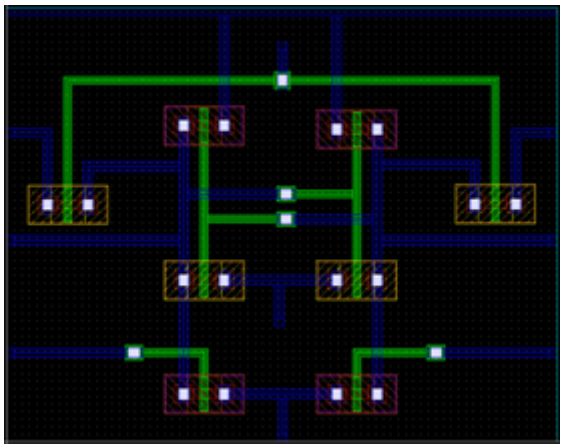

Figure 20

Layout of NOR CAM

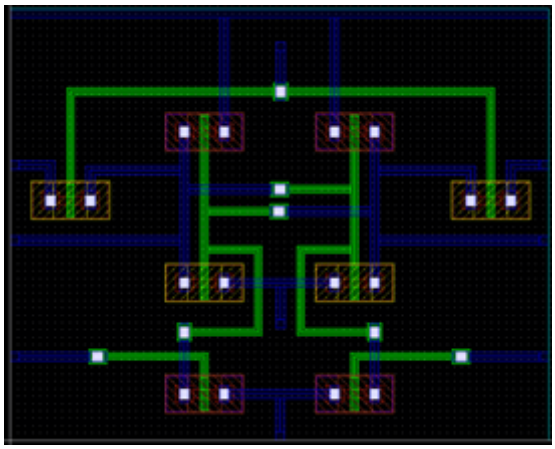

Figure 21

Layout of NAND CAM

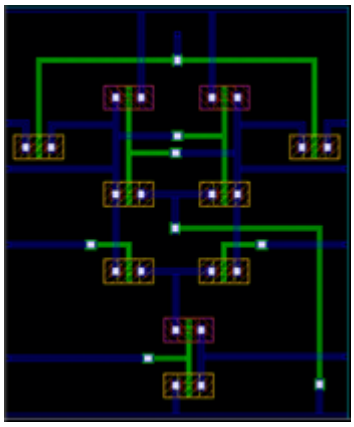

Figure 22

Layout of XOR CAM

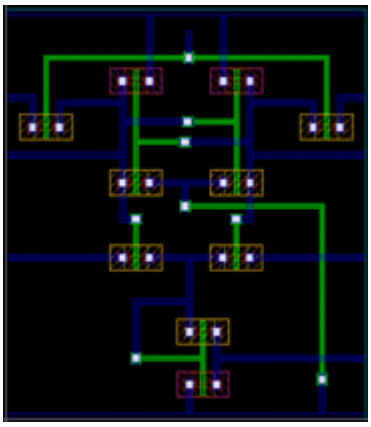

Figure 23

Layout of XNOR CAM

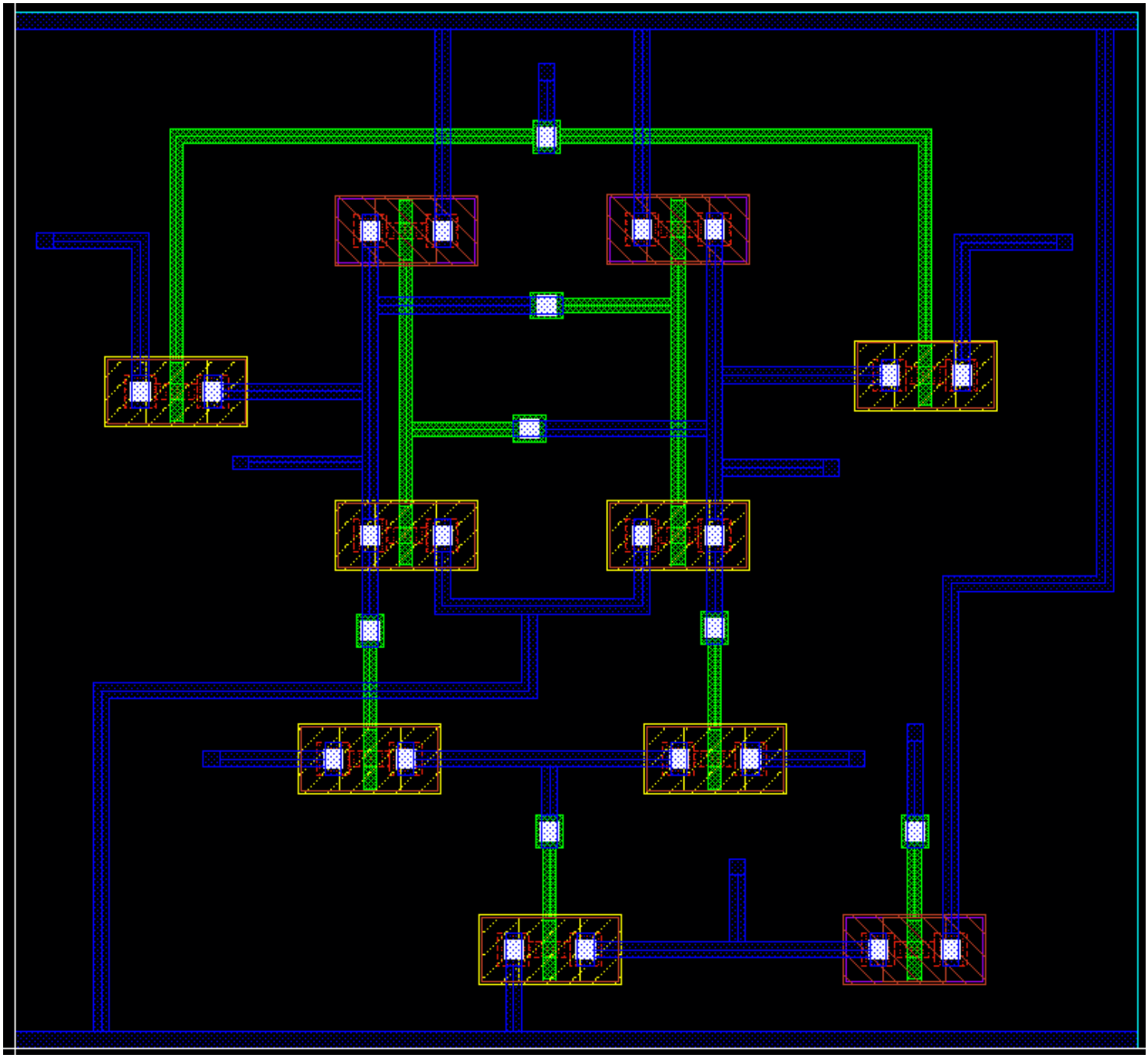

Figure 24

Layout of PF CAM

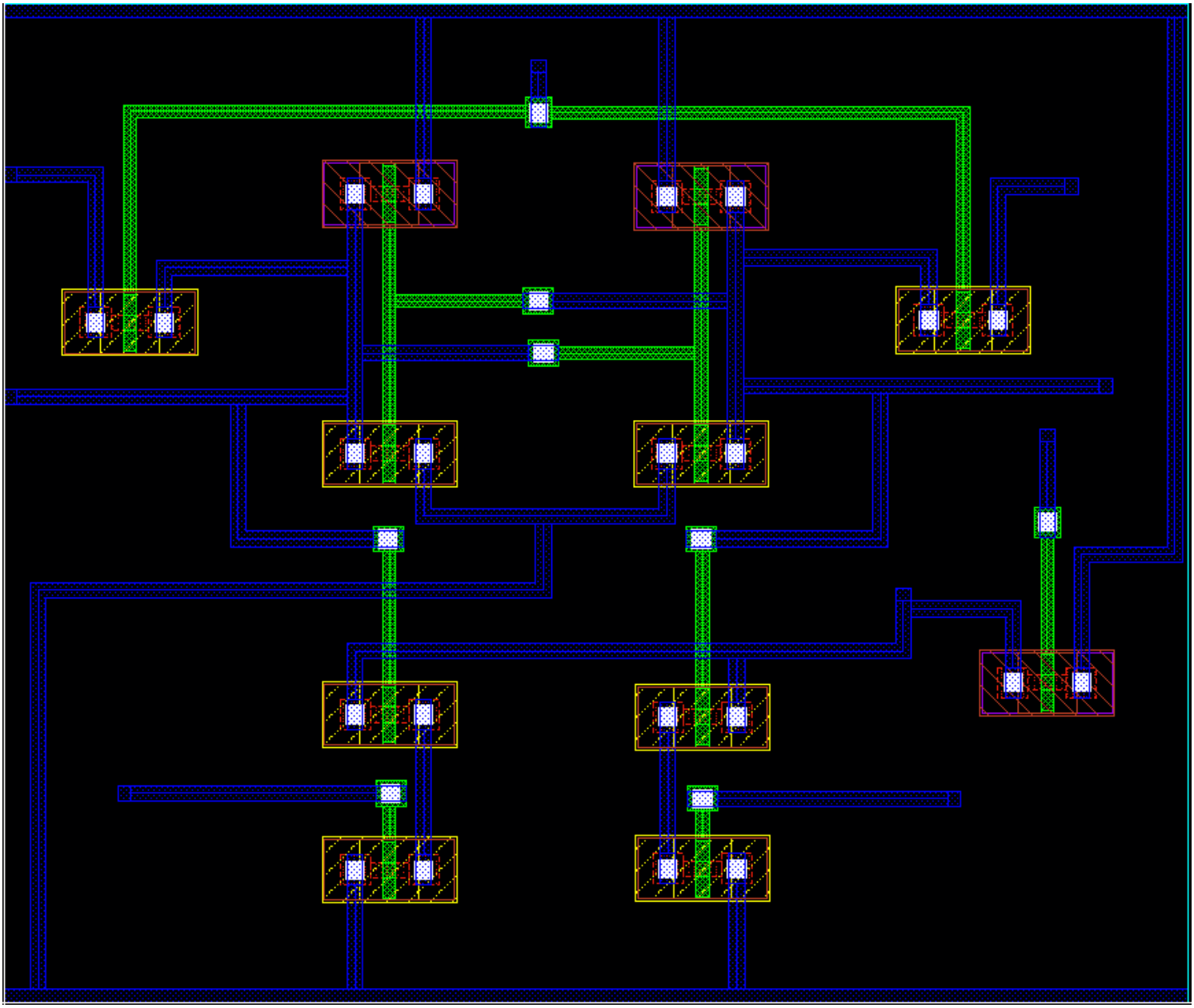

Figure 25

Layout of SCPF CAM

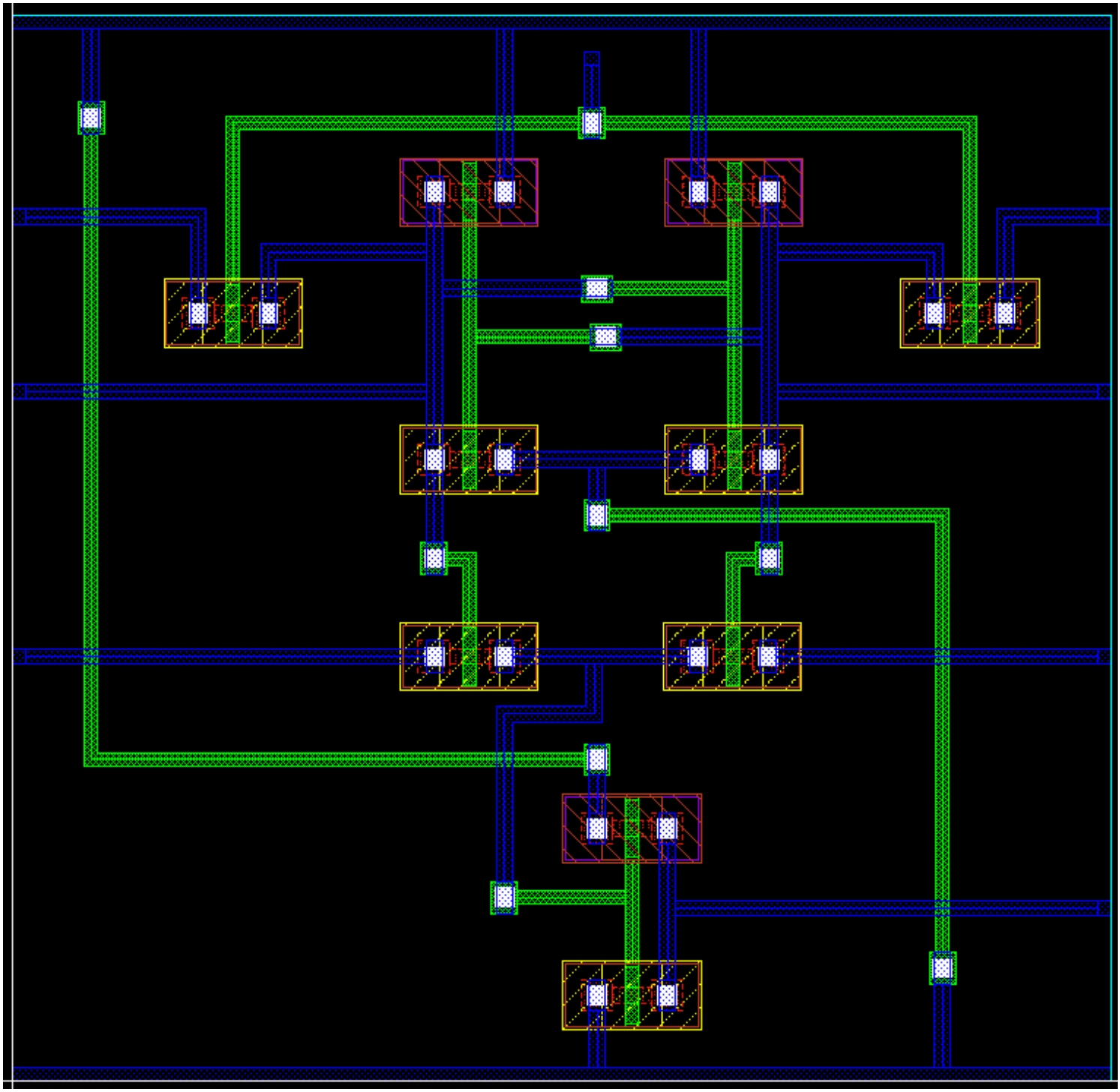

Figure 26

Layout of MPF CAM

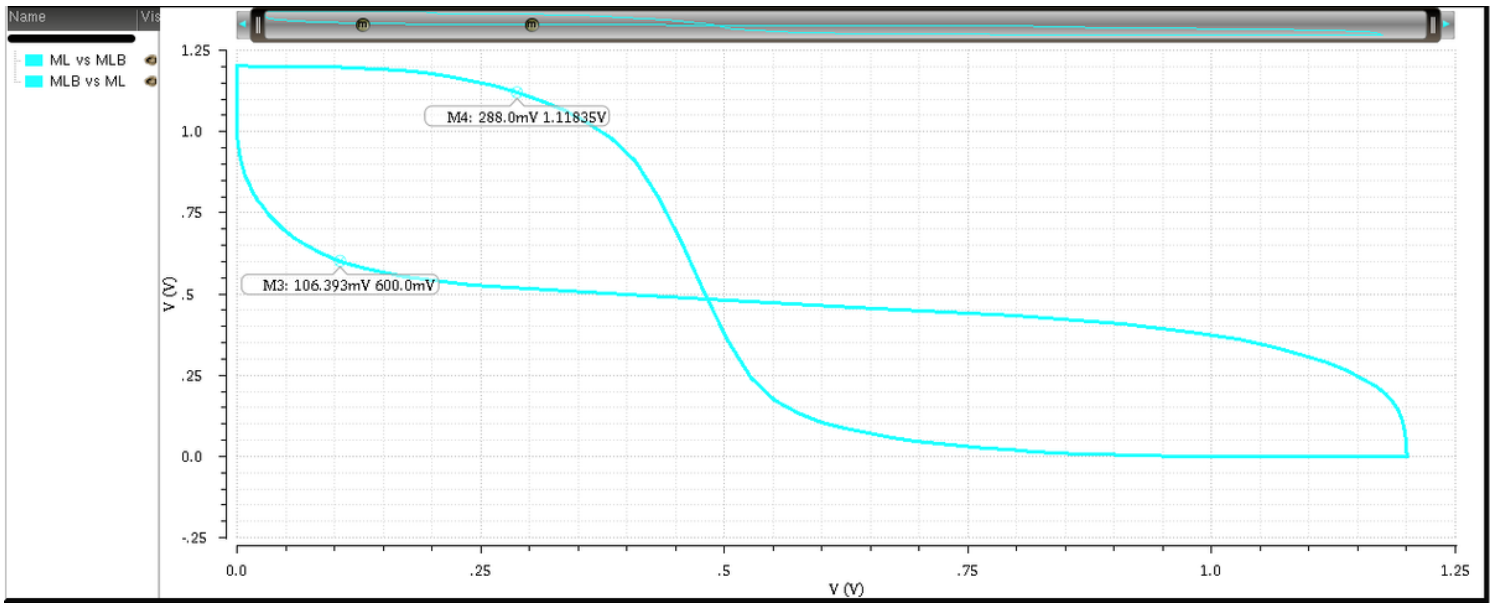

Figure 27

SNM of MPF CAM

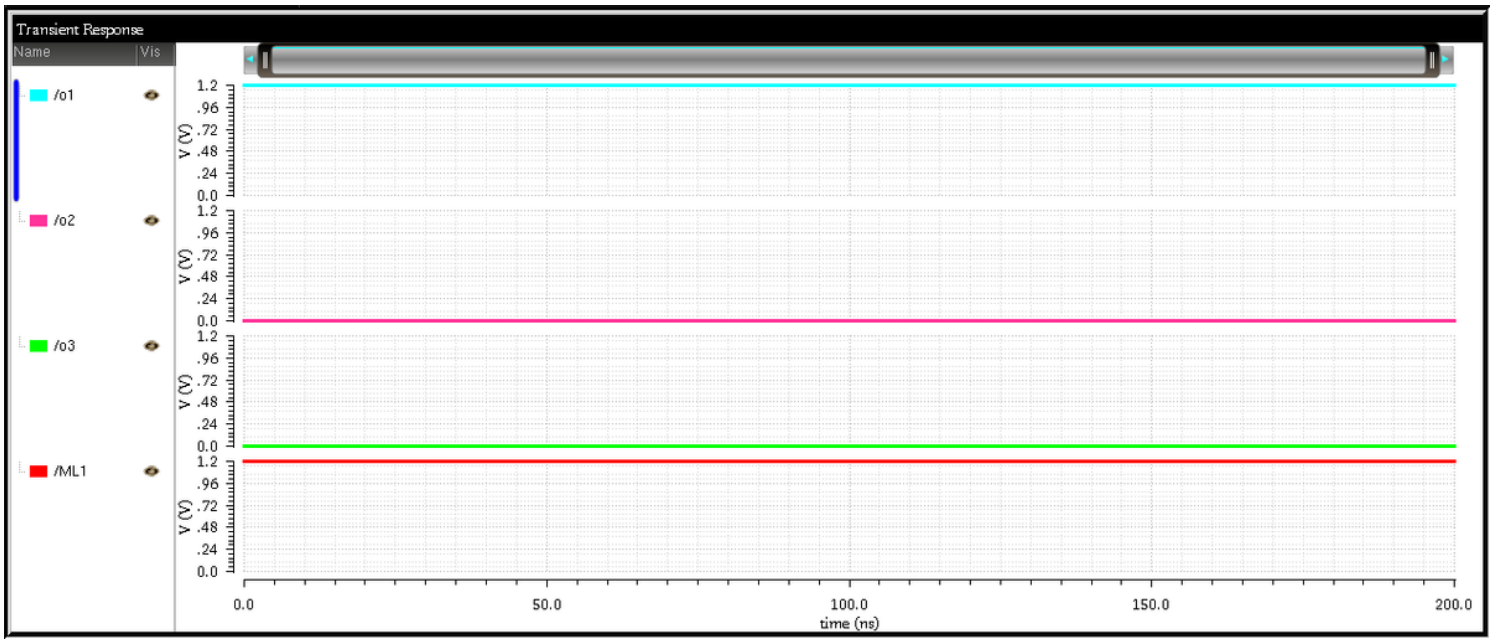

Figure 28

Output waveform of 8X8 Memory array when ML1 = 1

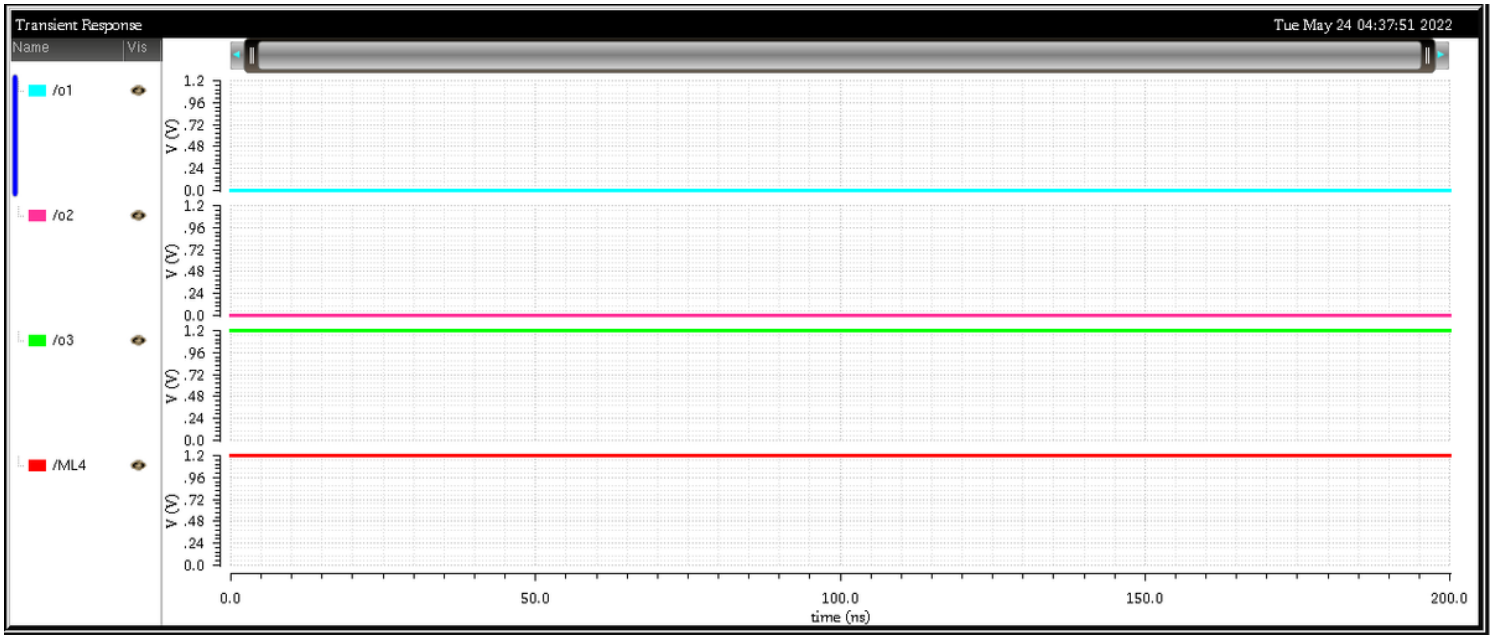

Figure 29

Output waveform of 8X8 Memory array when ML4 = 1