Fault Detection in Multi-input Analog Circuits using Regression Modelling

Anjali Rai (raianjali543@gmail.com)
Indian Institute of Technology (Indian School of Mines)
Rahul Bhattacharya
Indian Institute of Technology (Indian School of Mines)

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Abstract

The aim of this paper is to detect parametric faults in multi-input analog circuits by solving for the coefficients of a polynomial regression model using traditional linear least squares techniques, with some care applied in the solution. The multi-input circuit output is expressed in terms of more than one input variables using polynomial coefficients. In the proposed approach, the value of each component of the circuit under test (CUT) is varied within its tolerance limit using Monte-Carlo simulation to calculate its fault free polynomial coefficient bounds. The CUT is then declared fault free or faulty based on the result of the comparison of its estimated polynomial coefficients with the fault free coefficients. To the best of our knowledge, parametric fault detection in multi-input analog circuits using polynomial regression modelling is attempted for the first time in the literature. The effectiveness of the proposed method is demonstrated via two case studies, namely, a lead lag circuit and the PI compensator of a peak-current-mode-controlled buck-type switching converter.

1. Introduction

Due to the wide range of applications of electronic circuits in the recent years, testing of electronic circuits, especially analog circuits is a foremost problem to ensure fault free systems, as there is no simple analog fault model comparable to the digital stuck-at fault model. The accepted analog fault models [1] are catastrophic faults and parametric faults. Many literatures presents several techniques for detecting the faults in analog circuits. D. Binu *et al.* [2] thoroughly surveyed several high-tech techniques for fault detection and diagnosis in electronic circuits. Z. Guo and J. Savir [3] detected parametric faults in the CUT by exploiting an auto regression model to predict the coefficients of the CUT's transfer function, followed by comparison against their precomputed bounds. Z. Guo *et al.* [4] also presented a similar approach to detect parametric faults in passive components of the CUT from its transfer function by imposing minimum and maximum values on the coefficients. The frequency response based fault detection was proposed by Kavithamani A *et al*. [5] considering the fact that the frequency response of a circuit such as bandwidth, high cutoff frequency, low cutoff frequency etc. changes in the presence of faults. Signal Flow Graph (SFG) based approach was proposed by R. Ramadoss *et al*. [1] for detection of parametric fault detection of linear analog circuit where SFGs are inverted, and reverse simulated with good and faulty outputs to obtain test waveforms and component tolerances. Sindia and Agrawal [6, 7] proposed a method of testing for parametric faults in non-linear analog circuits based on a polynomial representation of fault-free function of the CUT, using Taylor series expansion. The response of the CUT is estimated as a polynomial in the root mean square (RMS) magnitude of the applied input voltage at a relevant frequency or DC. The test then classifies the CUT as fault-free or faulty based upon a comparison of the estimated polynomial coefficients with those of the fault-free circuit. X. Li *et al.* [8] presented a novel method that employs the cross-entropy between the good circuit and the bad circuit to detect component faults in analog circuits based on the autoregressive (AR) model.

In almost all literature reported so far till date, the fault detection algorithm for detection of parametric faults has been developed for single-input single-output analog circuits e.g., Sallenkey band pass filter [5, 8], low pass filter [3, 4, 7, 8], leapfrog filter [1, 3, 5] or Elliptic filter circuit [6, 7] where, the Op-amp is configured for single ended operation and the non-inverting input is grounded. In this paper, an utmost effort paid off in parametric fault detection in analog circuits where Op-amp is configured for double ended operation. Moreover, most of the practical analog circuits have limited accessible terminals for excitation and measurement of responses; hence detection of internal parametric faults is difficult. So, we adopt a strategy where we fit a polynomial regression model [9, 10] for the output function (V_{out}) of the circuit as a polynomial of degree n in terms of m independent input variables (voltages) Vin_1, Vin_2 …. Vinm. Classical linear least squares techniques are used to estimate coefficients of a polynomial regression model. In order to simplify the analysis, we further assume that all test measurements taken are noise-free. We also assume that the circuit does not become unstable in the presence of faults and faults occur in passive components only.

The paper is organized as follows: Section 2 outlines brief theory behind estimation of a linear regression in n-dimensions. Section 3 describes the fault detection procedure for analog circuits. Illustrations for validating the proposed algorithm are

detailed in Section 4 and Section 5 concludes the proposed fault detection method.

2. Theory Of Multiple Linear Regression

The function of a circuit can be expressed as a polynomial using a Taylor series expansion [14] in terms of two input voltages Vin_1, Vin_2, about the point $V_{in1} = 0$ and $V_{in2} = 0$ as follows:

$$V_{out}=f(V_{in1}, V_{in2}) = f(0,0) + f_x(0,0)V_{in1} + f_y(0,0).V_{in2} + \frac{1}{2!}[f_{xx}(0,0).{V_{in1}}^2 + 2f_{xy}(0,0).V_{in1}.V_{in2} + f_{yy}(0,0).{V_{in2}}^2] + \ldots\ldots \quad (1)$$

where $f(x,y)$ is a real function of x and y.

Ignoring the higher order terms in (1), we can expand V_{out} up to some n^{th} power of V_{in1}, V_{in2}, which gives us the approximation in (2).

$$V_{out}=a_0 + \sum_{k=1}^{n}\sum_{i=0}^{k} a_{ki}{V_{in1}}^{k-i}{V_{in2}}^{i} + \varepsilon \quad (2)$$

Where a_0, a_{ki} are real valued coefficients $\forall$ $i = 0$ to k and $\forall$ $k = 1$ to n. ε is the truncation error.

The coefficients a_{ki}'s are real functions of circuit parameters, e.g. resistances, capacitances etc. The coefficients a_{ki}'s in Eq. (2) cannot be exact to that of Eq. (1), as Eq. (2) comprises only a finite number of terms for what is essentially a truncated Taylor series. Eq. (2) is a linear regression model that describes the relationship between circuit output voltage Vout and two input voltages Vin1, Vin2. Judicious selection of the coefficients a_0 and a_{ki}'s of a polynomial regression model in (2) using traditional linear least squares techniques minimizes truncation error ε. The accuracy of regression model depends on the degree of the polynomial expansion used in practice. The traditional methods in MATLAB to estimate a linear regression model are already discussed in [15]. In this work, MATLAB *Polyfitn* library [16] is used to solve the coefficients of a polynomial regression model using classical linear least square techniques. Several numerical methods are used to implement *Polyfitn* library. However, to obtain a more stable solution, reasonably efficient QR factorization with pivoting [17] is introduced to build *Polyfitn* library. Any analog circuit in general can be represented using this model. The technique applies equally well to linear and nonlinear circuits.

3. Fault Detection Procedure

For fault detection, we assume that normal parameter variations (normal drift) in a fault-free circuit are within a fraction α of their nominal value, where α << 1. That is, every parameter p_j is allowed to vary within the hypercube $p_{j,nom}(1 - \alpha) < p_j < p_{j;nom}(1 + \alpha)$ $\forall$ j, where $p_{j;nom}$ is the nominal value of the circuit parameter p_j. Any change in the value of one or more parameters of an analog circuit result in a change in one or more coefficient values of its polynomial regression model described by Eq. (2). Due to parametric fault, if the value of any parameter p_j falls outside the hypercube, one or more coefficient values of Eq. (2) slip outside the hypercube $a_{ki,\min} < a_{ki} < a_{ki,\max}$. As a result, we get a different set of coefficients reflecting a detectable fault. Figure 1 outlines the procedure to test the CUT.

3.1 Estimation of Fault-free Polynomial Coefficients

For derivation of polynomial coefficients, the CUT is first simulated in PSpice [18] with nominal value of the circuit components. Using PSpice simulation data for V_{in1}, V_{in2} and V_{out}, a polynomial regression model of the form given by Eq. (2) is obtained using MATLAB *Polyfitn* function. The polynomial coefficients, thus obtained are fault-free coefficients.

3.2 Computation of Fault free Coefficient Bounds

To calculate fault free coefficient bound, the CUT is simulated using Monte-Carlo simulation [19] where each of the circuit parameters varies within the specified tolerance range (± 5%) [8] for which the circuit output is considered to be fault-free and the polynomial coefficients are estimated while the rest of the circuit parameters are kept at their nominal values. Thus, for every circuit parameter p_j, we get fault-free bounds $(a_{ki,\min}, a_{ki,\max})$ of coefficients $a_{ki} \forall\ i, j, k$.

3.3 Fault Modeling and Estimation of Faulty Polynomial Coefficients

It is noteworthy that only single parametric faults are considered in this paper. The operational amplifier used in the circuit is assumed to be fault free. The CUT is fault free when the resistors and capacitor values vary within the tolerance limits (± 5%). To test the CUT, single parametric fault is injected by varying one of the circuit parameters outside its tolerance limits followed by PSpice simulation. Polynomial coefficients of the faulty CUT are estimated using MATLAB *Polyfitn* function.

3.4 Fault Detection

The estimated polynomial coefficients of the faulty CUT are compared with the fault free coefficient bounds. If any of the estimated polynomial coefficients are found to be within its fault free coefficient bounds, the fault is said to be detected. On the contrary, if all of the coefficients are found to fall in the range, no conclusion can be drawn that whether the CUT is faulty or fault free. However, in most of the cases, it is observed that if the CUT passes the polynomial coefficient based fault detection test, the CUT can be declared as fault-free with a higher probability [6].

4. Illustration

To present how the methodology can be used to identify faulty component, here two examples are considered. The first circuit considered is a lead lag circuit [11], and the second circuit is the PI compensator of a peak-current-mode-controlled buck-type switching converter [12, 13]. For both circuits, single parametric fault conditions are simulated and the results are obtained.

4.1 Lead Lag Circuit

The circuit shown in Fig. 2 is an op-amp based lead lag circuit with two inputs. At the inverting input a sinusoidal signal of 100 Hz and amplitude of 2 Volts is applied while at the non-inverting input another sinusoidal signal of 10 Hz and amplitude of 4 Volts are applied.

The nominal values of the circuit components of lead-lag circuit shown in Fig. 2 are- R1 = 1kΩ, R2 = 10kΩ, R3 = 10kΩ, C1 = 0.1595μF, C2 = 1.595μF. The circuit is simulated for 30ms in PSpice with nominal component values and the response of the CUT is shown in the Fig. 3.

It is noteworthy that the output of the lead-lag circuit falls in the non-linear region because in some of the input voltages' range op-amp operates in the saturation region.

4.1.1 Estimation of Fault-free Polynomial Coefficients

Using PSpice simulation data for V_n, V_p and V_{out}, a 6th degree polynomial regression model for lead-lag circuit is derived in terms of its two inputs V_n, V_p. The 6th degree polynomial regression model is simulated in MATLAB as shown in Fig. 4. It may be noted that the response from the derived polynomial regression model matches well with PSpice simulated response.

The 6th degree polynomial results in 28 polynomial coefficients. Among these, first 13 polynomial coefficients are shown in Table 1.

Table 1
Nominal value of the first 13 polynomial coefficients of 6th degree polynomial regression model of lead-lag circuit

Coefficient	A0	A1	A2	A3	A4	A5	A6
Nominal Value	0	0.0002	-0.0006	0.0002	-0.0010	0.0011	-0.0004
Coefficient	A7	A8	A9	A10	A11	A12	
Nominal Value	0.0023	-0.0047	0.0038	-0.0005	0.0042	-0.0124	

4.1.2 Computation of Fault free Coefficient Bounds

To calculate fault free bounds of the polynomial coefficients, the lead-lag circuit is simulated using Monte-Carlo simulation as discussed in Section 3.2. Table 2 shows the fault-free bounds of 13 coefficients A0 to A12 corresponding to each circuit component.

Table 2. Fault free coefficient bound value of the polynomial coefficients A_0 to A_{12}

Parameters	Polynomial coefficient												
	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
R1 max	-0.0381	0.1901	-0.598	0.1394	-0.729	0.973	-0.428	2.949	-6.467	5.107	-0.507	4.385	-12.634
R1 min	-0.0337	0.1979	-0.622	0.1498	-0.8063	1.075	-0.408	2.7843	-6.096	4.9515	-0.5005	4.362	-12.823
R2 max	-0.0366	0.2008	-0.630	0.1354	-0.7118	0.958	-0.3791	2.5509	-5.4649	4.3108	-0.3591	2.7073	-5.812
R2 min	-0.0290	0.1955	-0.617	0.1382	-0.7238	0.9049	-0.3895	2.6157	-5.5546	4.31005	-0.3685	2.8343	-6.445
R3 max	-0.0359	0.1974	-0.613	0.1536	-0.8239	1.1026	-0.3880	2.6263	-5.7111	4.6147	-0.4911	4.2351	-12.245
R3 min	-0.0330	0.1938	-0.608	0.1325	-0.6903	0.8902	-0.4178	2.8566	-6.2149	4.8935	-0.4747	4.0122	-11.106
C1 max	-0.0382	0.2027	-0.625	0.1758	-0.9348	1.2161	-0.3946	2.6678	-5.7848	4.639	-0.5075	4.3541	-12.573
C1 min	-0.0404	0.1886	-0.583	0.1411	-0.7522	1.0316	-0.3682	2.4752	-5.2772	4.0821	-0.4099	3.277	-8.157
C2 max	0	0.2	-0.6	0.2	-0.9	1.1	-0.4	3.1	-6.6	5.0	-0.6	5.0	-15.1
C2 min	0	0.2	-0.6	0.2	-0.9	1.1	-0.4	3.0	-6.5	4.9	-0.60	5.1	-15.5

4.1.3 Fault Modeling and Estimation of Faulty Polynomial Coefficients

To test the lead-lag circuit, single parametric fault is injected by randomly varying each of the circuit parameters outside its tolerance limits followed by PSpice simulation. Polynomial coefficients of the faulty CUT are estimated as shown in Table 3.

Table 3. Various detected single faults

Injected Fault	Estimated Polynomial coefficient													Coefficient status	Fault status
	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12		
R1 12% up	0	0.0001	-0.0003	0.0001	-0.0007	0.0009	-0.0002	0.0012	-0.0012	.0002	-0.0001	0.0003	0.0041	A0-A12	Detected
R1 8 % down	-0.042	0.1786	-0.5646	0.1021	-0.5016	0.688	-0.3869	2.7768	-6.4325	5.2475	-0.3541	2.7006	-6.1762	A0-A6,A9-A12	Detected
R2 9% up	-0.0039	0.1604	-0.5430	0.0995	-0.5203	0.5277	-0.3706	2.5016	-5.2765	4.1495	-0.2511	1.8218	-3.2873	A0-A5,A9-A12	Detected
R2 6% down	0.0687	0.1893	-0.5824	0.1598	-0.8408	1.2922	-0.2854	1.8425	-3.7146	2.7461	-0.3452	2.3466	-3.6946	A0-A12,	Detected
R3 10% up	-0.0514	0.1760	-0.5689	0.1498	-0.7922	1.1597	-0.3324	2.1932	-4.5145	3.4574	-0.3254	2.3122	-4.2586	A0,A3,A8-A12	Detected
R3 7%down	-0.0398	0.1858	-0.5849	0.1368	-0.7116	0.9526	-0.3650	2.4052	-4.9441	3.7066	-0.3573	2.6932	-5.6724	A0,A8-A12	Detected
C1 13% up	-0.0273	0.1464	-0.4566	0.1796	-0.9365	1.1284	-0.2941	1.6915	-2.5864	1.2273	-0.3343	2.3938	-4.1585	A0,A1,A8-A12	Detected
C1 15%down	-0.0690	0.1801	-0.5326	0.0411	-0.1609	0.4191	-0.4382	3.277	-7.9639	6.4713	-0.0371	2.997	-7.7063	A0,A1,A8-A12	Detected
C2 11% up	0	0.0001	-0.0005	0.0001	-0.0004	0.0004	-0.0005	0.0034	-0.0073	0.0054	-0.0005	0.0050	-0.0160	A1,A1,A3,A8-A12	Detected
C2 14%down	-0.0716	0.1598	-0.5191	0.2192	-1.1844	1.7705	-0.1736	0.9597	-1.3851	0.7756	-0.3751	2.5169	-3.9576	A0,A1,A5,A6,A8-A12	Detected

4.1.4 Fault Detection

As per Table 3, each of the circuit components under single parametric fault results in atleast one or all of the first 13 estimated polynomial coefficients to slip outside the fault-free coefficient bounds. So, all parametric faults modelled in this case study of the lead-lag circuit are said to be detected.

4.2 PI Compensator of a Buck Converter

Figure 5 shows the peak current-mode [20] controlled DC–DC buck converter using pulse width modulation (PWM) control IC UC3843 [21]. The working principle of peak-current mode controlled DC–DC buck converter is studied in [22, 23, 24] in details. One of the key functional blocks of the current mode controller is the PI compensator shown in Fig. 6 and constructed using an error amplifier. This is required for regulation of the output voltage. The output voltage, V_{out} of the power stage, is divided through resistor divider network R_{f1} and R_{f2} and then applied to the error amplifier as shown in Fig. 6. The reference voltage V_{REF} = 2.5 V is applied to non-inverting terminal of the error amplifier as a soft-start ramp with rise time 4ms.

The controller is the important part of the converter to maintain the constant output. Therefore, it is very necessary that the controller is designed and tested properly. Our aim is to detect the parametric fault of the controller part of the Buck converter circuit. Figure 6 shows the discrete PI compensator of the Buck converter circuit.

The nominal values of the circuit components of the PWM controller circuit shown in Fig. 6 are: R_{f1}=9.76 kΩ, R_{f2}=3.25 kΩ, R_1 = 1kΩ, C_{hf}=30pF, C_{comp}=2nF, R_{comp1} =10 MΩ, R_{comp}=80 kΩ. The buck converter circuit is simulated for 1.5 ms in PSpice with nominal component values and the response of the PWM controller circuit is shown in the Fig. 7.

4.2.1 Estimation of Fault-free Polynomial Coefficients

Using PSpice simulation data for V_{COMP}, V_{out} and V_{REF}, a 5th degree polynomial regression model for PI controller circuit is derived in terms of its two inputs V_{out} and V_{REF}. The 5th degree polynomial regression model is simulated in MATLAB as shown in Fig. 8. The experimental result shows that the 5th degree polynomial gives the best match with PSpice simulated response of the controller circuit.

The 5th degree polynomial results in 21 polynomial coefficients shown in Table 4.

Table 4
The nominal value of the polynomial coefficients K0 to K21

Coefficient *10^{+7}	**K0**	**K1**	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
Nominal Value	0.0019	-0.035	0.0008	0.2556	-0.0114	0.0001	-0.904	0.0631	-0.0012	0	1.593
Coefficient *10^{+7}	**K11**	**K12**	**K13**	**K14**	**K15**	**K16**	**K17**	**K18**	**K19**	**K20**	
Nominal Value	-0.151	0.005	-0.0001	0	-0.9415	0.131	-0.006	0.0002	0.0000	-0.0000	

4.2.2 Computation of Fault free Coefficient Bounds

To calculate fault free bounds of the polynomial coefficients, PI controller of the buck converter is simulated using Monte-Carlo simulation as discussed in Section 3.2. Most of the parametric faults in the PI controller circuit are detected using first 13 coefficients. Table 5 shows the fault-free bounds of the first 13 coefficients K0 to K12 corresponding to each circuit component.

Table 5. Fault free coefficient bound K_0 to K_{14} for the controller circuit

Component	Polynomial Coefficient $*10^{+7}$												
	K0	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12
R_{f2} max	0.0019	-0.034	0.0007	0.249	-0.0112	0.0001	-0.881	0.0617	-0.0012	0	1.489	-0.1482	0.0049
R_{f2} min	0.0018	-0.036	0.0008	0.2631	-0.0117	0.0001	-0.929	0.06450	-0.0013	0	1.557	-0.1541	-0.0051
R_{f1} max	0.0019	-0.035	0.0008	0.2567	-0.0115	0.0001	-0.907	0.0633	-0.0012	0	1.5244	-0.1515	-0.005
R_{f1} min	0.0019	-0.035	0.0008	0.2556	-0.0114	0.0001	-0.904	0.0631	-0.0012	0	1.5204	-0.1512	-0.005
R_1 max	0.0018	-0.035	0.0008	0.2531	-0.0113	0.0001	-0.895	0.0624	-0.0012	0	1.5049	-0.1495	0.0049
R_1 min	0.0019	-0.035	0.0008	0.2582	-0.0115	0.0001	-0.913	0.0637	-0.0013	0	1.5345	-0.1525	0.0050
R_{compl} max	0.0019	-0.035	0.0008	0.2557	-0.0114	0.0001	-0.904	0.0631	-0.0012	0	1.5199	-0.1511	0.0050
R_{compl} min	0.0019	-0.035	0.0008	0.2556	-0.0114	0.0001	-0.904	0.0631	-0.0012	0	1.5194	-0.1510	0.0050
R_{comp} max	0.0019	-0.036	0.0008	0.2648	-0.0119	0.0001	-0.936	0.0655	-0.0013	0	1.5730	-0.1566	0.0052
R_{comp} min	0.0018	-0.033	0.0007	0.2464	-0.0110	0.0001	-0.872	0.0607	0.0012	0	1.4655	-0.1454	0.0048
C_{comp} max	0.0019	-0.035	0.0008	0.2557	-0.0114	0.0001	-0.904	0.0631	-0.0012	0	1.5197	-0.1511	0.0050
C_{comp} min	0.0019	-0.035	0.0008	0.2552	-0.0114	0.0001	-0.905	0.0631	-0.0012	0	1.5205	-0.1510	0.0050
C_{hf} max	0.0019	-0.035	0.0008	0.2565	-0.0115	0.0001	-0.907	0.0633	-0.0012	0	1.5240	-0.1515	0.0050
C_{hf} min	0.0018	-0.035	0.0008	0.2549	-0.0114	0.0001	-0.901	0.0628	-0.0012	0	1.5153	-0.1505	0.0050

Table 6. Various detected single fault using the coefficient K_0 to K_{14} of the controller circuit

Fault Injected	Polynomial Coefficient $*10^{+7}$												
	K0	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12
R_{f2} 5.8% up	0.0018	-0.0339	0.0007	0.2486	-0.0111	0.0001	-0.8806	0.0616	-0.0012	0	1.4845	-0.1479	0.0049
R_{f2} 6% Down	0.0019	-0.0360	0.0008	0.2637	-0.0117	0.0001	-0.9308	0.0647	-0.0013	0	1.5598	-0.1544	0.0051
R_{f1} 7% up	0.0019	-0.0349	0.0008	0.2558	-0.0114	0.0001	-0.9042	0.0630	-0.0012	0	1.5186	-0.1507	0.0050
R_{f1} 8.5% down	0.0019	-0.0348	0.0008	0.2555	-0.0115	0.0001	-0.9054	0.0636	-0.0013	0	1.5277	-0.1526	0.0051
R 6% up	0.0018	-0.0345	0.0007	0.2527	-0.0113	0.0001	-0.8936	0.0623	-0.0012	0	1.5021	-0.1492	0.0049
R 5.5 % down	0.0019	-0.0353	0.0008	0.2585	-0.0115	0.0001	-0.9319	0.0638	-0.0013	0	1.5360	-0.1527	0.0051
R_{comp} 9% up	0.0020	-0.0372	0.0008	0.2722	-0.0122	0.0001	-0.9617	0.0674	-0.0013	0	1.6160	-0.1610	0.0053
R_{comp} 6.8% down	0.0018	-0.0331	0.0007	0.2431	-0.0108	0.0001	-0.8603	0.0598	-0.0012	0	1.4462	-0.1434	0.0047
C_{hf} 8% up	0.0019	-0.0351	0.0008	0.2570	-0.0115	0.0001	-0.9084	0.0634	-0.0012	0	1.5266	-0.1518	0.0050
C_{hf} 10% down	0.0018	-0.0347	0.0008	0.2541	-0.0113	0.0001	-0.8987	0.0626	-0.0012	0	1.5109	-0.1500	0.0050
R_{compl} 7.5% up	0.0019	-0.0349	0.0008	0.2559	-0.0114	0.0001	-0.9408	0.0631	-0.0012	0	1.5207	-0.1511	0.0050
R_{compl} 5.6% down	0.0019	-0.0349	0.0008	0.2556	-0.0114	0.0001	-0.9037	0.0630	-0.0012	0	1.5119	-0.1510	0.0050
C_{comp} 10% up	0.0019	-0.0350	0.0008	0.2554	-0.0114	0.0001	-0.9032	0.0631	-0.0012	0	1.5185	-0.1511	0.0050
C_{comp} 6% down	0.0019	-0.0349	0.0008	0.2557	-0.0114	0.0001	-0.9046	0.0631	-0.0012	0	1.5202	-0.1510	0.0050
C_{comp} 8% down	0.0019	-0.0349	0.0008	0.2559	-0.0114	0.0001	-0.9051	0.0631	-0.0012	0	1.5210	-0.1510	0.0050

4.2.3 Fault Modeling and Fault Detection by Estimation of Faulty Polynomial Coefficients

To test the PI controller circuit, single parametric faults are injected randomly followed by PSpice simulation of faulty circuit. Polynomial coefficients of the faulty CUT are estimated as shown in Table 6. All parametric faults except – 5.6% and – 6% variation in R_{comp1} and C_{comp} respectively are detected using first 13 coefficients. These two faults can be detected by considering the rest 8 coefficients, i.e. K13 to K20. Fault free bound of these 8 coefficients is shown in Table 7. Table 8 shows the faulty values of coefficients, i.e. K13 to K20 after injecting parametric faults.

Table 7
Fault free bounds of K13 to K20 for R_{comp1} and C_{comp}

Component	Polynomial Coefficient $*10^{+07}$							
	K13	K14	K15	K16	K17	K18	K19	K20
R_{comp1} max	-0.0001	0.000	-0.9419	0.1313	-0.0068	0.0002	0.000	-0.000
R_{comp1} min	-0.0001	0.000	-0.9414	0.1312	-0.0068	0.0002	0.000	-0.000
C_{comp} max	-0.0001	0.000	-0.9418	0.1313	-0.0069	0.0002	0.000	-0.000
C_{comp} min	-0.0001	0.000	-0.9417	0.1312	-0.0068	0.0002	0.000	-0.000

Table 8
Faulty Coefficients K13 to K20 for single parametric faults in R_{comp1} and C_{comp}

Fault Injected	Polynomial Coefficient $*10^{+07}$								Coefficient out of bound	Fault Status
	K13	K14	K15	K16	K17	K18	K19	K20		
R_{comp1} 5.6% down	-0.0001	0	-0.9413	0.1312	-0.0068	0.0002	0	-0.00	K15	Detected
C_{comp} 6% down	-0.0001	0	-0.9415	0.1312	-0.0068	0.0002	0	-0.00	K15	Detected

5. Conclusion

We have described a polynomial coefficient based test method to detect the existence of parametric faults in multi-input analog circuits, where signals are applied to more than one input. Our test procedure uses an estimation of polynomial coefficients of linear regression modelling followed by a determination of whether or not any of the coefficients is outside the fault-free range imposed by the circuit-parameter drifts. If any of the coefficients is found to be outside its prescribed fault-free range (tolerance box), the CUT is declared faulty. The advantage of this approach is that any component fault can be detected without circuit augmentation. Although, we have successfully demonstrated our test method for detecting single parametric faults only, this method is well applicable for detection of catastrophic faults too. The proposed approach is validated with the help of two case studies where some part of the output voltage V_{out} falls in the non-linear region. We have chosen 6th degree polynomial for lead-lag circuit and 5th degree polynomial for PI controller circuit of buck converter. High order polynomials often suffer from severe ringing between the data points. Moreover, with the increase in

order of the polynomial, the number of coefficient increases and makes the fault detection procedure more complex. So, judicious selection of order of polynomial model is one of the key aspects in our proposed method which can be further explored. It may be noted that some of the parametric faults are sensitive to only fewer number of polynomial coefficients. As a result, those circuit-parameter drifts may not be captured by most of the coefficients which occur in case of PI Compensator of a Buck Converter. The proposed approach can be extended for fault diagnosis by exploiting the sensitivity of polynomial coefficients to circuit parameters.

Declarations

Data availability statement

All data generated or analysed during this study are included in this article.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Author Contributions Statement

Author Anjali Rai conducted simulation, formal analysis and wrote original draft. Author Rahul Bhattacharya provided necessary resources, validated the results and edited the manuscript. Both the authors reviewed the final manuscript.

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Figures

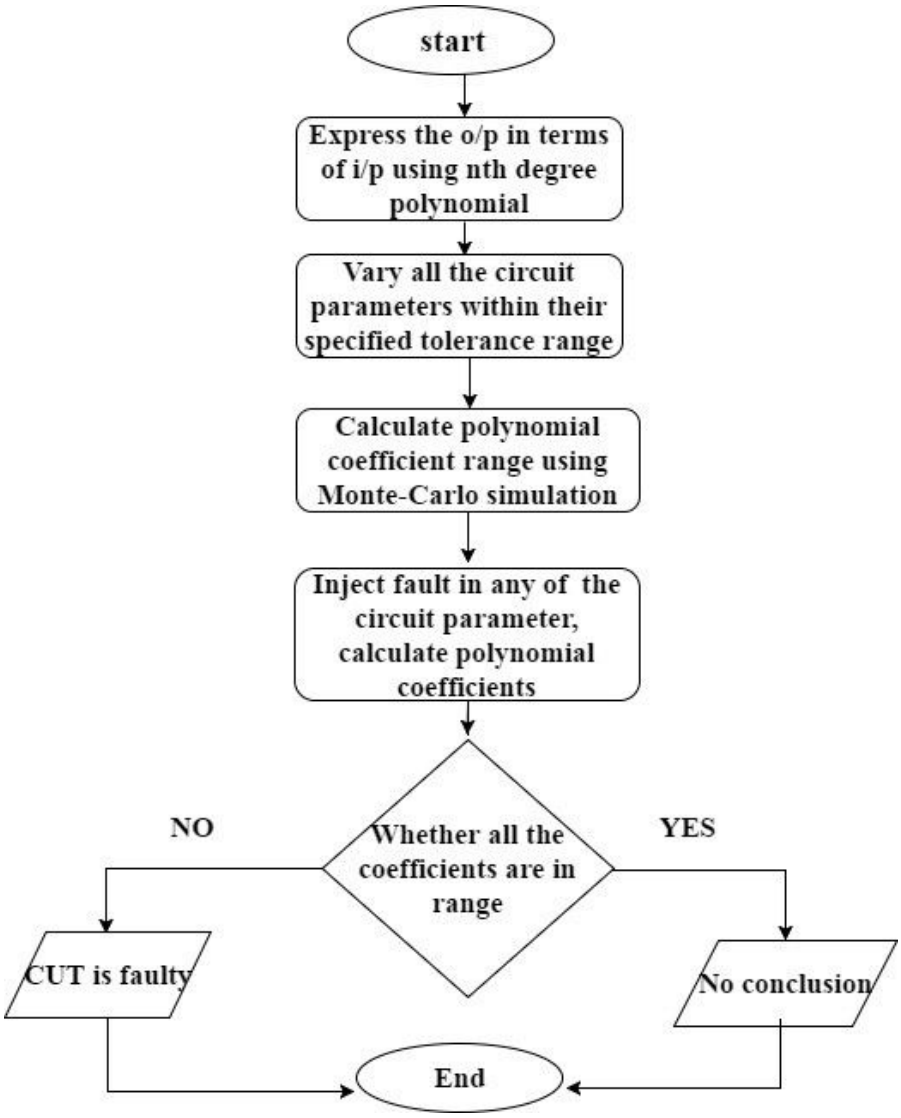

Figure 1

Flow chart of fault detection stage

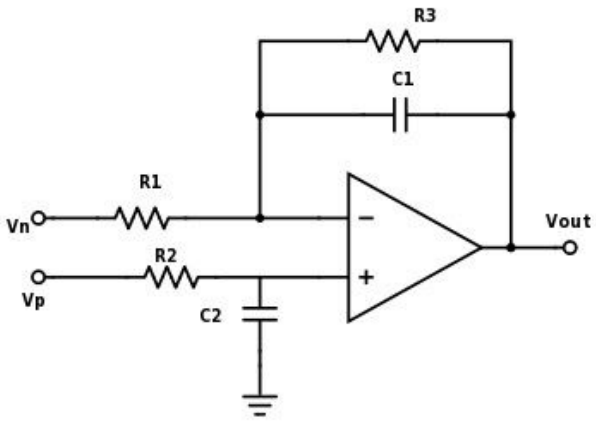

Figure 2

Lead-lag circuit with two low-pass filters.

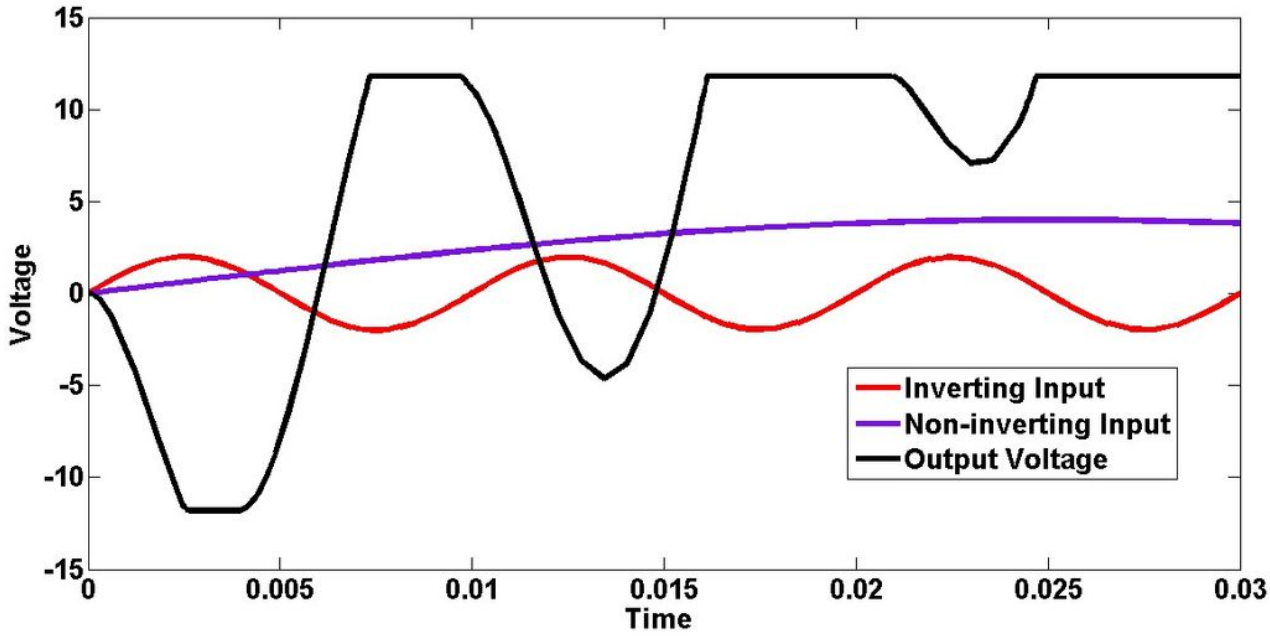

Figure 3

Response of lead-lag circuit simulated in PSpice.

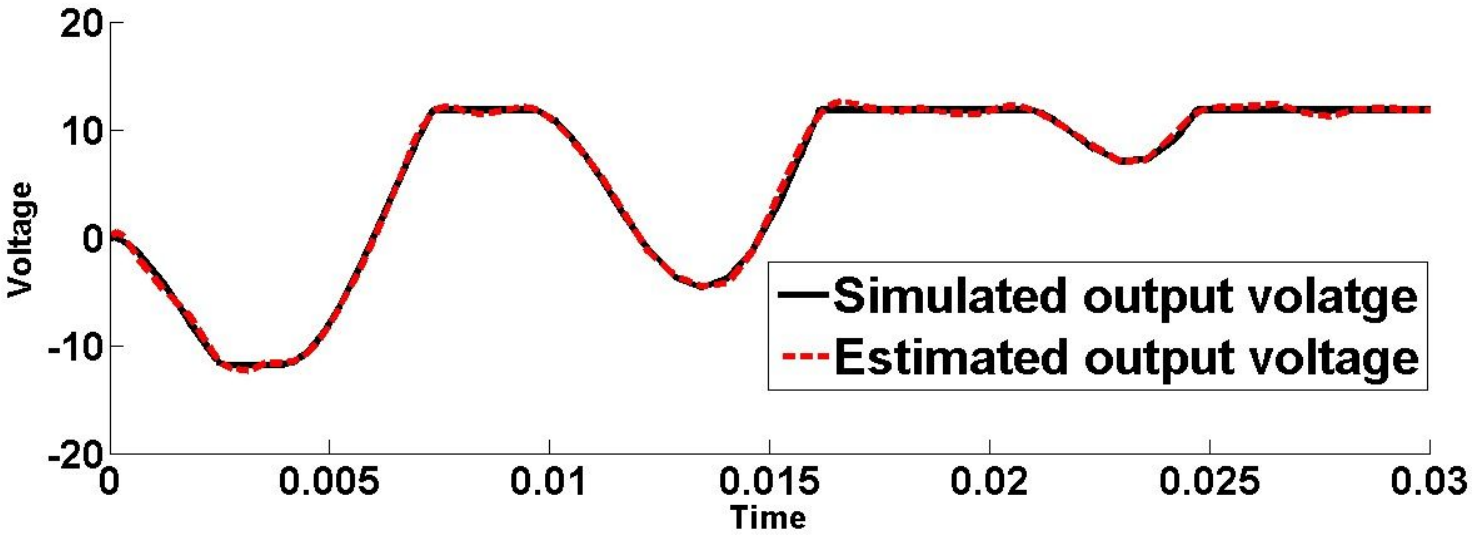

Figure 4

Simulated response of 6th degree polynomial regression model of lead-lag circuit.

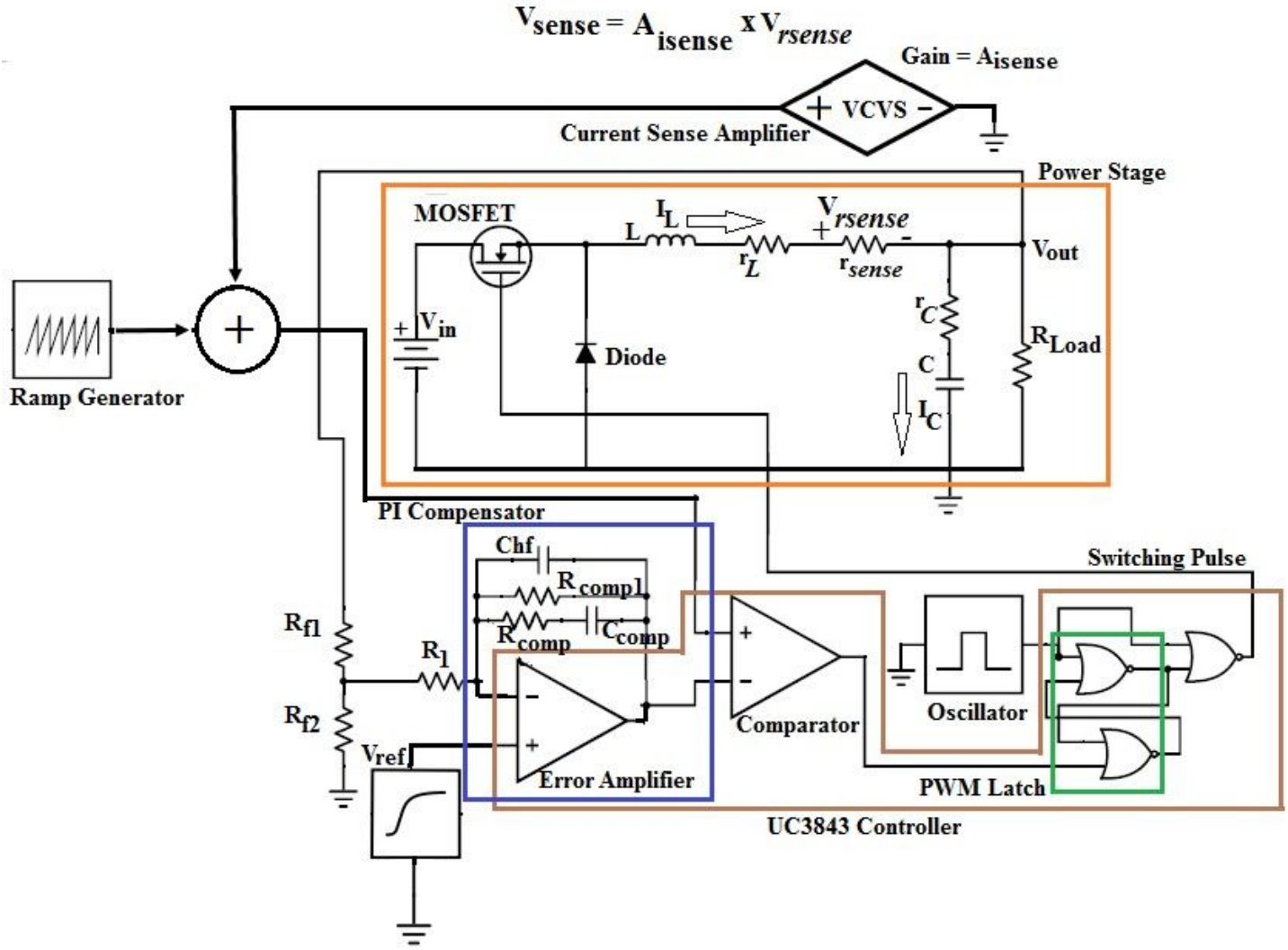

Figure 5

Schematic of a current programmed control buck converter [22-24].

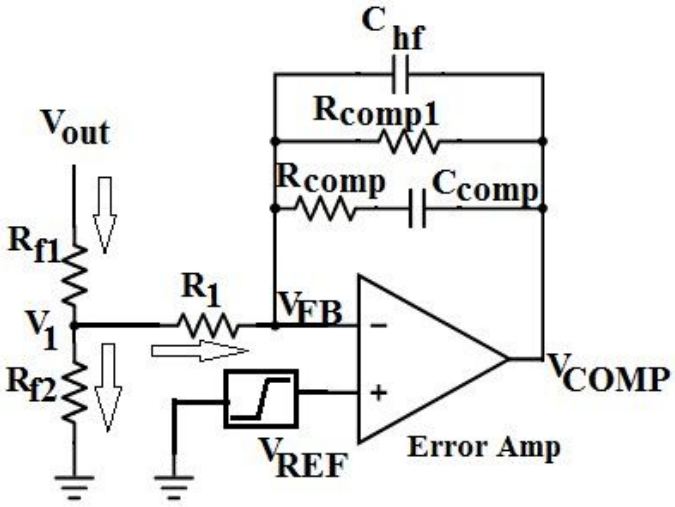

Figure 6

PWM controller circuit of buck converter [20, 22-24].

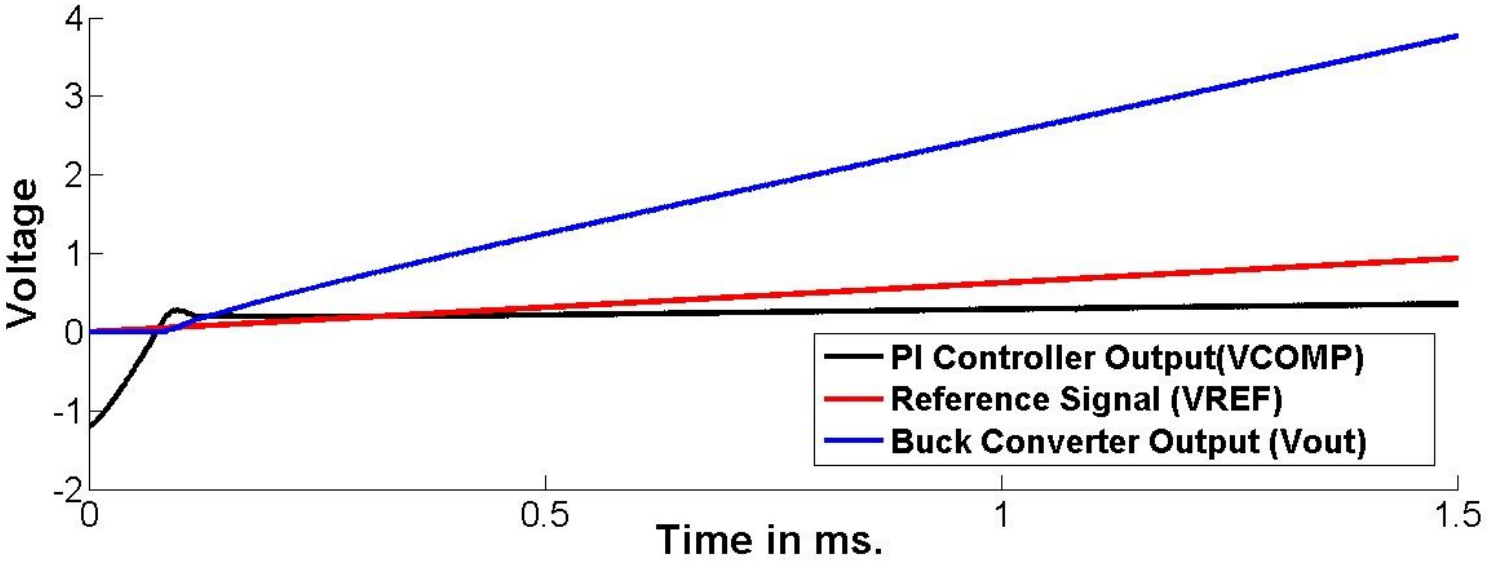

Figure 7

Response of Buck converter and PWM controller circuit simulated in PSpice.

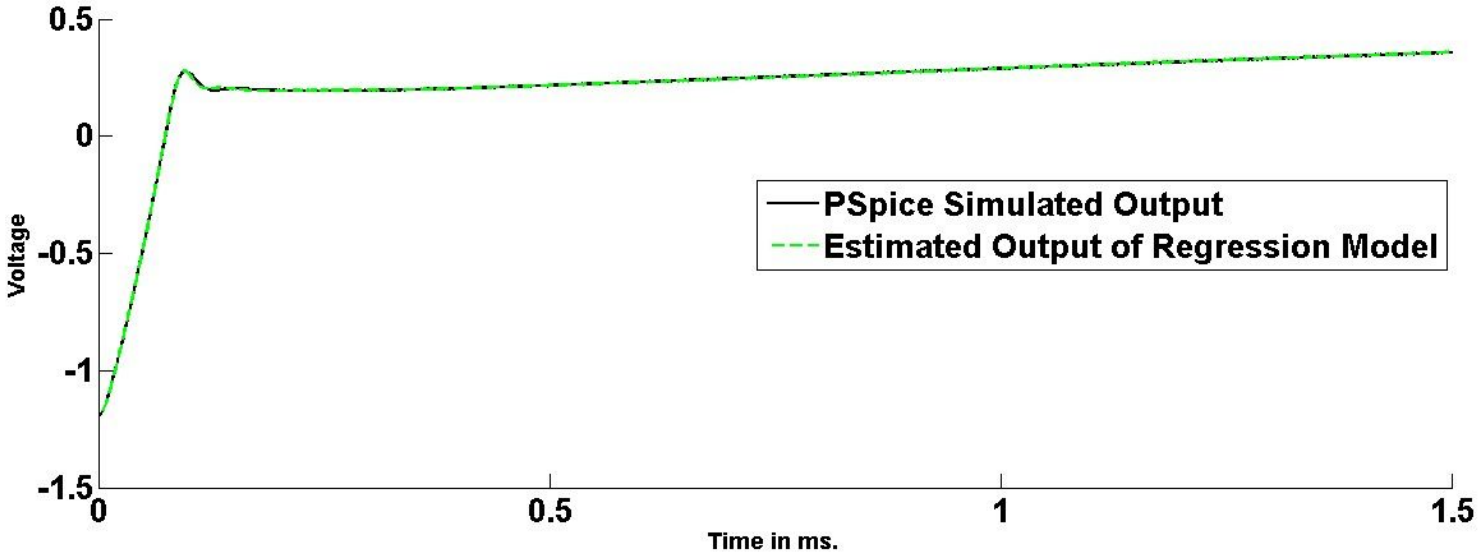

Figure 8

Response of controller circuit with 5th degree polynomial.