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Research Article

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A Design of 45nm Low Jitter Charge Pump Phase-Locked Loop Architecture for VHF and UHF Fields

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Abstract

Phase-locked loop has contributed significantly toward the technological advancement in data transmission and communication. In addition, many recent studies in Phase-locked loop schemes combined with novel integrated circuit technology have made Phase-locked loop devices become essential system components. This work designed a Phase-locked loop with an input voltage of 1.0 V, which is researched on the 45 nm NCSU PDK with Cadence Virtuoso tools to gain output frequency over 800 MHz and low jitter of 150 ps. Furthermore, the proposed procedure uses Ocean language to analyze the variation of Phase-locked loop parameters in this work, including output voltage, operating frequency, and phase jitter.

Keywords: Charge-Pump Phase-Locked Loop (CPPLL), Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Current Starved-Voltage Controlled Oscillator (CS-VCO), CMOS Technology, Ocean Language.

1 Introduction

Phase-Locked Loop (PLL) has been used in many high-speed designs, such as the microprocessors in communication systems, the frequency multiplication, and the frequency recovery of receive systems [1]. In the integrated circuits (IC) design field, the main applications of PLL are generating and synchronizing the high-frequency signal from the reference source [2]. Moreover, the PLL decreases the skew of the external frequency source; thus, it is also used as a clock recovery system in the data communications field [3]. A Charge-Pump Phase-Locked Loop (CPPLL) architecture was applied in the PLL design process to prioritize overcoming the problem with the skew of signal because this architecture has been realized widely in discrete form, a wide frequency range, low jitter, and small locking phase error [4, 5]. Thank to these properties, CPPLL would offer wide use in high-performance integrated circuits. Furthermore, thank to technological advancements and demands in high packing density, high speed, and low power integrated chips, CPPLL has been becoming a trend study [6].

In studying the CPPLL, the jitter parameter should be concerned primarily. Jitter is represented by the deviation of zero crossings of a periodic waveform and its ideal points on the time axis. The deviation of zero crossings of the waveform synthesized by the PLL could break the setup and hold time violations in digital circuits. Moreover, the setup and hold time violations lead to data transmission errors and functionality failure of the whole chip [7, 8]. Therefore, jitter plays a vital role in PLL research because of its severe effects on the quality of PLL [9]. Consequently, in this work, our architecture with Current Starved Voltage Controlled Oscillator (CS-VCO) is proposed in circuit design to reduce jitter effectively. This proposal is our first contribution.

The next one would be related to the problem of CPPLL design implementation. Conventional analog IC design is mainly time-consuming due to the complicated non-linear relationship between the design parameters and specifications. Typically, hand calculations may facilitate the design process of analog IC, provide a good starting point for the designer and significantly narrow the design space. Nevertheless, design time still depends on the experience of the designer, who performs a huge number of iterative simulations to achieve the targeted design specifications. These simulations are conducted manually on many CAD tools, such as Spectre, HSPICE. Thus, the CPPLL design process takes the design time too long to meet the targeted specifications, including jitter, output voltage, and frequency. In addition, the approximation errors and the complex circuit analysis process increase dramatically in the design time [10].

Meanwhile, the Ocean language is built as an extension of the Skill language, which is used to control and conduct the simulation tests automatically in the analog IC design field. This language is not only integrated into CAD tools, but the language also generates automatically the simulation results file as the *.lib file format. With these properties, the Ocean language would help the analog designers conduct the design and simulation circuits to achieve the

targeted specification easier than the conventional IC design flow [11]. Consequently, a flow using Ocean language to study the parameters variation of the CPPLL will significantly reduce the implementation time. Therefore, the second contribution of our work is proposing the design flow using Ocean language to overcome the CPPLL design implementation problem.

The remainder of this paper is organized as follows. Firstly, in section 1, our proposed schematic design of CPPLL is presented, which is designed with CS-VCO. Next, the detailed flow for the transistor-level design of CPPLL applying Ocean language is briefly illustrated. Meanwhile, our simulation results based on 45nm NCSU PDK and analysis are demonstrated in section 4. Finally, the conclusion is given in section 5.

2 The Proposed CPPLL Design

In this section, the implemented schematic design of CPPLL is shown. Overall, the CPPLL has five components, including Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO) and Divider [12]. The CPPLL generates the cyclic output signal Φ_{out} from the input signal Φ_{in} [4]. First, the Φ_{in} is taken from the crystal oscillator. Next, the PFD generates voltage signal V_{PFD}, which is linearly proportional to the difference between Φ_{in} and Φ_{out} (Δ_{Φ}). CPPLL is locked when either Φ_{in} and Φ_{out} are aligned or $\Delta_{\Phi} = 0$. Subsequently, V_{PFD} was charged in the CP for producing voltage signal V_{CP} to the VCO. Unfortunately, the voltage signal V_{CP} consists of dc component (preferable to the VCO function) and high-frequency component (undesirable need to remove). Therefore, the LPF had to keep the dc level to the VCO and suppress the high frequency level. Since the VCP has been filtered by the LPF, the VCO is able to start oscillating with the voltage control V_{con}. Finally, the center frequency value of output signal is affected by both VCO architecture and value of voltage controlled V_{con}. Also, the output frequency is divided by the N factor of the feedback channel to the PFD for matching Φ_{out} and Φ_{in} in the locked state. The block diagram of CPPLL is presented clearly in the figure 1. Depending on the application of CPPLL, the topology of each cell is chosen accordingly [13].

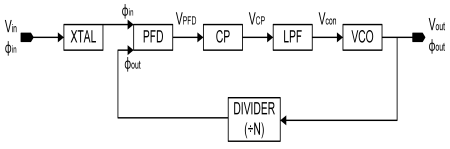

Fig. 1 Block diagram of Charge Pump Phase Locked Loop

Specifically, integrated circuits are applied widely in the VHF and UHF radio frequency bands, so the demand of PLL design whose output frequency is stable in these bands significantly [14]. Thus, our CPPLL is designed appropriately with an output frequency range from 500 MHz to 800 MHz. In this

paper, the proposed schematic PFD consists of D Flip-Flop positive cells (DFF positive) and 1 NAND2 cells, shown in figures 2.

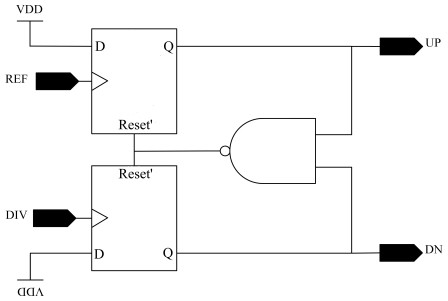

Fig. 2 Our schematic of PFD cell

The gain of the PFD is formulated by:

$$K_{PFD} = \frac{V}{2 \times \pi}, V = \overline{V_{UP} - V_{DN}} \tag{1}$$

Next, CP architecture is illustrated in figure 3. After design the CP, the loop filter consists of a single resistor $R_0 = 100$ kΩ and two capacitors $C_0 = C_1 = 1$ pF. Capacitance C_1 parallel with C_0 and R_0 are connected in series. Its function is used to filter the high-frequency noise out of the PLL. The transfer function of the loop filter is:

$$LF(s) = \frac{s + \frac{1}{R_0 \times C_0}}{C_1 \times s^2 \times (s + \frac{C_0 + C_1}{R_0 \times C_1 \times C_2})} \tag{2}$$

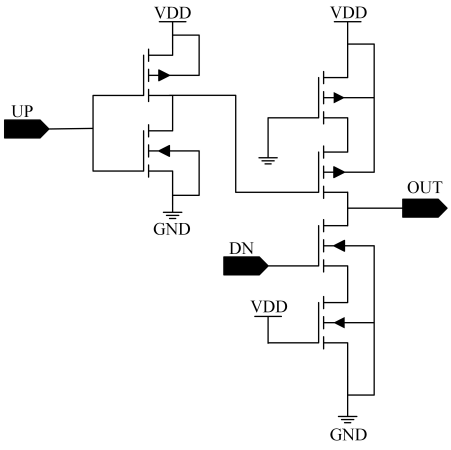

Fig. 3 Schematic of proposed CP cell

Once the design of both the CP and LPF have been finished, the range of changing voltage signal V_{con} is calculated by:

$$\Delta V_{con} = \frac{I_{CP}}{C_0} \times \frac{\Delta_\Phi}{2 \times \pi} \times T \tag{3}$$

With T is a period of Φ_{in} signal and Δ_Φ is a difference between Φ_{in} and Φ_{out}. The average charge dumped per cycle is:

$$Q_{con} = \frac{C_0 \times \Delta V_{con}}{T} = \frac{I_{CP}}{2 \times \pi} \times \Delta_\Phi \tag{4}$$

Thus, the PFD and charge pump are modeled together by the following relation in the locked state:

$$K_{PFD} = \frac{I_{CP}}{2 \times \pi} \tag{5}$$

Types of VCO are concerned widely: LC oscillator VCO (LC-VCO) and Current Starved VCO (CS-VCO) [15]. LC oscillator performs better phase noise than CS-VCO, but its area is extremely large, and its tuning range is limited because of the LC oscillator. Thus, this architecture is rarely applied for IC design. While CS-VCO has many advantages, including its tuning range is much larger due to the Ring oscillator, and its area is very less than LC-VCO [16]. Therefore, the CS-VCO architecture is used in this work and illustrated in figure 4. In detail, the three stages CS-VCO is used to get the desired result [17].

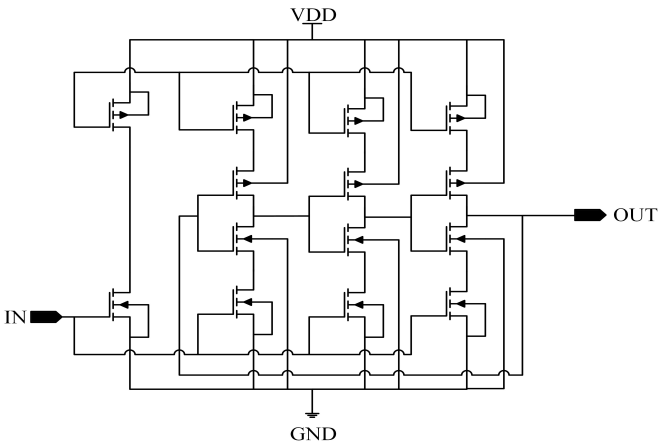

Fig. 4 Our schematic of three-stage CS-VCO cell

The transfer function of the VCO is given as:

$$VCO(s) = \frac{K_{VCO}}{s} \tag{6}$$

The total capacitance on the drain terminal is given by equation:

$$C_{tot} = C_{out} + C_{in} = \frac{5}{2} \times C_{out} \times (W_P \times L_P + W_P \times L_P) \tag{7}$$

And oscillation frequency can be calculated by following formula:

$$f_{osci} = \frac{1 \times T_{Delay}}{N} \tag{8}$$

With $(W/L)_N$ and $(W/L)_P$ ratio of each CMOS transistor, C_{OX} is gate oxide capacitance, T_{Delay} delay of each inverter stage, and N is the number of inverter stages in VCO. Therefore, the center frequency is affected by the (W/L) ratio. Next, the Divider is designed with the N factor = 8 to match Φ_{out} and Φ_{in} in the locked state for this work. Hence, the divider consists of three DFF positive connected in the manner shown in figure 5.

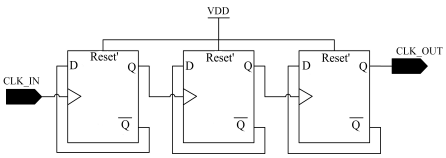

Fig. 5 Our schematic of the DIV cell

Finally, our proposed schematic design of CPPLL is linked by Charge Pump, Phase Frequency Detector, Low Pass Filter and Divider circuit, which is shown in figure 6, and its transfer function is given by following formula:

$$CPPLL(s) = K_{PFD} \times K_{VCO} \times \frac{s + \frac{1}{R_0 \times C_0}}{C_1 \times s^2 \times (s + \frac{C_0 + C_1}{R_0 \times C_1 \times C_2})} \tag{9}$$

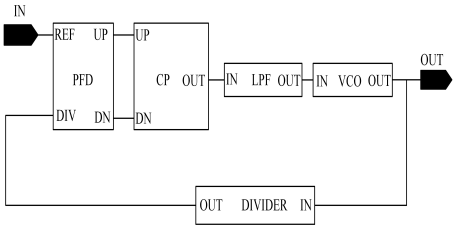

Fig. 6 Schematic of the proposed CPPLL

Our proposed architecture is designed with 45 nm NCSU PDK. In the next section, simulation results and evaluations for this proposed CPPLL are presented distinctly.

3 Design Process Of CPPLL

The detailed flow using Ocean language is proposed in this section. Due to the absence of a model for the accurate measurement of parameters in the circuit, it has led the circuit designer to define and explore the new designs using various optimization and simulation methods. The process of analog circuit design consists of three major tasks: (1) selection of topology, (2) sizing of components, and (3) guaranteeing cells meet specifications [11]. If the complexity of the circuits increases, the design time also increases. In work [18], to design a NAND2 cell and extract its parameter for guaranteeing cells meet specifications, they did manually 7x7 simulations and 49x6 calculations to generate all parameters [18]. This process in work [18] becomes an excessive time-consuming task for the designer to obtain the optimal design parameters. Therefore, in this paper, using the Ocean language is proposed to solve problems of running many simulations manually. The flow automatically performs parametric simulations of each logic cell and generates output parameters with the format as the liberty file, which is presented in figure 7.

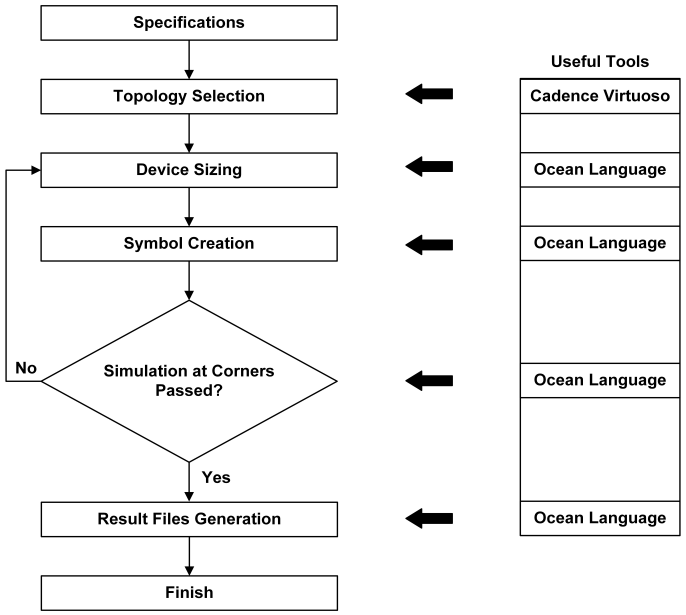

Fig. 7 Our proposed flow to design transistor level of CPPLL.

The below pseudo-code conducts the design flow of NAND2 cell with our flow to generate the lookup table 7x7 format as *.lib file.

Pseudo-code of the design flow using Ocean language:

1: Read C_{Load}
$(2 \times 10^{-15}, 5 \times 10^{-15}, 6 \times 10^{-15}, 7 \times 10^{-15}, 8 \times 10^{-15}, 9 \times 10^{-15}, 9.5 \times 10^{-15})$

2: Read Risetime
$(1 \times 10^{-11}, 2 \times 10^{-11}, 4 \times 10^{-11}, 6 \times 10^{-11}, 8 \times 10^{-11}, 9 \times 10^{-11}, 9.5 \times 10^{-11})$
3: Read Falltime
$(1 \times 10^{-11}, 2 \times 10^{-11}, 4 \times 10^{-11}, 6 \times 10^{-11}, 8 \times 10^{-11}, 9 \times 10^{-11}, 9.5 \times 10^{-11})$
4: Set Slope = Risetime = Falltime
5: Read VDD(1)
6: Read Temperature(27)
7: Read the netlist file of design
8: Read the Spectre model file
9: Create simulation results folder
10: Open this folder
11: For every the C_{load} value
12: For every the Risetime/Falltime value
13: Conduct simulation
14: Read data
15: Plot data
16: Calculate parameters
17: Printf parameters
18: End For
19: End For

4 Simulation Results Of Proposed CPPLL

4.1 Simulation setup: testbench, parameter boundaries

In this section, the parameters of the proposed CPPLL are presented and analyzed after the design process. The simulation process of the proposed CPPLL is conducted by the Spectre tools. For investigating CPPLL optimization, the simulation environment should be regarded carefully with the change of both CPPLL input and output. Therefore, the testbench circuit chooses input parameters to combine with: input oscillator is 20 MHz, the operating voltage is 1 V and temperature 27 ^0C. In addition, simulation environments use the capacitance load C_{load} (2 fF, 5 fF, 6 fF, 7 fF, 8 fF, 9 fF, 9.5 fF), Risetime and Falltime of input waveform V_{slope} (0.01 ns, 0.02 ns, 0.04 ns, 0.06 ns, 0.08 ns, 0.09 ns, 0.095 ns) to analyze the important parameter variations including operating frequency, output voltage and jitter. On the other hand, these simulation models can assess the quality of CPPLL in many cases, which is used to design CPPLL for practical application. Our testbench circuit is shown in figure 8.

After the PLL transient has been simulated by Spectre, its simulation results are presented in figure 9. Following that, the important parameters of proposed CPPLL simulated by Ocean language are shown in following figures from 10 to 13 and table 1.

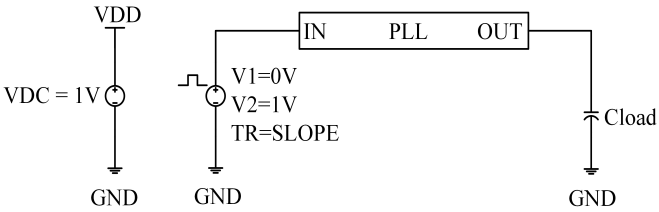

Fig. 8 Our testbench circuit of CPPLL.

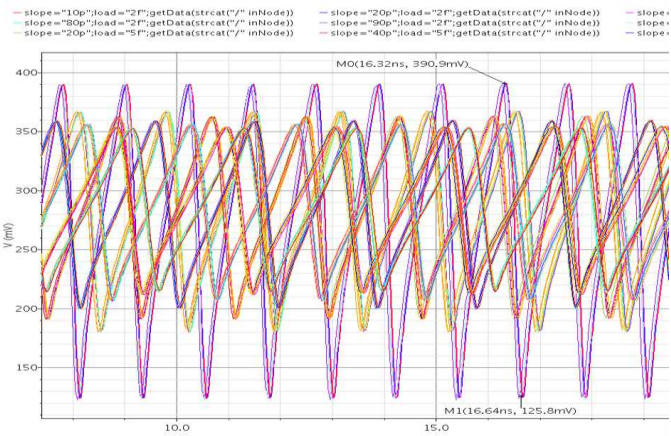

Fig. 9 Simulation results of CPPLL after characterization in this work.

4.2 Parameters Of Proposed CPPLL

4.2.1 Operating Frequency

Initially, the values of an operating frequency of CPPLL are demonstrated in figure 9. Based on the figure 10, when C_{load} rises from 2 fF to 9.5 fF, the operating frequency drops from from 467.29 MHz to 877.93 MHz. In contrast, while C_{load} = 2 fF and V_{slope} increase from 10^{-11} to 9.5×10^{-11}, the operating frequency gains from 855 MHz to 877 MHz. Therefore, the operating frequency is directly proportional to V_{slope} and inversely proportional to C_{load}. In our study, with C_{load} = 2 fF and V_{slope} = 0.095 ns, the frequency gains the best values of 877.93 MHz. On the other hand, the frequency gets the low value of 467.29 MHz with C_{load} = 9.5 fF and V_{slope} = 0.01 ns. Absolutely, these results are applied successfully in both Very High Frequency (VHF) and Ultra High Frequency (UHF) fields such as cell phone, GPS, and navigation aids.

4.2.2 Output Voltage

Next, figures 11 and 12 show minimum and maximum output voltage values of CPPLL, respectively. The output voltage range got from 0.1256 V to 0.3932 V when the input voltage is 1 V. Definitely, the output voltage decreases

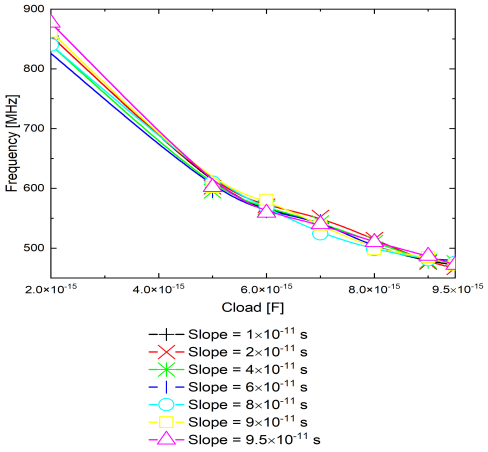

Fig. 10 Frequency variation with C_{load} and V_{slope} variable

70% compared to the input voltage. Regarding the minimum value of output voltage, this value increases from 0.1256 V to 0.219 V when C_{load} rises from 2 fF to 9.5 fF. In contrast, the maximum value of output voltage, this value decreases from 0.3932 V to 0.365 V when C_{load} rises from 2 fF to 9.5 fF. While V_{slope} climbs from 10^{-11} s to 9.5×10^{-11} s, output voltage is constant. Consequently, it supports the idea that the dynamic output power can be decreased in CPPLL architecture. Moreover, these values of the output voltage can be applied in different designs, which use the low threshold voltage to turn on. This parameter should be designed carefully to drive load circuits and save the dynamic power of PLL.

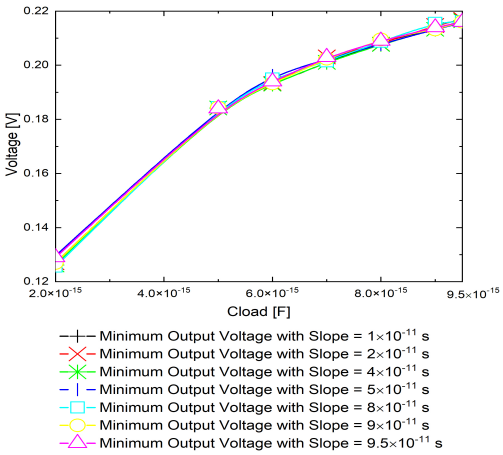

Fig. 11 Minimum output voltage variation with C_{load} and V_{slope} variable

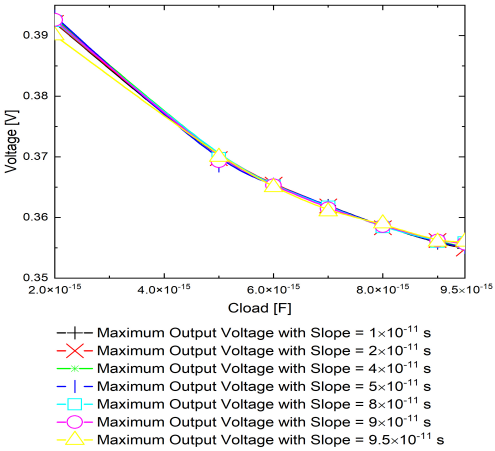

Fig. 12 Maximum output voltage variation with C_{load} and V_{slope} variable

4.2.3 Jitter

Following the output voltage, the values of the jitter parameter are shown in figure 13. Jitter should be supervised carefully in sequential circuits which use the periodic clock to process many tasks in special designs, such as CPU, GPU, Memory. In this work, the jitter varies from 115.7 ps to 1293.3 ps, which depends on input and output of the CPPLL design, including the slope of input signal and output capacitance. Our results pointed to the possibility that jitter is affected by both input and output in many cases. For example, at the same condition: C_{load} = 9.5 fF and the slope of input waveform = 0.09 ns, the designers will trade-off between the low operating frequency = 471.698 MHz and the best quality of jitter = 115.7 ps.

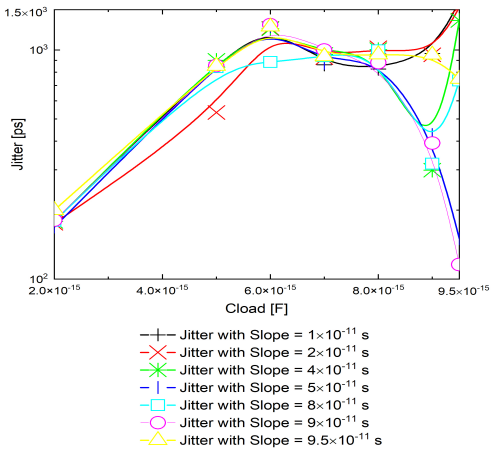

Fig. 13 Jitter variation with C_{load} and V_{slope} variable

Finally, our simulation results are compared with other studies [19] and [20], which are summarized in table 1. Most of the experiments were executed under the same conditions, including 45 nm technology, supply voltage = 1 V, temperature = 27 ^0C. However, the proposed design of [20] is performed with NCPPLL architecture and supply voltage = 2.5 V. In general, CPPLL has many benefits, such as generating a higher operating frequency range and lower output voltage value than NCPPLL. In 2020, with experiments in [19], its operating frequency range is wider than our study, but its output voltage values are quite big. If the output voltage value is very big, it may cause power waste.

Table 1 PERFORMANCE COMPARISION OF VARIOUS PHASE LOCKED LOOP

Parameter Description	Work in [19]	Work in [20]	This Work
Technology (nm)	45-FinFet	45	45
Supply Voltage (V)	1	2.5	1
Temperature (^{0}C)	27	27	27
PLL Architecture	CPPLL	NCPPLL	CPPLL
Reference Frequency (MHz)	X	0.25	20
Operating Frequency (MHz)	250 -1600	120-800	467.3 - 877.2
Output Voltage (V)	0-1	0.9-1.3	0.12 - 0.4
Variation Jitter (ps)	X	X	115.7 - 1293.3
Divider Ratio	4	16	8
C_{load} (fF)	X	X	2÷9.5
Slope (ns)	X	8.3	0.01÷0.095

*X was not available

5 Conclusion

This paper mainly deals with the proposed design of the Charge Pump Phase Locked Loop applied in both UHF and VHF frequency bands. Besides, our design has many advantages consisting of low jitter, low power, and high operating frequency. Furthermore, there has been an approach recommended to perform a time-saving design process that involves Ocean language, which is presented in this study. Finally, to validate the proposed design process, our Charge Pump Phase Locked Loop is designed in the Cadence simulation tools with NCSU 45 nm PDK using the optimum value of design variables obtained by the algorithms.

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