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Article

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Proposing an ITC vandalized Threshold Voltage Divergence Model for short channel Omega Gate MOSFET using a partial 3-D Environment

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Abstract. We present an interface-trapped-charge (ITC) vandalized threshold voltage (V_{TH}) divergence model for omega-gate (Ω-G) MOSFETs using a partial 3-D scaling equation. To account the impact, the model comprises the equivalent number of gates, gate dielectric and silicon film thickness, channel limitations. The impacts of analogous oxide charges on the flat-band voltage are also examined for short-channel-free operation. A thin gate oxide is essential to prevent V_{TH} value divergence caused by the ITC charges. The ITC vandalized device with a thick silicon sheet is altered with wee V_{TH} value variations caused by trapped charges but rapidly increases in the thin silicon sheet device. We can reduce the V_{TH} value by changing the value of oxide-to-gate underlap coverage factor (OUCF). Large underlap coverage factor value is desirable for positive trapped charges and small value for negative trapped charges. A damaged device with negative trapped charges performs better in short-channel conditions than one with positive trapped charges. Due to its 3-D nature, the proposed model may be efficiently used to investigate the V_{TH} behavior and the device operating characteristics of omega-gate (Ω-G) MOSFET. It may also be competently used in device memory cell applications. Hence, the proposed model provides a deep understanding of device physics along with its computational ability, effectiveness and simplicity.

Keywords: Threshold Voltage, Omega Gate MOSFET, partial 3-D scaling, Weighted Sum Model, HCE, SCE, Interface Trapped Charges, OUCF, Natural Length.

1 Introduction

Many semiconductor companies are now conducting research on Multi-Gate (M-G) MOSFETs for deep submicron CMOS packaging. These devices have the potential to push the limits of silicon integration beyond what is possible with traditional planar technology. Below the 16 nm technology node, M-G designs are recommended to overcome substantial difficulties such as short channel effects (SCE) and preferring a manufacturing techniques identical to conventional CMOS [1]. They have the potential to be a promising candidate for future scaling with novel device structures like Triple-Gate (T-G), Surrounding-Gate (SR-G), Omega-Gate (Ω-G), pi-Gate (π- G), and Quadruple-Gate (Q-G) FETs. These devices have strong field confinement, prominent volume conduction, and high packing density required for future CMOS scaling [2]. It is necessary to accurately model these devices for their efficient use in circuit applications [3]. Despite the fact that various studies have modelled M-G devices [4]-[6], very less research has been done on the divergence of the threshold voltage (V_{TH}) model for Ω-G MOSFETs because of interface trapped charges

(ITC).

In the memory cell application for electronic effects memory, charge injection and the trapping mechanism are extremely important. As a result, we believe it is necessary to construct an analytical compact model for the M-G MOSFET device that takes into account the divergence effect generated by the ITC. Due to the well-understood 2-D symmetrical structure of Double-Gate (D-G) and SR-G MOSFETs in bulk silicon, the 2-D analytical solutions [7]-[8] are sufficient to construct the device model. T-G devices such as π-G, Ω-G, and FinFET devices exhibit 2-D asymmetry in their bulk silicon structure. Rendering this, 2-D analytical technique is unsuitable for modelling these 2-D asymmetrical devices. Additional approach to successfully model these 2-D asymmetrical devices is by employing the 3-D solution method on them [9]-[10]. The 3-D technique, on the other hand, requires far too much calculation to be applied.

To surmount these issues, in this paper, we present a unique partial 3-D ITC vandalized V_{TH} model for Ω-G MOSFETs established using partial3-D scaling equation. The suggested method, which use the partial 3-D scaling equation, avoids the complicated mathematics of the 3-D model while still providing a relatively simple compact model for describing the device's V_{TH} behavior. The mathematically and logically developed outcomes are endorsed and supported by the 3-D device simulation results [11]. The simulation results also clearly demonstrates the V_{TH} divergence characteristics caused by fixed ITC of various polarities, ITC section length, gate oxide thicknesses, OUCF, and silicon film thicknesses. The proposed model provides a deep understanding of device physics along with its computational ability, effectiveness and simplicity

2 ITC vandalized V_{TH} Divergence Model Development

The short-channel effect (SCE) of any device can be measured by its Natural Length (λ). It denotes the depth of the drain electric field's penetration into the channel. To reduce the SCE, a low value of λ is preferred. It is governed by the gate oxide and silicon film thicknesses. The thinner the gate oxide and silicon layer is, the lower the natural length and, thus, the impact of the drain electric field on the channel area. According to numerical calculations, the effective gate length of a MOS device must be more than 5 to 10 times the natural length to eradicate SCEs. Multi-gate devices with a square cross section can benefit from the natural length concept. Table 1summaries the natural lengths associated with various MOSFET device geometries as below.

Table 1. Natural lengths associated with various device geometries.

MOSFET Device geometries	Natural lengths
S-G MOSFET	$\lambda_{S\text{-}G} = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox} + \frac{t_{Si}^2}{2}}$
D-G MOSFET	$\lambda_{D\text{-}G} = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} t_{Si} t_{ox} + \frac{t_{Si}^2}{8}}$
Q-G MOSFET	$\lambda_{Q\text{-}G} = \sqrt{\frac{\epsilon_{Si}}{4\epsilon_{ox}} t_{Si} t_{ox} + \frac{t_{Si}^2}{16}}$
SR-G MOSFET	$\lambda_{SR\text{-}G} = \sqrt{\frac{\epsilon_{Si}}{4\epsilon_{ox}} t_{Si} t_{ox} + \frac{t_{Si}^2}{16}}$

Established on the similarity, the natural lengths associated with various M-G MOSFET device geometries can be generalized as:

$$\lambda_{M\text{-}G} = \sqrt{\frac{1}{n}\left(\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox} + \frac{t_{Si}^2}{4}\right)} \quad (1)$$

where n represents the Effective Equivalent number of Gates (EEG) of the device. The EEG Logic was first developed by J.P. Colinge to determine the channel's gate control ability in M-G MOSFET devices [3]. Fig. 1(a) depicts a conventional 3-D device structure design of Ω-G MOSFET for easy implementation of EEG Logic. The EEG of any device can also be defined as basically the physical number of sides of the device covered by gate control assuming a square cross sectional device. It represents the effectiveness of the gate to control the electrostatics of the channel.

We can observe, EEG=1 denotes a Single-Gate (S-G) MOSFET, EEG=2 a Double-Gate (D-G) device, and EEG=4 a Quadruple-Gate (Q-G) MOSFET. EEG=3 for a Triple-Gate (T-G) device, EEG is close to π in a pi-Gate (π-G) device by some strange coincidence. EEG fluctuates between 3 and 4 in the Ω-G MOSFET device, depending on the length of the gate extension under the fin. It should be noticed that when the EEG increases, the device gate capacitance increases as well. As a result, when the EEG is

prolonged, the gate-delay does not improve. The EEG, on the other hand, will cause the delay to rise. As a result, gate-delay in Q-G devices is longer than in T-G devices, and in D-G devices is longer than in S-G devices. In evaluation to a smaller EEG, a bigger one might give superior immunity to SCEs. The EEG for M-G MOSFETs, such as D-G, T-G, Q-G, and SR-G MOSFETs, is [6]:

$$EEG_{M\text{-}G} = \lambda^2_{S\text{-}G} / \lambda^2_{M\text{-}G} \quad (2a)$$

The natural length (λ), and hence the SCE behavior of the device can be minimized by reducing gate oxide thickness, silicon film thickness, and switching to a high-k gate dielectric, instead of SiO_2 [12]-[13]. Furthermore, when the number of gates increases, the natural length decreases. The lowering of oxide thickness below 1.5 nm causes gate tunneling current difficulties in short channel devices. Since λ is proportional to the square-root product of gate oxide thickness (t_{ox}) and silicon film thickness (t_{Si}), it is feasible to swap a thin gate oxide for a thin silicon film in M-G devices.

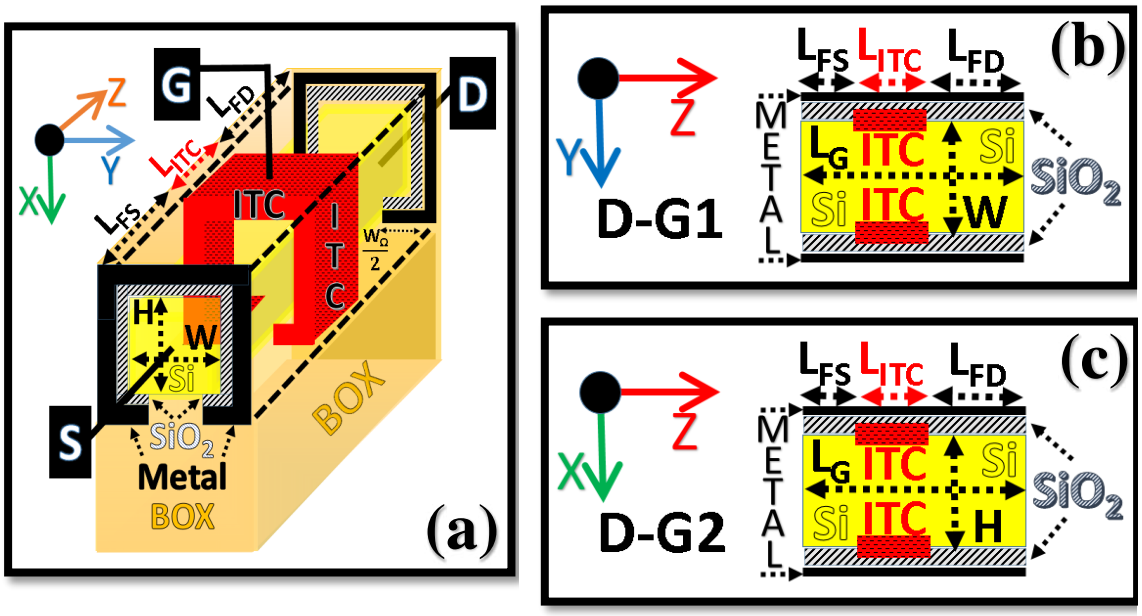
Applying the Weighted Sum Approach (WSA), the 3-D Ω-G MOSFET functioning in X-Y-Z plane can be separated into two D-G MOSFETs (D-G1 & D-G2) working in the 2-D Y-Z and X-Z planes and one S-G MOSFET (S-G2) working in the 2-D X-Z plane respectively [14] as shown in Fig. 1(b), 1(c) and 1(d). Hence, the EEG of Ω-G MOSFET ($EEG_{\Omega\text{-}G}$) can be defined as:

$$EEG_{\Omega-G} = EEG_{D-G1} + (1 - GEF) \times EEG_{D-G2} + GEF \times EEG_{S-G2} \quad (2b)$$

The Gate Extension Factor (GEF) for the Ω-G MOSFET can be considered as the oxide–to-gate underlap factor. As shown in Fig. 1(a), let the one side bottom extension width of the channel in X-Z plane of the Ω-G MOSFET device be $W_\Omega/2$. Assuming the symmetrical extensions, mathematically, $GEF = \frac{W - W_\Omega}{W}$ where W represents the device active channel width along Y-axis.

The natural length of Ω-G MOSFET can be modified using the WSA approach. Employing EEG equation on Ω-G MOSFET, it can be formulated using the natural length of D-G MOSFET and S-G MOSFET as shown below [15]:

$$\left(1/\lambda^2_{\Omega-G}\right) = \left(1/\lambda^2_{D-G1}\right) + \left((1 - GEF)/\lambda^2_{D-G2}\right) + \left(GEF/\lambda^2_{S-G2}\right) \quad (3)$$



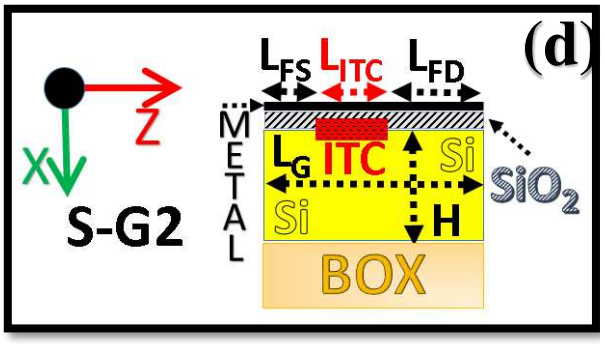


Fig. 1(a). 3-D device structure of omega-gate (Ω-G) MOSFET used for device modeling.
Fig. 1(b). The 2-D device structure of D-G1 operating in Y-Z plane.
Fig. 1(c). The 2-D device structure of D-G2 operating in X-Z plane.
Fig. 1(d). The 2-D device structure of S-G2 operating in X-Z plane.

In extreme case, when GEF = 0, the Ω-G should act as SR-G in respect of SCE and gate controlling properties because of the identical EEG. $\lambda_{D\text{-}G1}$ is the natural length for a Double-Gate device operating in the Y-Z plane; $\lambda_{D\text{-}G2}$ and $\lambda_{S\text{-}G2}$ are the natural lengths for Double-Gate and Single-Gate devices operating in the X-Z plane, separately. $C_{ox} = \mathcal{E}_{ox}/t_{ox}$ is the gate oxide capacitance per unit area. In the bulk conduction mode, the natural lengths of D-G1, D-G2, and S-G2 can be represented as follows:

$$\lambda_{D-G1} = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} W_{Si} t_{ox} + \frac{W_{Si}^2}{8}} \tag{4a}$$

$$\lambda_{D-G2} = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} H_{Si} t_{ox} + \frac{H_{Si}^2}{8}} \tag{4b}$$

$$\lambda_{S-G1} = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} H_{Si} t_{ox} + \frac{H_{Si}^2}{2}} \tag{4c}$$

The omega-gate (Ω-G) MOSFET device structure in 3-D and 2-D formats used for device modeling is distinctly presented in Fig. 1. It also clearly denotes the fresh and ITC vandalized sections of the device across the channel. To understand the ITC dispersals, the channel can be separated into three sections as one ITC-Section (with Interface-Trapped-Charges) and two fresh-sections (without any Interface-Trapped-Charges). The fresh sections are distinctly represented as FD section i.e. Fresh channel section towards Drain terminal and FS section i.e. Fresh channel section towards Source terminal. The FS section length at the Si/SiO_2 interface along the channel length can be limited from 0 to ($L_G - L_{ITC} - L_{FD}$) in Z-axis direction. Similarly, the ITC vandalized section length is limited from ($L_G - L_{ITC} - L_{FD}$) to ($L_G - L_{FD}$). Further, the FD section length is limited from ($L_G - L_{FD}$) to L_G in the same direction.

Solving 3-D Poisson's equation with the depletion approximation yields the potential distribution in the channel of a fully depleted M-G MOSFET. As a result, the channel potential can be obtained by solving the three-dimensional Poisson's equation with the depletion approximation.

$$\frac{d^2\emptyset}{dx^2}(x,y,z) + \frac{d^2\emptyset}{dy^2}(x,y,z) + \frac{d^2\emptyset}{dz^2}(x,y,z) = \frac{qN_a}{\epsilon_{Si}} \tag{5}$$

where Φ(x, y, z) represents the 3-D channel potential, N_a represents the uniform channel doping density. Using the 3-D electric field components (E_x, E_y, E_z), the equation can be rewritten in simple form as:

$$\frac{dE_x}{dx}(x,y,z) + \frac{dE_y}{dy}(x,y,z) + \frac{dE_z}{dz}(x,y,z) = Const. \tag{6}$$

The statement asserts that the total of the deviations of the electric field components in all directions is a constant value (Const.) at every location inside the channel. As a result, if one of the components rises, the total of the other two will almost surely fall.

Square cross sectioned Q-G MOSFET devices, we may observe $d^2\Phi/dy^2 = d^2\Phi/dz^2$ near the device's center, where the electric field lines from the drain have the greatest influence on the device body. As a result, the Poisson equation becomes:

$$\frac{d^2\emptyset}{dx^2}(x,y,z) + 2\frac{d^2\emptyset}{dy^2}(x,y,z) = \frac{qN_a}{\epsilon_{Si}} \tag{7}$$

When examining the central conduction mode for the -G MOSFET operating in the sub-threshold region, the central channel potential of the different sections should fulfil the scaling equation (8) [16]. Assuming a symmetrical channel doping across the section, the scaling equations for fresh and ITC vandalized sections are represented as:

$$\frac{d^2\emptyset_F(z)}{dz^2} = \frac{1}{\lambda^2_{\Omega-\mathrm{G}}}(\emptyset_F(z) - \theta_F) \tag{8a}$$

$$\frac{d^2\emptyset_{ITC}(z)}{dz^2} = \frac{1}{\lambda^2_{\Omega-\mathrm{G}}}(\emptyset_{ITC}(z) - \theta_{ITC}) \tag{8b}$$

where Φ_F and Φ_{ITC} are the central channel potentials of the fresh and ITC vandalized sections of Ω-G MOSFET respectively. Correspondingly, θ_F and θ_{ITC} represents the central channel potential for the fresh and ITC vandalized sections in long channel device. Mathematically, the terms θ_F and θ_{ITC} can be formulated as:

$$\theta_F = V_{GS} - V_F - \frac{qN_a}{\epsilon_{Si}}\lambda^2_{\Omega-\mathrm{G}} \tag{9a}$$

$$\theta_{ITC} = V_{GS} - V_{ITC} - \frac{qN_a}{\epsilon_{Si}}\lambda^2_{\Omega-\mathrm{G}} \tag{9b}$$

where V_{GS} is the applied gate voltage and $\lambda_{\Omega\text{-}G}$ is the natural length of Ω-G MOSFET. The flat-band voltage in fresh and ITC vandalized sections of the Ω-G MOSFET device is represented as V_F and V_{ITC} respectively. Using fresh section flat-band voltage (V_F) and equivalent oxide charge effect, the expression of flat-band voltage in ITC vandalized section (V_{ITC}) can be approximated as [17]:

$$V_{ITC} = V_F - \frac{qN_{ITC}}{C_{ox}} \tag{10}$$

where N_{ITC} is the uniformly distributed interface trapped charge density per unit area at the Si-SiO_2 interface of Ω-G MOSFET. For simplicity, the localized oxide charge density is assumed to be negligible. Effective gate oxide capacitance per unit area is represented as C_{ox}.
Solving the central channel potential for fresh section (Φ_F) and ITC vandalized section (Φ_{ITC}) along the channel length, the general solution of (8) can be represented as:

$$\emptyset_{ITC}(z) = a_{ITC}e^{\frac{z}{\lambda}} + b_{ITC}e^{\frac{-z}{\lambda}} + \theta_{ITC} \tag{11a}$$

$$\emptyset_F(z) = a_f e^{\frac{z}{\lambda}} + b_f e^{\frac{-z}{\lambda}} + \theta_F \tag{11b}$$

Assuming the continuity of electric field and potential in the respective sections, we can calculate the coefficients of equation (11). As shown in Fig. 1(a), the total channel length of Ω-G MOSFET (L_G) is represented as the channel length submission of ITC vandalized section (L_{ITC}) and fresh sections ($L_G = L_{ITC} + L_{FD} + L_{FS}$). Applying the appropriate boundary conditions of ITC vandalized section length on device's central potential (11a), we can easily determine the coefficients (a_{ITC} and b_{ITC}). We use the V_{bi} as the device built-in voltage at FS-channel and FD-channel junction. The drain bias is represented as V_{DS}. The variable k is inverse of the device natural length. Using these parameters, the coefficients in (11a) can be represented as:

$$a_{ITC} = \frac{\coth(kL_G)-1}{2}\Big[e^{kL_G}\left(V_{bi} + V_{DS} - \theta_{ITC} + \frac{qN_{ITC}}{C_{ox}}\right) + \theta_{ITC} - \frac{qN_{ITC}}{C_{ox}} - V_{bi} + (\theta_{ITC} - \theta_F)\left(\cosh(kL_{FS}) - \frac{e^{-kL_{FD}}}{2} - \frac{e^{k(L_G-L_{FD})}}{2}\right)\Big] \tag{12a}$$

$$b_{ITC} = \frac{\coth(kL_G)-1}{4}[2e^{2kL_G}V_{bi} - 2e^{kL_G}(V_{bi} + V_{DS}) + (\theta_F - \theta_{ITC})\left(e^{k(2L_G+L_{FS})} + e^{k(2L_G-L_{FS})}\right) - 2e^{k(L_G-L_{FD})}(\theta_F - \theta_{ITC}) - 2\left(\theta_{ITC} - \frac{qN_{ITC}}{C_{ox}}\right)(e^{2kL_G} - e^{kL_G})\Big] \tag{12b}$$

The fresh section of the Ω-G MOSFET device has been divided into two distinct sections: fresh section near the source side (FS) and fresh section near the drain side (FD) as shown in Fig. 1. Applying the appropriate channel length boundary conditions of the fresh section's length on equation (11b), the corresponding coefficients (a_F and b_F) can be determined. The coefficients for fresh section near the source side and drain side are represented as (a_{FS} and b_{FS}) and (a_{FD} and b_{FD}) respectively.

$$a_{FS} = \frac{\coth(kL_G)-1}{2}[(\cosh(kL_G - kL_{FS}) - \cosh(kL_{FD}))(\theta_{ITC} - \theta_F) + (V_{DS} + V_{bi} - \theta_F)e^{kL_G} - V_{bi} + \theta_F] \quad (12c)$$

$$b_{FS} = \frac{\operatorname{csch}(kL_G)}{2}[(\cosh(kL_{FD}) - \cosh(kL_G - kL_{FS}))(\theta_F - \theta_{ITC}) + e^{kL_g}(V_{bi} - \theta_F) - V_{DS} - V_{bi} + \theta_F] \quad (12d)$$

$$a_{FD} = \frac{\coth(kL_G)-1}{2}[e^{kL_G}(V_{bi} + V_{DS} - \theta_F) + \theta_F - V_{bi} + (\theta_{ITC} - \theta_F)(\cosh(kL_{FS}) - \cosh(kL_G - kL_{FD}))] \quad (12e)$$

$$b_{FD} = \frac{e^{kL_G}(\coth(kL_G)-1)}{2}[e^{kL_G}(V_{bi} - \theta_F) - V_{bi} - V_{DS} + \theta_F + e^{kL_G}(\theta_{ITC} - \theta_F)(\cosh(kL_G - kL_{FD}) - \cosh(kL_{FS}))] \quad (12f)$$

Using the coefficients, we can easily calculate the central potential for both fresh and ITC vandalized sections. As a result, the minimal central potentials of the respective sections can be represented as:

$$\emptyset_{F,MIN} = 2\sqrt{a_f b_f} + \theta_F \quad \text{and} \quad \emptyset_{ITC,MIN} = 2\sqrt{a_{ITC} b_{ITC}} + \theta_{ITC} \quad (13)$$

It should be noted that the complete channel's minimum central potential (Φ_{MIN}) can be derived by selecting the least value in (13).

$$\emptyset_{MIN} = min(\emptyset_{ITC,MIN}, \emptyset_{F,MIN}) \quad (14)$$

Further, the V_{TH} fundamental model states that V_{TH} value of a device is equal to the summation of the flatband voltage, minimum surface potential and the voltage drop across the oxide due to the depletion layer charge. The flatband voltage of fresh and ITC vandalized sections has already been derived above as V_F and V_{ITC} respectively. We know the well-established condition that the gate voltage value represents the device V_{TH} value when the channel minimum surface potential (Φ_{MIN}) is twice the bulk potential (Φ_B). Mathematically, the condition can be represented as: $\emptyset_{MIN} = 2\emptyset_B$. Hence, the discrete V_{TH} values of fresh and ITC vandalized sections can be derived by solving for gate voltage with this applied condition on (13), and equating the respective section minimum surface potential ($\Phi_{ITC,MIN}$ and $\Phi_{F,MIN}$) to twice the bulk potential (Φ_B).

The V_{TH} value for fresh section (V_{TF}) and ITC vandalized section (V_{TITC}) of the Ω-G MOSFET device can be modeled as:

$$V_{TF} = V_F + \frac{qN_aH_{Si}}{4C_{OX}} - \frac{B_f + \sqrt{B_f^2 - A_f C_f}}{A_f} \quad (15a)$$

$$V_{TITC} = V_{ITC} + \frac{qN_aH_{Si}}{4C_{OX}} - \frac{B_{ITC} + \sqrt{B_{ITC}^2 - A_{ITC}C_{ITC}}}{A_{ITC}} \quad (15b)$$

The coefficients in (15) are simplified as below:

$$A_f = 1 - 4\alpha_f\gamma_f \quad \text{and} \quad A_{ITC} = 1 - 4\alpha_{ITC}\gamma_{ITC}$$
$$B_f = -2(\Phi_B + \beta_f\gamma_f + \alpha_f\sigma_f) \quad \text{and} \quad B_{ITC} = -2(\Phi_B + \beta_{ITC}\gamma_{ITC} + \alpha_{ITC}\sigma_{ITC})$$
$$C_f = 4(\emptyset_B^2 - \beta_f\sigma_f) \quad \text{and} \quad C_{ITC} = 4(\emptyset_B^2 - \beta_{ITC}\sigma_{ITC})$$

where

$$\alpha_f = \alpha_{ITC} = \frac{\coth(kL_G)-1}{2}(1 - e^{kL_G})$$

$$\beta_{fs} = \frac{\coth(kL_G) - 1}{2}[((\cosh(kL_G - kL_{FS}) - \cosh(kL_G - kL_{FD}))(\theta_{ITC} - \theta_F) + V_{DS} + V_{bi})e^{kL_G} - V_{bi}]$$

$$\beta_{ITC} = \frac{\coth(kL_G) - 1}{2}\left[e^{kL_G}\left(V_{bi} + V_{DS} + \frac{qN_f}{C_{ox}}\right) - \frac{qN_f}{C_{ox}} - V_{bi} + (\theta_{ITC} - \theta_F)(\cosh(kL_{FS}) - e^{k(L_G - L_{FD})})\right]$$

$$\beta_{fd} = \frac{\coth(kL_G)-1}{2}[e^{kL_G}(V_{bi} + V_{DS}) - V_{bi} + (\theta_{ITC} - \theta_F)(\cosh(kL_{FS}) - \cosh(kL_G - kL_{FD}))]$$

$$\gamma_{fs} = \frac{csch(kL_G)}{2}(1 - e^{kL_G})$$

$$\gamma_{ITC} = \gamma_{fd} = \frac{\coth(kL_G)-1}{2}e^{kL_G}(1 - e^{kL_G})$$

$$\sigma_{fs} = \frac{csch(kL_G)}{2}[(\cosh(kL_{FD}) - \cosh(kL_G - kL_{FS}))(\theta_{ITC} - \theta_F) + (e^{kL_G} - 1)V_{bi} - V_{DS}]$$

$$\sigma_{ITC} = \frac{\coth(kL_G)-1}{4}\left[\frac{2qN_f}{C_{ox}}e^{kL_G}(1 - e^{kL_G}) + (\theta_F - \theta_{ITC})(e^{k(2L_G + L_{FS})} - e^{k(L_G - L_{FD})} + e^{k(2L_G - L_{FS})})\right]$$

$$-e^{k(L_G+L_{FD})}(\theta_F-\theta_{ITC})-2e^{kL_G}(V_{bi}+V_{DS})+2e^{2kL_G}V_{bi}\big]$$

$$\sigma_{fd}=\frac{\coth(kL_G)-1}{2}e^{kL_G}[(e^{kL_G}-1)V_{bi}-V_{DS}+e^{kL_G}(\theta_{ITC}-\theta_F)(\cosh(kL_G-kL_{FD})-\cosh(kL_{FS}))]$$

The V_{bi} is the device built-in voltage at source-channel and drain-channel junction. The drain bias is represented as V_{DS}. The variable k is inverse of the device natural length.

Using the above modeled variables, we are successfully able to calculate discrete values of V_{TH} for fresh section and ITC vandalized section as V_{TF} and V_{TITC} respectively. The largest V_{TH} value of the (15) will finally define the V_{TH} characteristics of the Ω-G MOSFET device. Hence, we can represent the device V_{TH} value of the Ω-G MOSFET ($V_{TΩ\text{-}G}$) as:

$$V_{T\Omega-G}=max(V_{TF},V_{TITC}) \qquad (16).$$

3 Outcomes and the Analysis of the Model

The proposed model is validated using the ATLAS, a TCAD 3-D device simulator. Fig. 2(a) depicts a plot of the channel's minimum central potential (Φ_{MIN}) vs. the normalized ITC vandalized section (L_{ITC}/L_G) and for different gate oxide thickness (t_{ox}) with fixed positive and negative ITC. The Φ_{MIN} variations are reduced as the t_{ox} is reduced. The channel's Φ_{MIN} value is raised by the positive ITC and lowered by negative ITC as clearly seen in Fig. 2(a). The variation of the Φ_{MIN} in the channel increases as the ITC vandalized section is enlarged. Hence, in a device, a thin gate oxide layer should be employed to reduce V_{TH} divergence value. The increased value of Φ_{MIN} will pull-down the V_{TH} value due to decreased flatband voltage value.

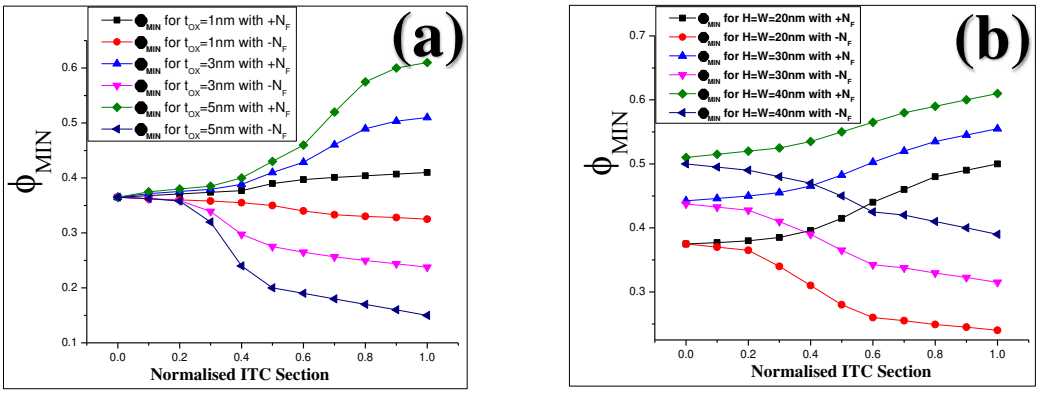
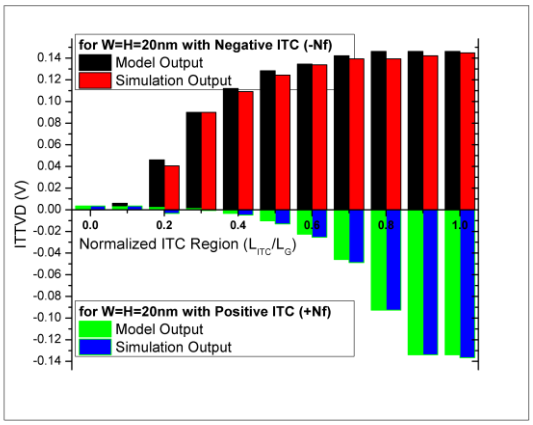
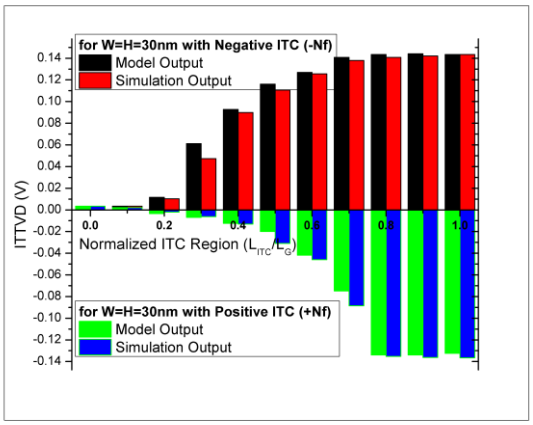
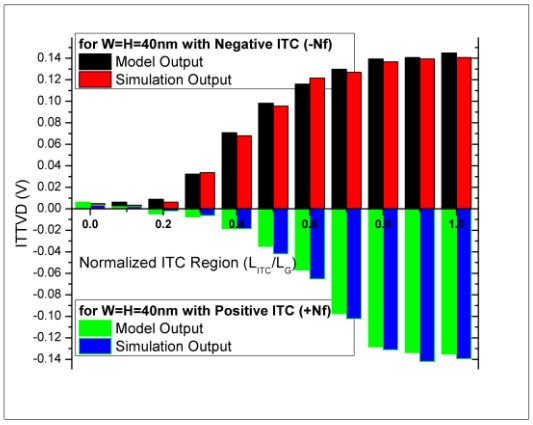


Fig. 2. Plot for channel's minimal central potential (Φ_{MIN}) vs. normalized ITC vandalized section (L_{ITC}/L_G) trapped with fixed positive charges and negative interface charges ($\pm N_f$): (a). for different gate oxide thickness (t_{ox}) with silicon film square cross section channel (H = W = 20 nm). (b). for different silicon film square cross section channels (H = W) with gate oxide thickness (t_{ox} = 3 nm). V_{DS} = 0.05 V, L_G = 100 nm, $N_a = 1.0\times10^{16}$ cm^{-3}, $N_d = 1.0\times10^{20}$ cm^{-3}, $N_f = \pm1.0\times10^{12}$ cm^{-2}, L_{FD} = 0 nm, and OUCF = 0.5 were used as simulation parameters.

For the fixed positive and negative ITC, Fig. 2(b) displays a plotting of Φ_{MIN} vs. the normalized ITC vandalized section (L_{ITC}/L_G) and for different silicon film square cross section channels (H = W). It can be easily verified through Fig 2(b) that the fixed positive ITC will raise the Φ_{MIN} and fixed negative ITC will lower the Φ_{MIN} in the channel. The Φ_{MIN} variations increase as the silicon film thickness is reduced. The Φ_{MIN} variations increase as the ITC vandalized section is increased. On the other hand, the figure also validates that thick silicon film is necessary to increase Φ_{MIN} divergence value and decreases the V_{TH} divergence value induced by negative ITC. Fig. 3–5 present more information about how positive and negative ITC affect V_{TH} divergence value with varied normalized ITC vandalized section (L_{ITC}/L_G). The V_{TH} value roll-off versus device gate length is plotted in Fig. 6 for both fresh and ITC vandalized devices.





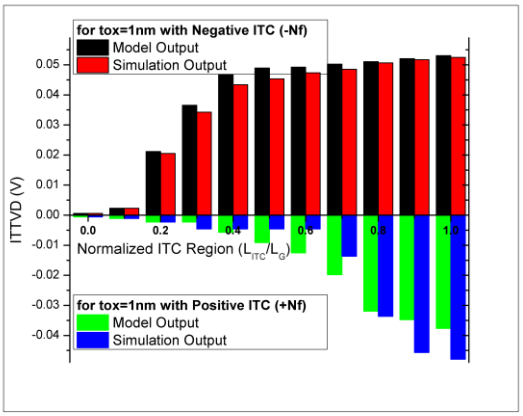


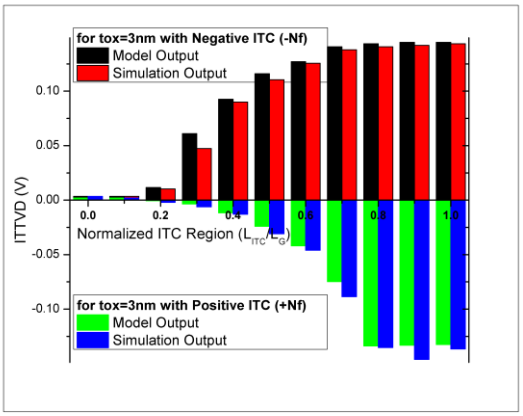
Simulation Parameters
V_{DS} = 0.05 V
L_G = 100 nm
t_{ox} = 3 nm
N_a = 1.0 x 10^{16} cm^{-3}
N_d = 1.0 x 10^{20} cm^{-3}
N_f = ±1.0 x 10^{12} cm^{-2}
L_{FD} = 0 nm
OUCF = 0.5

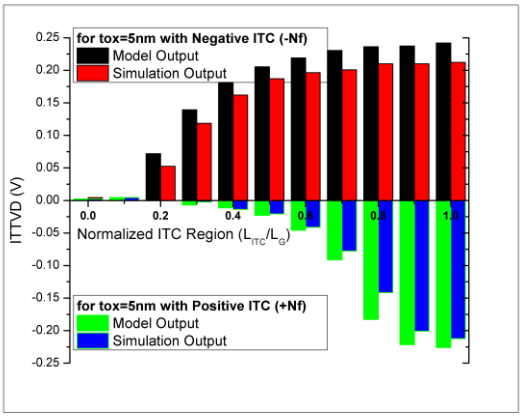
Fig. 3. ITTVD vs. normalized ITC vandalized section (L_{ITC}/L_G) for different silicon film square cross section channels (H = W) trapped with fixed positive and negative interface charges (±N_f).

ITTVD stands for Interface-Trapped-Charge-Induced V_{TH} value Degradation. The fixed positive and negative ITC causes roll-up or roll-off in the device V_{TH} characteristics. Hence, the term ITTVD is used to describe the V_{TH} value differential between ITC vandalized device and fresh device. Mathematically, ITTVD = (V_{TITC} - V_{TF}).

Fig. 3 illustrates ITTVD vs. normalized ITC vandalized section (L_{ITC}/L_G) for different silicon film square cross section channels (H = W) trapped with fixed positive and negative interface charges (±N_f). By imitating the ITC impact on V_{TH} value deterioration, the expanded normalized ITC vandalized section can increase ITTVD impact even further. Thin silicon film square cross section channel is preferred for positive trapped charges to lower the ITTVD as the ITC vandalized section grows. When the ITC vandalized section expands, thin silicon film, on the other hand, can intensify the ITTVD impact induced by the negative ITC. To reduce the ITTVD induced by negative trapped charges, thick silicon film square cross section channel is preferred.



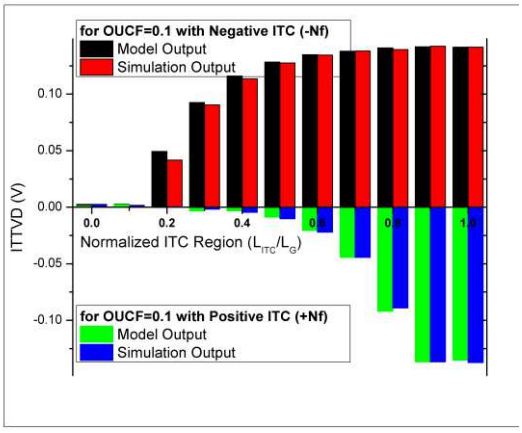


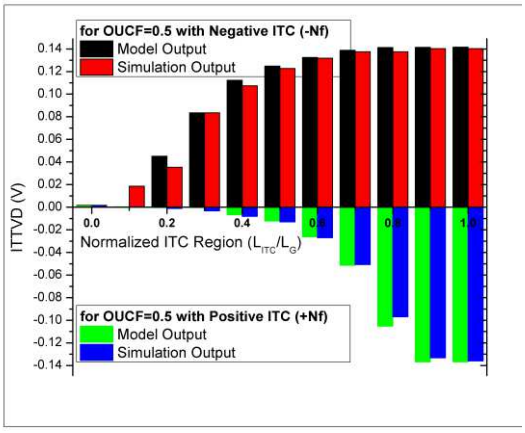


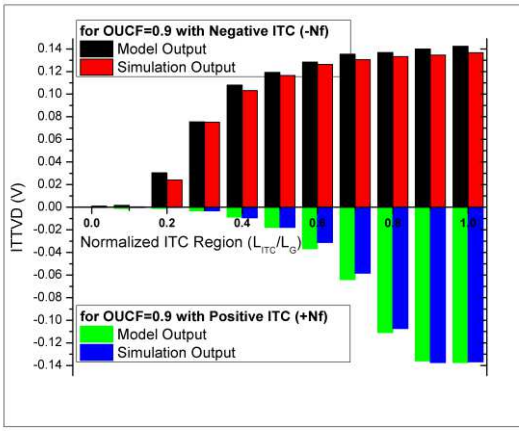
Simulation Parameters
V_{DS} = 0.05 V
L_G = 100 nm
H = W = 20 nm
N_a = 1.0 x 10^{16} cm^{-3}
N_d = 1.0 x 10^{20} cm^{-3}
N_f = ±1.0 x 10^{12} cm^{-2}
L_{FD} = 0 nm
OUCF = 0.5

Fig. 4. ITTVD vs. normalized ITC vandalized section (L_{ITC}/L_G) for different oxide thicknesses trapped with fixed positive and negative interface charges (±N_f).

For varied oxide thicknesses, Fig. 4 displays the ITTVD vs. the normalized ITC vandalized section. The device ITTVD will be severe if trapped charges with a large ITC vandalized section are present, especially if the gate oxide is thick. A thin gate oxide, as well as a small ITC vandalized section, are essential for the device to suffer from less ITTVD impact. When the normalized ITC vandalized section (L_{ITC}/L_G) is increased from 0 to 1.0, Fig. 5 shows how the OUCF impacts the device ITTVD. To resist the ITTVD impact, a big OUCF of 0.9 is preferable for positive trapped charges. The modest OUCF of 0.1, on the other hand, is favored to ease the ITTVD induced by negative ITC. When (L_{ITC}/L_G) exceeds 0.9, all of these devices with various OUCFs have nearly the same V_{TH} value divergence.



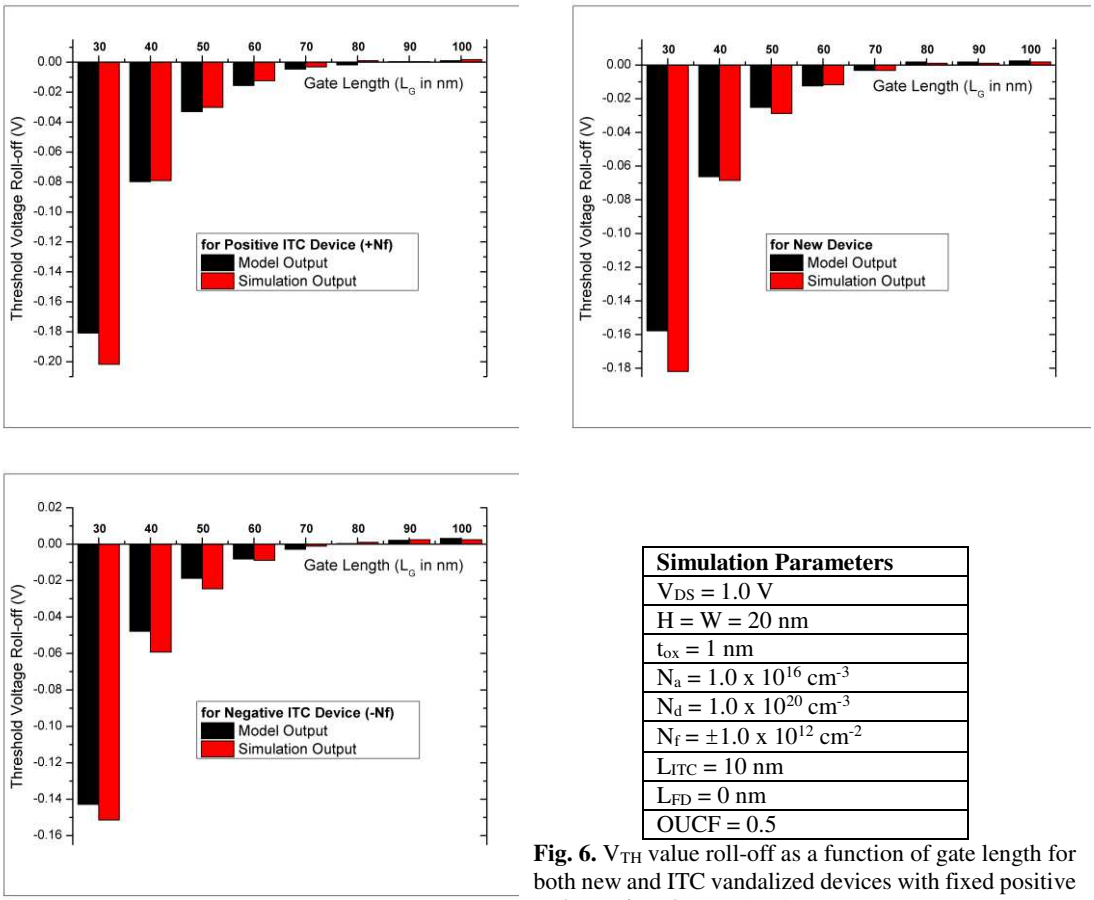




Simulation Parameters
V_{DS} = 0.05 V
L_G = 100 nm
H = W = 20 nm
t_{ox} = 3 nm
N_a = 1.0 x 10^{16} cm^{-3}
N_d = 1.0 x 10^{20} cm^{-3}
N_f = ±1.0 x 10^{12} cm^{-2}
L_{FD} = 0 nm

Fig. 5. ITTVD vs. normalized ITC vandalized section (L_{ITC}/L_G) for various oxide-to-gate underlap coverage factors trapped with fixed positive and negative charges (±N_f).

The V_{TH} value roll-off versus gate length is shown in Fig. 6 for both new and ITC vandalized devices. It plots the dependency of V_{TH} value as a function of gate length for both new and ITC vandalized devices with fixed positive and negative ITC (±N_f). We can observe that the device with negative ITC can better combat SCEs and has a lower V_{TH} roll-off value than the device with positive ITC.



Simulation Parameters
V_{DS} = 1.0 V
H = W = 20 nm
t_{ox} = 1 nm
N_a = 1.0 x 10^{16} cm^{-3}
N_d = 1.0 x 10^{20} cm^{-3}
N_f = ±1.0 x 10^{12} cm^{-2}
L_{ITC} = 10 nm
L_{FD} = 0 nm
OUCF = 0.5

Fig. 6. V_{TH} value roll-off as a function of gate length for both new and ITC vandalized devices with fixed positive and negative charges (±N_f).

4 Conclusion

For the Ω-G MOSFETs, a novel partial 3-D ITC vandalized V_{TH} divergence model was effectively established. The model investigates how varying positive and negative polarities of interface trapped charges, normalized ITC vandalized section (L_{ITC}/L_G), gate oxide thicknesses, OUCF, and silicon thicknesses effect the V_{TH} characteristics of the device. Due to its computing efficiency and simple formula, the model can be straightforwardly implemented for the charge-trapped Ω-G MOSFET device simulation. Additionally, it also provides a practical insight into the device physics. This further helps us in understanding the SCEs behavior of the device. The model may also be used to investigate the Ω-G MOSFET's memory cell application's hot-carrier-induced V_{TH} divergence. Likewise, the model can also be utilized to explore the Ω-G device hot-carrier-Injection effects on the V_{TH} value divergence characteristics for memory cell application.

Author Declarations

Ethics approval: "Not Applicable"

Consent to participate: "Not Applicable"

Consent for publication: The author gives his consent for the publication of his submitted research work, to be published in the above Journal and Article.

Availability of data and materials: The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Competing interests: The author declares that he has no competing interests.

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Authors' contributions: The author confirms sole responsibility for the following: study conception and design, data collection, analysis and interpretation of results, and manuscript preparation.

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