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Rajneesh Sharma (✉ sharma.rajneesh@tcd.ie)

Thapar Institute of Engineering and Technology <https://orcid.org/0000-0003-3182-8700>

Ashwani Kumar Rana

National Institute of Technology Hamirpur

Shelja Kaushal

National Institute of Technology Hamirpur

Justin King

Trinity College Dublin: The University of Dublin Trinity College

Ashish Raman

Dr BR Ambedkar National Institute of Technology

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Analysis of Underlap Strained Silicon on Insulator MOSFET for Accurate and Compact Modeling

Rajneesh Sharma^{1*}, Ashwani K. Rana², Shelza Kaushal², Justin B. King³ and Ashish Raman⁴

¹Department of Electronics and Communication Engineering, TIET, Patiala, India

²Department of Electronics and Communication Engineering, NIT Hamirpur, India

³Department of Electrical and Electronics Engineering, Trinity College Dublin, Ireland

⁴Department of Electronics and Communication Engineering, Dr. B. R. Ambedkar NIT Jalandhar, India

Abstract: Recently, transistors with an underlapped gate structure have been widely studied to overcome several challenges associated with nanoscale devices. In this work, underlap region is incorporated at source and drain (S/D) ends in a fully depleted Strained Silicon On Insulator (SSOI) device, with high-k dielectric material in the spacer region. The S/D underlapped region helps to reduce the leakage current and can be particularly useful for low power applications. However, increased underlap length degrades the ON current significantly. We show that this issue can be mitigated via the inclusion of a high-k spacer, which improves the ON current by enhancing the gate controllability over the S/D underlap channel region. It helps to achieve the essential requirement low power applications i.e. the high ON/OFF current ratio at extremely low value of leakage current. The strained silicon material is used in the channel region to further improve the ON current. A compact threshold voltage model is developed for the proposed device (underlap-SSOI) while maintaining the accuracy at par with TCAD simulations. This threshold voltage model incorporates underlap length, strain-induced offsets and spacer dielectric constant. This device model may be used for circuit simulations.

Keywords: Fully Depleted Strained Silicon On Insulator, Underlap, Threshold Voltage Model, Strain Effects.

1. Introduction:

In the nanoscale regime, the increased short channel effects (SCEs), parasitic capacitances and leakage current, all restrict the scaling of bulk MOSFET technology. The fully depleted Silicon On Insulator (SOI) structure has received

attention as a method of achieving high performance and enhancing the scalability [1,2]. The advantages of SOI has been come from low device variability due to low channel doping, superior SCEs control due to elimination of leakage path, low parasitic

*Correspondence Author: rajnish1ece@gmail.com

capacitance and excellent compatibility with current bulk MOSFET technology [3,4]. These entire features are very useful for low power and low standby power applications such as Internet of Things (IoT), consumer multimedia, wearables, System on Chip (SoC) integration etc [4]. However, the distance between the source and drain regions becomes very small in nanoscale overlap strained SOI (overlap-SSOI) devices. As a result, gate control over the channel current is reduced and the drain becomes prominent in governing the electric potential across the device channel. The dominance of drain voltage (V_{DS}) increases the drain induced barrier lowering (DIBL) effect and leakage current in the device [5]. To alleviate these problems, various advanced structures have been studied such as the FinFET [6], the silicon nanowire FET [7], CNT FET [8] and quadruple-gate MOSFET [9, 10]. However, these structures are vulnerable to process variability, are difficult to realize, are costly and have complex fabrication techniques [11-14]. Alternatively, underlap structures have been reported in refs. 15–19 as a way to control SCEs especially a leakage current problem. The underlap region increases the distance between source and drain (S/D), and reduces the drain dominance over the channel electric potential. However, there is further scope for improvement in underlap devices as this modification has resulted in

degradation of the ON current due to the increase in the S/D series resistance [19, 20].

Various performance booster techniques required to maintain the inevitable trend of downscaling. In this direction, strain engineering has been investigated as one of the most prominent solutions to achieve high ON current with the present fabrication techniques. The strained devices show high driving capability due to enhanced carrier mobility [21]. A strained Si layer, of desired thickness, is used as the channel in SOI MOSFETs, using layer transfer (LT) techniques [22]. Moreover, recent work suggests that the high-k dielectric material as a spacer region enhances the ON current in underlap devices without degrading the OFF current and intrinsic delay of the device [18]. The International Technology Roadmap for Semiconductors (ITRS) has recommended that one of, or a combination of, the new techniques is required to continue the performance improvement in low power applications [23]. Therefore, in this work, an underlapped fully depleted strained SOI MOSFET with high-k spacer, termed as underlap-SSOI, is proposed, as shown in Fig. 1. This structure has been analyzed across the key performance metrics of: leakage current, ON current, total gate capacitance and gate delay, with

the objective of achieving low power consumption.

Based on our earlier work [24], the innovative modeling approach is adapted here to develop a threshold voltage model for the underlap-SSOI structure. The threshold voltage model includes the effects of strain induced offsets, underlap length, gate length, spacer dielectric constant and channel doping. The model results have been compared with TCAD simulations in order to establish the accuracy of the model.

2. Device Design and Performance Evaluation:

In this section, an n-channel underlap-SSOI device is designed and compared to the performance of conventional overlap-SSOI devices. In Fig. 1, the gate underlap regions can be seen as those lengths L_1 and L_2 ,

between the source and the gate, and the drain and the gate, respectively. A high-k dielectric material is used to form gate oxide, spacer1 and spacer2. Strained Si is used as body of the device, with a thickness of t_{ssi} . Channel region along the x-axis from 0 to L_1+L+L_2 , as shown in Fig. 1, is separated into three regions, Region1,

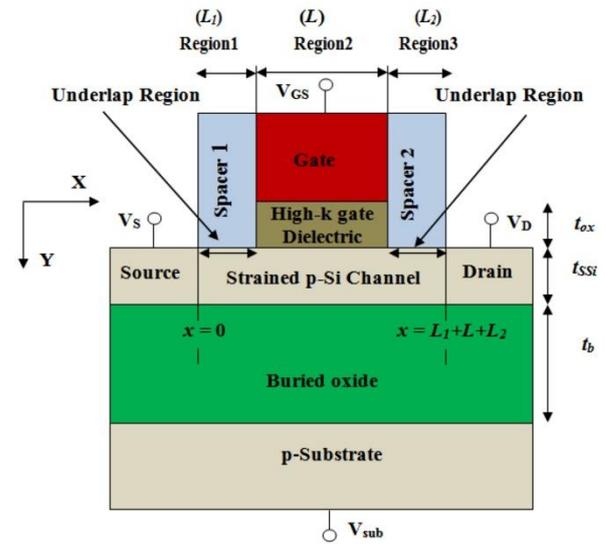
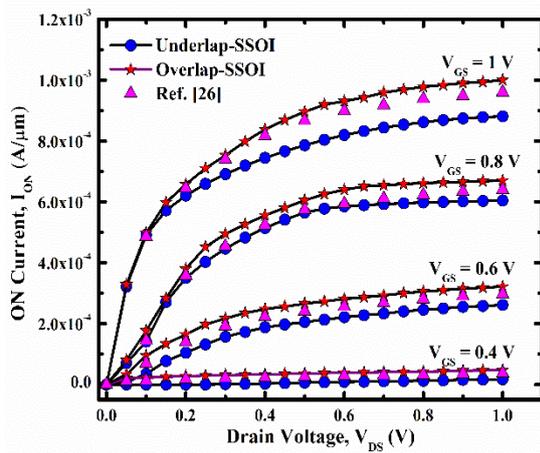
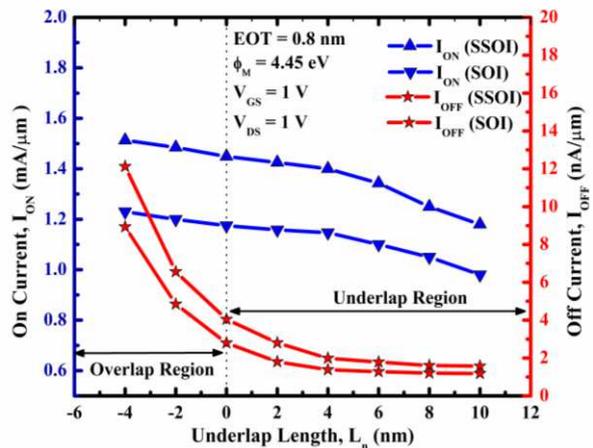


Fig. 1 Schematic structure of Underlap-SSOI with associated physical parameters



(a)



(b)

Fig. 2 (a) ON current vs drain voltage for $\phi_M = 4.4$, $EOT = 1$. (b) Variation in ON and OFF current with underlap length for strained SOI and unstrained SOI. Other parameters: $x = 0.25$, $t_{ssi} = 6$ nm and $L = 25$ nm.

Region2 and Region3 of length $0 < x < L_1$, $L_1 < x < L+L_1$ and $L+L_1 < x < L+L_1+L_2$ respectively. The device dimensions and electrical parameters of underlap-SSOI structure are given in Table I.

In order to evaluate the performance of the underlap-SSOI structure, TCAD simulations are carried out using the Synopsys Sentaurus TCAD Tool, as shown in Figs. 2 to 5. In addition to the drift-diffusion transport model, the Enhanced Lombardi model with high-k mobility degradation has been enabled to account for remote coulomb scattering (RCS) and remote phonon scattering (RPS) at the high-k/channel interface [25]. The bandgap narrowing and strain effect has been taken into consideration using Slotboom model and Monte Carlo-computed mobility for strained Si respectively [25].

Table I Device Parameters used in modeling

Parameters	Values
Underlap length, L_n	-4 nm to 10 nm
Channel length, L	15 nm to 90 nm
Ge Mole fraction, x	0.1 to 0.4
Body thickness, t_{Si}	6 nm
Gate height, t_g	30 nm
Channel doping, N_A	$1 \times 10^{16} \text{ cm}^{-3}$
S/D peak doping, N_{SD}	$1 \times 10^{20} \text{ cm}^{-3}$

The simulation results of underlap-SSOI and overlap-SSOI have been compared to experimental data of [26] as shown in Fig. 2.a. Here, it is important to

note that the difference between the ON current values of underlap-SSOI and overlap-SSOI is decreasing with the decrease in gate voltage. It indicates that underlap-SSOI is beneficial for low voltage operations since the I_{ON} of underlap-SSOI is comparable to overlap-SSOI for lower gate voltage. It has also been observed that the I_{ON} values of simulations are in the good agreement with reported experimental results [26]. Fig. 2.b shows ON current variation as a function of L_n (underlap length) for strained-SOI (SSOI) and unstrained-SOI (SOI). Here, the negative values of L_n represent a length of overlap between the gate and S/D regions. It is shown in Fig. 2 that I_{OFF} decreases significantly with L_n due to reduction in charge sharing between gate and S/D regions. A small degradation in I_{ON} is also observed with increasing L_n due to an increase in the effective channel length. The I_{ON}/I_{OFF} current ratio of the SSOI device is slightly lower than that of the SOI device in the overlap region due to increased I_{OFF} . However, the I_{ON}/I_{OFF} ratio has significantly improved in the underlap region up to $L_n = 4$ nm, as I_{OFF} is reduced exponentially with increasing value of L_n . Thus, the results indicate that the underlap-SSOI structure with L_n of 4 nm maximizes performance.

The underlap length increases the effective channel length which increases the channel resistance and lowers the I_{ON} . The channel resistance in the underlap region has been reduced via the incorporation of a high-k spacer. The high-k spacer also reduces the I_{OFF} due to high potential barrier in the OFF condition [27]. In this way, both I_{ON} and I_{OFF} improves with increasing spacer relative permittivity (ϵ_{sp}), as shown in Fig. 3. However, the use of the high-k spacer increases the parasitic capacitance in both the underlap and overlap structures.

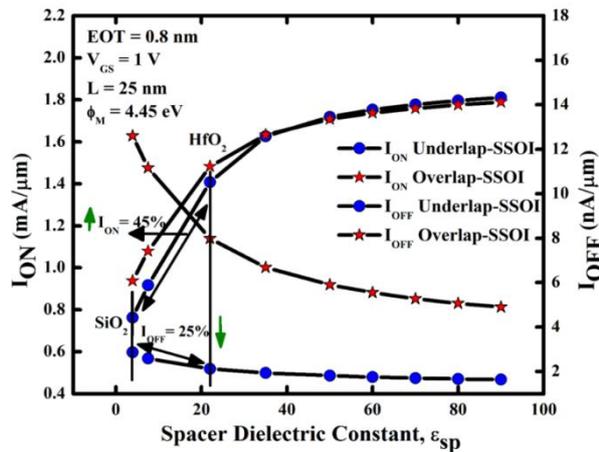


Fig. 3 ON and OFF current variation with spacer dielectric constant for underlap-SSOI and overlap-SSOI

The comparison of the total gate capacitances (C_{gg}) of the underlap-SSOI device versus that of the overlap-SSOI device, as a function of ϵ_{sp} , has been shown in Fig. 4. The total gate capacitance is combination of gate capacitance and parasitic capacitances i.e. overlap capacitance, outer fringe capacitance (C_{FO})

and inner fringe capacitance (C_{FI}). The value of parasitic capacitance depends upon the region of operation [28]. In the saturation condition, the parasitic capacitance is modeled with the equation for underlap devices as for overlap devices [29] and a similar trend is observed from simulation results – see Fig. 4.

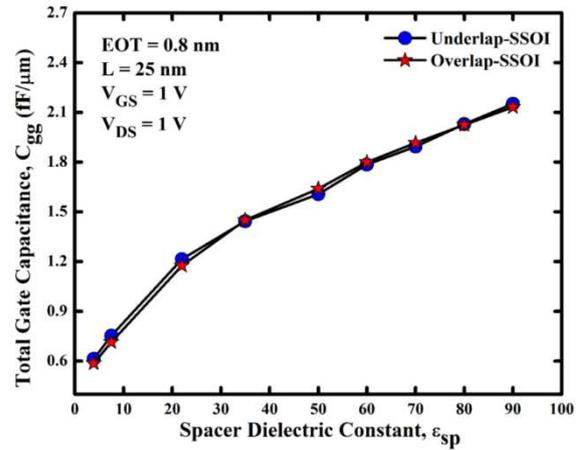


Fig. 4 Total gate capacitance dependence on spacer dielectric constant for underlap-SSOI and overlap-SSOI devices

For the high-k spacer, the larger C_{gg} value results in higher intrinsic gate delay (CV/I), as depicted in Fig. 5. In the underlap-SSOI device, we observe a 6% increase in delay for HfO₂ ($\epsilon_{sp} = 22$) spacer as compared to SiO₂ ($\epsilon_{sp} = 3.9$) spacer. On the other side, the HfO₂ spacer increases I_{ON} and decreases I_{OFF} by 45% and 25%, respectively, as shown in Fig. 3. It is important to note in Fig. 5 that the delay penalty of the underlap-SSOI device (using an HfO₂ spacer) is only 7% higher than that of the overlap-SSOI device, when the poor

turn ON characteristics of the underlap-SSOI structure is taken into account. However, the HfO₂ spacer has increased the I_{ON}/I_{OFF} ratio by 470% (calculated from Fig. 3) for the underlap-SSOI device compared to the overlap-SSOI device. Therefore, in many cases, such as low power and low frequency circuit design, this may be a beneficial trade-off.

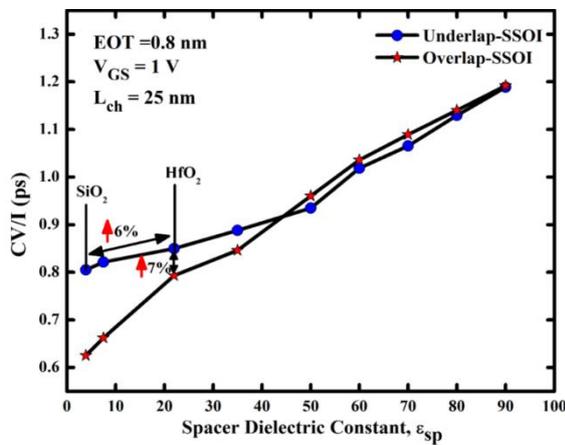


Fig. 5 Comparison of underlap-SSOI and overlap-SSOI delay (CV/I) penalty as a function of spacer dielectric constant

3. Impact of Strain on Various Parameters of Underlap-SSOI:

The use of strained Si as the channel material in MOSFET technology has attracted the interest of researchers due to significant resulting improvement in device performance. In the present work, the strained Si layer, without the presence of relaxed SiGe, is used as the channel in the underlap SOI device to avoid the disadvantages of the SiGe layer [30].

3.1 Strain Induced Bandgap Offset

Strain causes an energy offset in the conduction and valence bands of Si. The presence of strain causes the six-fold degenerate valleys of the conduction band minimum to split into two groups i.e. two lower valleys and four raised valleys. This leads to an offset in the conduction band, bandgap and density of states. These energy offsets have been modeled in the literature as a function of Ge mole fraction [31, 32] i.e. x :

$$(\Delta E_c)_{SSi} = E_{C,Si} - E_{C,SSi} = 0.57x \quad (1)$$

$$(\Delta E_g)_{SSi} = E_{G,Si} - E_{G,SSi} = 0.4x \quad (2)$$

$$V_T \ln \left(\frac{N_{V,Si}}{N_{V,SSi}} \right) = 0.075x \quad (3)$$

where x is Ge mole fraction, $(\Delta E_c)_{SSi}$ is conduction band offset due to strain, $E_{C,Si}$ is conduction band for unstrained silicon, $E_{C,SSi}$ is conduction band for strained silicon, $(\Delta E_g)_{SSi}$ is the bandgap offset due to strain, $E_{G,Si}$ is bandgap for unstrained silicon, $E_{G,SSi}$ is bandgap for strained silicon, V_T is the thermal voltage, $N_{V,Si}$ and $N_{V,SSi}$ are the density of states in the valence band in unstrained and strained Si respectively.

3.2 Strain Induced Flat Band Offset:

The changes in front channel flat-band voltage of underlap-SSOI, due to the offset in bandgap and conduction band can be given as³²:

$$(V_{\text{FB}_f})_{\text{SSi}} = (V_{\text{FB}_f})_{\text{Si}} + \Delta V_{\text{FB}_f} \quad (4)$$

where

$$(V_{\text{FB}_f})_{\text{Si}} = \phi_M - \phi_{\text{Si}}$$

$$\Delta V_{\text{FB}_f} = -(\Delta E_C)_{\text{SSi}} + (\Delta E_g)_{\text{SSi}} - V_T \ln \left(\frac{N_{V,\text{Si}}}{N_{V,\text{SSi}}} \right)$$

$(V_{\text{FB}_f})_{\text{SSi}}$ and $(V_{\text{FB}_f})_{\text{Si}}$ are the front channel flat-band voltage of strained and unstrained Si respectively, ΔV_{FB_f} change in front channel flat-band voltage due to strain, ϕ_M and ϕ_{Si} are the gate work function and unstrained Si work function respectively. In the same way, the back channel flat-band voltage of underlap-SSOI can be modified as given below:

$$(V_{\text{FB}_b})_{\text{SSi}} = (V_{\text{FB}_b})_{\text{Si}} + \Delta V_{\text{FB}_b} \quad (5)$$

where

$$(V_{\text{FB}_b})_{\text{Si}} = \phi_{\text{sub}} - \phi_{\text{Si}}$$

$$\Delta V_{\text{FB}_b} = -(\Delta E_C)_{\text{SSi}} + (\Delta E_g)_{\text{SSi}} - V_T \ln \left(\frac{N_{V,\text{Si}}}{N_{V,\text{SSi}}} \right)$$

ϕ_{sub} is the substrate work function.

Similarly, the built-in potential at the interface of source and channel in strained Si channel as a function of strain can be formulated as:

$$V_{\text{bi,SSi}} = V_{\text{bi,Si}} + (\Delta V_{\text{bi}})_{\text{SSi}} \quad (6)$$

where

$$V_{\text{bi,Si}} = \frac{E_{\text{g,Si}}}{2} + \phi_{F,\text{Si}}$$

$$(\Delta V_{\text{bi}})_{\text{SSi}} = -(\Delta E_g)_{\text{SSi}} + V_T \ln \left(\frac{N_{V,\text{Si}}}{N_{V,\text{SSi}}} \right)$$

4. Model Formulation:

The analytical threshold voltage model has been derived based upon the surface potential model by solving the 2D Poisson equation for the underlap-SSOI structure. This model formulation is different from the earlier model as the strain induced effect and the high-k spacer parameters have not been included in that model²⁴.

4.1 Formulation of Surface Potential

Fig. 1 shows the schematic of underlap-SSOI with high-k spacer around gate. Channel region, beneath gate and spacer dielectric, is break up into three regions: region1, region2 and region3 with L_1 , L & L_2 lengths respectively. The potential profile in Si channel before the strong inversion condition can be expressed by Poisson equation as [33]:

$$\frac{d^2 \phi(x, y)}{dx^2} + \frac{d^2 \phi(x, y)}{dy^2} = \frac{qN_A}{\epsilon_{\text{Si}}} \quad (7)$$

$$0 \leq x \leq L_1 + L + L_2, \quad 0 \leq y \leq t_{\text{SSi}}$$

where $\phi(x, y)$, ϵ_{Si} , N_A , L and t_{SSi} is the 2-D potential, dielectric constant of Si, p-type channel doping concentration, gate length

and strained Si body thickness respectively. region along y-axis is given as:

$$\phi(x, y) = \phi_s(x) + C_2(x)y^2 + C_1(x)y \quad (8)$$

The channel of underlap-SSOI has three regions and thereby potential distribution, ϕ given in Eq. (8) divided into three regions i.e. ϕ_1 , ϕ_2 and ϕ_3 as given below:

where ϕ_{s1} , ϕ_{s2} and ϕ_{s3} are the channel surface potentials under region1, region2 and region3 respectively.

Above coefficients $C_{11}(x)$ to $C_{32}(x)$ are functions of x (length along X-axis) and obtained via the following boundary conditions:

The electric flux continuity at the interface of strained Si-channel/gate-oxide, strained Si-channel/region1 and strained Si-channel/region2 is given as:

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} \left(\frac{\phi_{s2}(x) - V_{GS}'}{t_f} \right)$$

for region2 i.e. $L_1 \leq x \leq L_1 + L$

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{sp}}{\epsilon_{si}} \left(\frac{\phi_{s1}(x) - V_{GS}'}{t_{sp}} \right)$$

for region1 i.e. $0 \leq x \leq L_1$

$$\left. \frac{d\phi_3(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{sp}}{\epsilon_{si}} \left(\frac{\phi_{s3}(x) - V_{GS}'}{t_{sp}} \right)$$

for region3 i.e. $L_1 + L \leq x \leq L_1 + L + L_2$

The effective gate to source voltage (V_{GS}') is given by

$$V_{GS}' = V_{GS} - (V_{FB-f})_{SSi} \quad (15)$$

where V_{GS} is the applied gate to source bias voltage V_{FB-b} is the back channel flat-band voltage.

Mathematically, surface potential at source end is described as:

$$\phi_1(x, y) = \phi_{s1}(x) + C_{11}(x)y + C_{12}(x)y^2 \quad (9)$$

for $0 \leq x \leq L_1$, $0 \leq y \leq t_{SSi}$

$$\phi_2(x, y) = \phi_{s2}(x) + C_{21}(x)y + C_{22}(x)y^2 \quad (10)$$

for $L_1 \leq x \leq L_1 + L$, $0 \leq y \leq t_{SSi}$

$$\phi_3(x, y) = \phi_{s3}(x) + C_{31}(x)y + C_{32}(x)y^2 \quad (11)$$

for $L_1 + L \leq x \leq L_1 + L + L_2$, $0 \leq y \leq t_{SSi}$

$$\phi_1(0, 0) = \phi_{s1}(0) = V_{bi,SSi} \quad (16)$$

Similarly, surface potential at drain end is described as:

$$\phi_3(L_1 + L + L_2, 0) = \phi_{s3}(L_1 + L + L_2) = V_{bi,SSi} + V_{DS} \quad (17)$$

Electric flux at the interface of BOX/back channel is continuous for all three regions and is given as:

Electric flux at the interface of BOX/back channel is continuous for all three regions and is given as:

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=t_{SSi}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{[V_{sub}' - \phi_B(x)]}{t_b} \quad (18)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=t_{SSi}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{[V_{sub}' - \phi_B(x)]}{t_b} \quad (19)$$

$$\left. \frac{d\phi_3(x, y)}{dy} \right|_{y=t_{SSi}} = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{[V_{sub}' - \phi_B(x)]}{t_b} \quad (20)$$

where t_b and ϕ_b is the BOX thickness and back channel potential at the BOX/strained

Si-channel interface respectively. Effective substrate bias voltage is given as $V_{sub}' = V_{sub} - (V_{FB_b})_{SSi}$ where V_{GS} is the applied gate to source bias voltage. Electric flux continuity at the interface of spacer1/metal-gate and spacer2/metal-gate is represented as:

$$\left. \frac{d\phi_1(x, y)}{dx} \right|_{x=L_1} = \left. \frac{d\phi_2(x, y)}{dx} \right|_{x=L_1} \quad (21)$$

$$\left. \frac{d\phi_3(x, y)}{dx} \right|_{x=L_1+L} = \left. \frac{d\phi_2(x, y)}{dx} \right|_{x=L_1+L} \quad (22)$$

Surface potential in region1, region2 and region3 is continuous which is given as:

$$\phi_{s1}(L_1, 0) = \phi_{s2}(L_1, 0) \quad (23)$$

$$\phi_{s2}(L_1 + L, 0) = \phi_{s3}(L_1 + L, 0) \quad (24)$$

The coefficients $C_{11}(x)$ to $C_{32}(x)$ given in equations (9)-(11) are calculated by boundary conditions (12)-(14) and (18)-(20). By taking the derivative of equations (9)-(11) as per equation (7) which result in following equation:

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha_1\phi_{s1}(x) = \beta_1 \quad (25)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha_2\phi_{s2}(x) = \beta_2 \quad (26)$$

$$\frac{d^2\phi_{s3}(x)}{dx^2} - \alpha_3\phi_{s3}(x) = \beta_3 \quad (27)$$

where $\alpha_1, \alpha_2, \alpha_3, \beta_1, \beta_2$ and β_3 are constants and their calculated values are given below:

$$\alpha_1 = \alpha_3 = \frac{2 \left(1 + \frac{c_s}{c_b} + \frac{c_s}{c_{si}} \right)}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \quad (28)$$

$$\alpha_2 = \frac{2 \left(1 + \frac{c_f}{c_{si}} + \frac{c_f}{c_{si}} \right)}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \quad (29)$$

$$\beta_1 = \beta_3 = \frac{qN_A}{\epsilon_{si}} - 2 \left(\frac{V_{GS} \left(\frac{c_s}{c_b} + \frac{c_s}{c_{si}} \right)}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \right) - 2V_{sub} \left(\frac{1}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \right) \quad (30)$$

$$\beta_2 = \frac{qN_A}{\epsilon_{si}} - 2 \left(\frac{V_{GS} \left(\frac{c_f}{c_b} + \frac{c_f}{c_{si}} \right)}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \right) - 2V_{sub} \left(\frac{1}{t_{SSi}^2 \left(1 + 2 \frac{c_{si}}{c_b} \right)} \right) \quad (31)$$

In the above model equations (28)-(31), capacitances values are front gate oxide ($C_f = \epsilon_{ox}/t_f$), BOX capacitance ($C_b = \epsilon_{box}/t_b$) and strained silicon channel capacitance ($C_{si} = \epsilon_{si}/t_{SSi}$). The equations (25)-(27) is solved further for formulating the surface potential for three different regions i.e. Region1, Region2 and Region3 as follows:

$$\phi_{s1}(x) = Ae^{\sqrt{\alpha_1}x} + Be^{-\sqrt{\alpha_1}x} - \frac{\beta_1}{\alpha_1} \quad (32)$$

$$\phi_{s2}(x) = Ce^{\sqrt{\alpha_2}(x-L_1)} + De^{-\sqrt{\alpha_2}(x-L_1)} - \frac{\beta_2}{\alpha_2} \quad (33)$$

$$\phi_{s3}(x) = Ee^{\sqrt{\alpha_1}[x-(L+L_1)]} + Fe^{-\sqrt{\alpha_1}[x-(L+L_1)]} - \frac{\beta_1}{\alpha_1} \quad (34)$$

4.2 Formulation of Threshold Voltage

In this section, the threshold voltage is obtained by solving the surface potential equations for the underlap-SSOI device structure. It is well known that the threshold voltage is the gate voltage (V_{GS}) at which the minimum surface potential ($\phi_{s,min}$) in channel region is equal to twice the body Fermi potential (ϕ_F). The $\phi_{s,min}$ occurs at the minimum value of x (x_{min}). The x_{min} is derived from equation (32) as follows:

$$x_{min} = \frac{1}{2\sqrt{\alpha_1}} \times \ln\left(\frac{B}{A}\right) \quad (35)$$

$$\phi_{s,min} = \phi_{th} = 2\sqrt{AB} - \frac{\beta_1}{\alpha_1} \quad (36)$$

The $\phi_{s,min}$ is equal to the threshold potential (ϕ_{th}) because ϕ_{th} is the minimum potential at which surface carrier density get inverted. The A and B factors are determined from (32)-(34) by using boundary conditions described in (16)-(17) and (21)-(24) respectively. The calculated value of A and B are given below:

$$A = \frac{V_{bi2} - V_{GS} \left(ze^{-\sqrt{\alpha_1}L_1} \left(\sqrt{\frac{\alpha_1}{\alpha_2}} - \tanh\sqrt{\alpha_2}L \right) + y_1 \right)}{2 \left(\sqrt{\frac{\alpha_1}{\alpha_2}} \cosh\sqrt{\alpha_1}L_1 + \sinh\sqrt{\alpha_1}L_1 \tanh\sqrt{\alpha_2}L \right)} \quad (37)$$

$$B = \frac{V_{bi1} - V_{GS} \left(ze^{\sqrt{\alpha_1}L_1} \left(\sqrt{\frac{\alpha_1}{\alpha_2}} - \tanh\sqrt{\alpha_2}L \right) + y_2 \right)}{2 \left(\sqrt{\frac{\alpha_1}{\alpha_2}} \cosh\sqrt{\alpha_1}L_1 + \sinh\sqrt{\alpha_1}L_1 \tanh\sqrt{\alpha_2}L \right)} \quad (38)$$

where the associated constants are given as:

$$V_{bi1} = (V_{bi,SSi} - u) \left(e^{\sqrt{\alpha_1}L_1} \left(\sqrt{\frac{\alpha_1}{\alpha_2}} + \tanh\sqrt{\alpha_2}L \right) \right) + (u - v) \tanh\sqrt{\alpha_2}L$$

$$V_{bi2} = (V_{bi,SSi} - u) \left(e^{-\sqrt{\alpha_1}L_1} \left(\sqrt{\frac{\alpha_1}{\alpha_2}} - \tanh\sqrt{\alpha_2}L \right) \right) + (v - u) \tanh\sqrt{\alpha_2}L$$

$$z = \frac{\left(\frac{C_s}{C_b} + \frac{C_s}{C_{Si}} \right)}{\left(1 + \frac{C_s}{C_b} + \frac{C_s}{C_{Si}} \right)},$$

$$y_1 = (z - 1) \tanh\sqrt{\alpha_2}L \quad \text{and} \quad y_2 = (1 - z) \tanh\sqrt{\alpha_2}L$$

The gate to source voltage (V_{GS}) is derived by solving (36) using (37, 38). Here, the V_{GS} is solved for minimum surface potential condition and it is defined as threshold voltage V_{th} as follows:

$$V_{GS} = V_{TH} = \frac{-V_{t1} + \sqrt{V_{t1}^2 - 4\gamma V_{t2}}}{2\gamma} \quad (39)$$

where the values of constants i.e. V_{t1} , V_{t2} and γ are given in appendix.

5. Model Validation and Discussion

In Fig. 6, both the model and simulated data points of the surface potential have been plotted along the channel direction for underlap-SOI device at $V_{DS} = 0.2$ V, 0.5 V and 1 V. It is observed from the figure that there is insignificant change occurring in surface potential under the gate terminal due to the presence of Gate-S/D underlap region. The impact of the drain potential has been restricted near the drain terminal only. Consequently, the drain voltage has less control over the ON current after

saturation, which is required for low power circuit design. It is seen in the inset of Fig. 6 that the surface potential minimum is shifted only 17 mV when the drain potential is increases from 0.2 V to 1 V. This lower change in the position of surface potential minima with drain voltage leads to reduced DIBL for underlap-SOI device. Further, the model results track the numerical results very closely which establishes the accuracy of the proposed model.

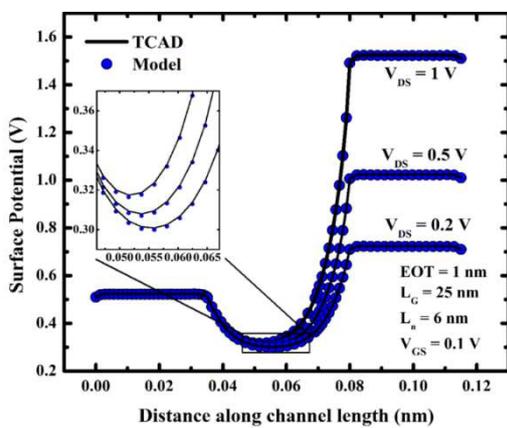


Fig. 6 Surface potential distribution along the channel length for underlap-SOI at different drain voltages i.e. $V_{DS} = 0.2$ V, 0.5 V and 1 V

The variation of threshold voltage of underlap-SSOI with Ge mole fraction (x) is shown in Fig. 7. A larger value of x reduces the energy bandgap since the bandgap offset is directly proportional to x , as given in (2). Consequently, the flat-band voltage and built-in potential at S/D-channel interface has decreased. This causes the earlier onset of inversion layer in strained Si and leads to decrease in threshold voltage as shown in Fig. 7. Very

high value of x (generally greater than 0.4) for a given channel thickness leads to strain relaxation due to formation of dislocations [34]. Thus, strain relaxation puts the upper limit on x value. On the other side, the lower value of x reduces the ON current due to the increase in threshold voltage. Thus, the optimum value of x can be obtained according to the required value of threshold voltage. Further, the threshold voltage calculated from model equations follow the simulation results closely thereby establishing the model accuracy.

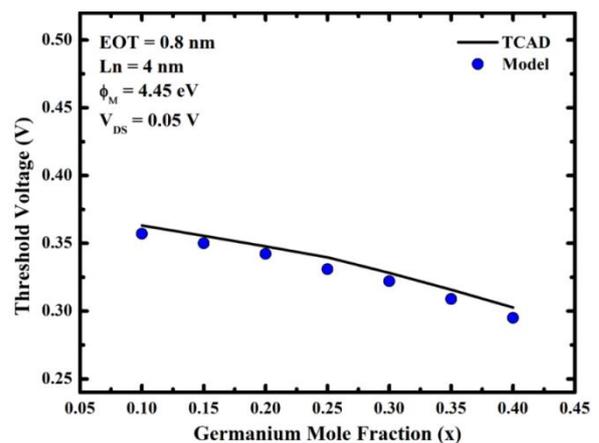


Fig. 7 Variation of threshold voltage with Ge mole fraction.

Fig. 8 demonstrates the threshold voltage as a function of underlap length for different value of Ge mole fraction; $x = 0.2$, 0.25 and 0.3. Here the negative values of underlap length represent the overlap length between gate and S/D regions. The threshold voltage is found to be increasing with increase in underlap length. This owes to increase in series resistance for higher

value of underlap length. In this way, underlap structure provides additional flexibility to achieve the desired value of the threshold voltage.

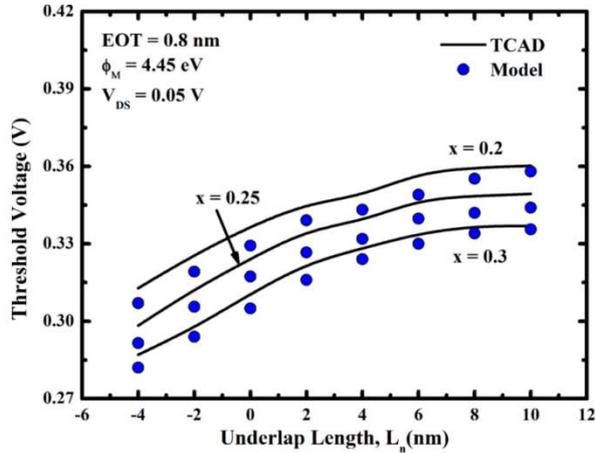


Fig. 8 Variation of threshold voltage with underlap length at different mole fraction i.e. $x = 0.2$, $x = 0.25$ and $x = 0.3$

The threshold voltage decreases with decrease in channel length from 90 nm to 15 nm as seen in Fig. 9. Reduction in threshold voltage with channel length is called as threshold voltage roll-off (ΔV_{TH}). This is undesirable effect and it should be low for high performance nanoscale devices. The presence of S/D underlap region increases the threshold voltage (as observed in Fig. 8) which helps to reduce the ΔV_{TH} with the channel length scaling. Consequently, low value of $\Delta V_{TH} = 25$ mV is observed in underlap-SSOI device as compared to $\Delta V_{TH} = 100$ mV of ref. 35.

The metal gate work function is a key parameter in obtaining the threshold voltage. Fig. 10 shows the plot of the

threshold voltage versus metal gate work function. It is clear that the threshold voltage becomes large for higher values of the metal gate work function since the metal gate work function has a direct relationship with the threshold voltage. The same trend is found in Fig. 10 and the model values closely follow the simulated values.

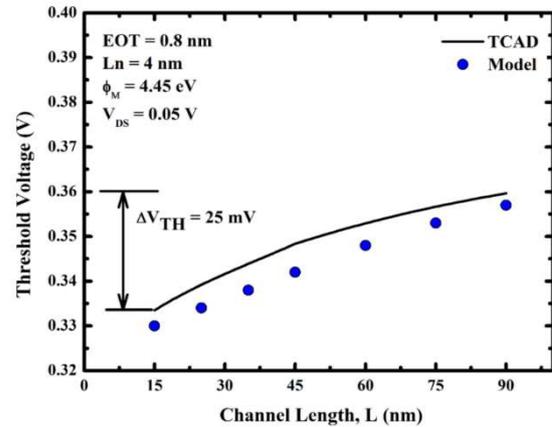


Fig. 9 Reduction of threshold voltage with decreasing channel length

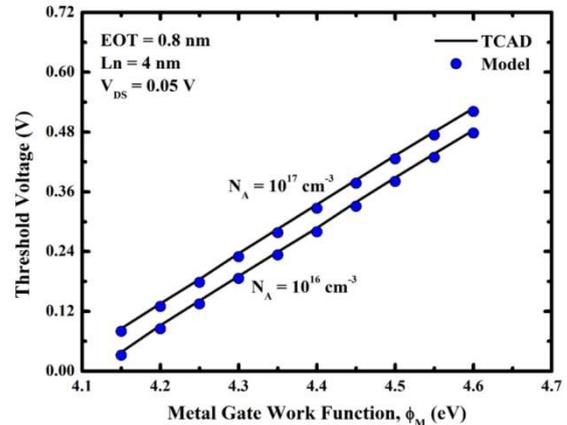


Fig. 10 Variation of threshold voltage with gate work function at channel doping concentration $N_A = 10^{17} \text{ cm}^{-3}$ and $N_A = 10^{16} \text{ cm}^{-3}$

6. Conclusion

In this work, an underlap-SSOI structure with high-k spacer is proposed to mitigate

the leakage current and SCEs with the aim of enabling continued scaling for low power applications. Inclusion of underlap region in SOI structure exponentially reduces the leakage current i.e. 509%. On the other hand, underlap region degrades the ON current. In proposed structure, ON current enhances by incorporating strained Si and a high-k spacer region, without degrading the intrinsic delay of the proposed device. Using HfO₂ as the material for the high-k spacer region allows direction of the gate-fringing field towards the channel region, which helps to enhance the ON current by 45% as well as reducing the OFF current by 25%. Further, a 2D threshold voltage model is formulated for the underlap-SSOI structures by incorporating strain induced effects to formulate a new analytical model. The close match between model results and numerical simulations establishes the accuracy of proposed model. The model results show that the proposed structure achieves lower threshold-voltage roll off and provides enhanced controllability on threshold voltage as compared to conventional SOI MOSFETs.

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- **Code availability** Not Applicable
- **Authors' contribution:** Design, Methodology, Formal analysis, and investigation, Validation, Writing - original draft preparation: [Rajneesh Sharma]; Conceptualization, Resources, Supervision: [Ashwani K. Rana]; Writing - review and editing: [Shelza Kaushal, Justin B. King and Ashish Raman]
- **Authors' information:** Not Applicable
- **Acknowledgements:** Not Applicable
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- **Consent for publication:** Not Applicable

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Figures

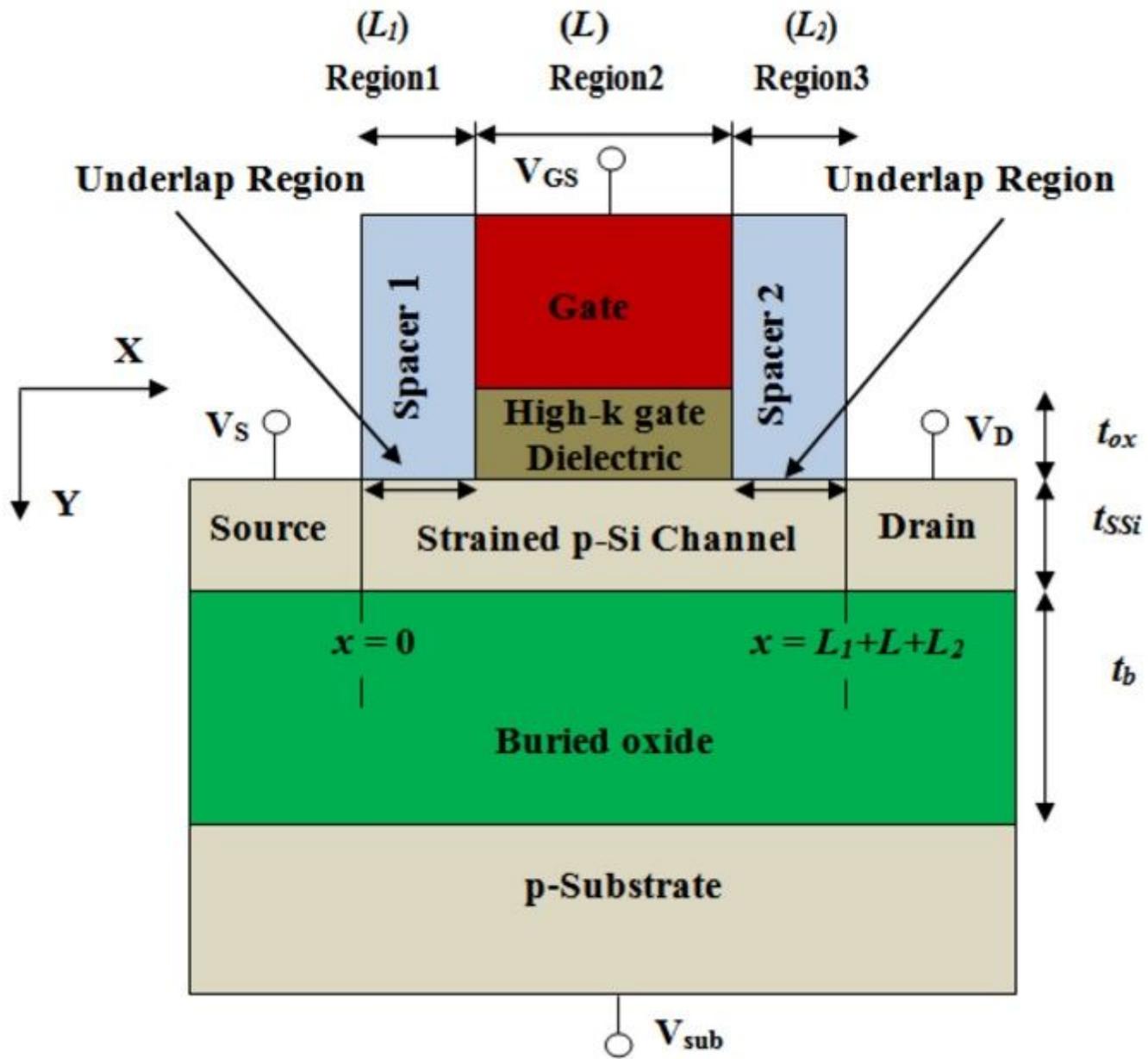
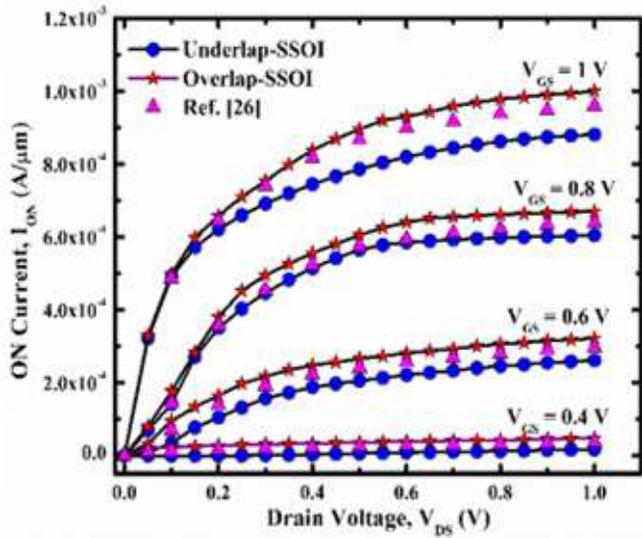
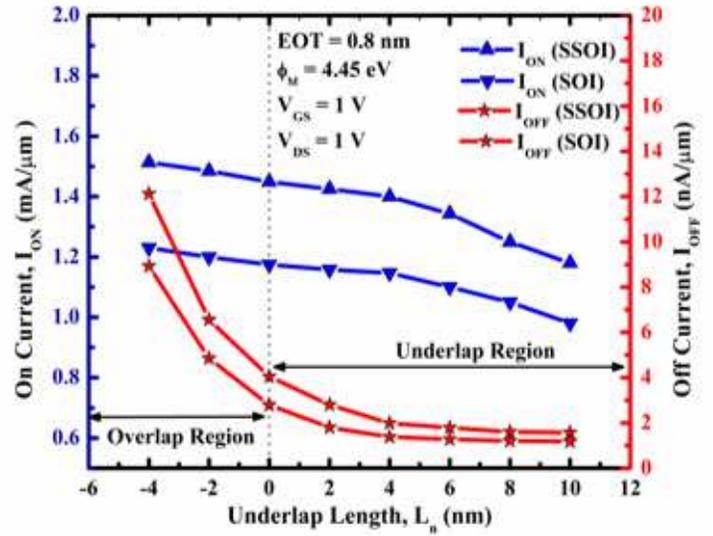


Figure 1

Schematic structure of Underlap-SSOI with associated physical parameters



(a)



(b)

Figure 2

Fig. 2 (a) ON current vs drain voltage for $\chi_M = 4.4$, EOT = 1. (b) Variation in ON and OFF current with underlap length for strained SOI and unstrained SOI. Other parameters: $x = 0.25$, $t_{SSi} = 6$ nm and $L = 25$ nm.

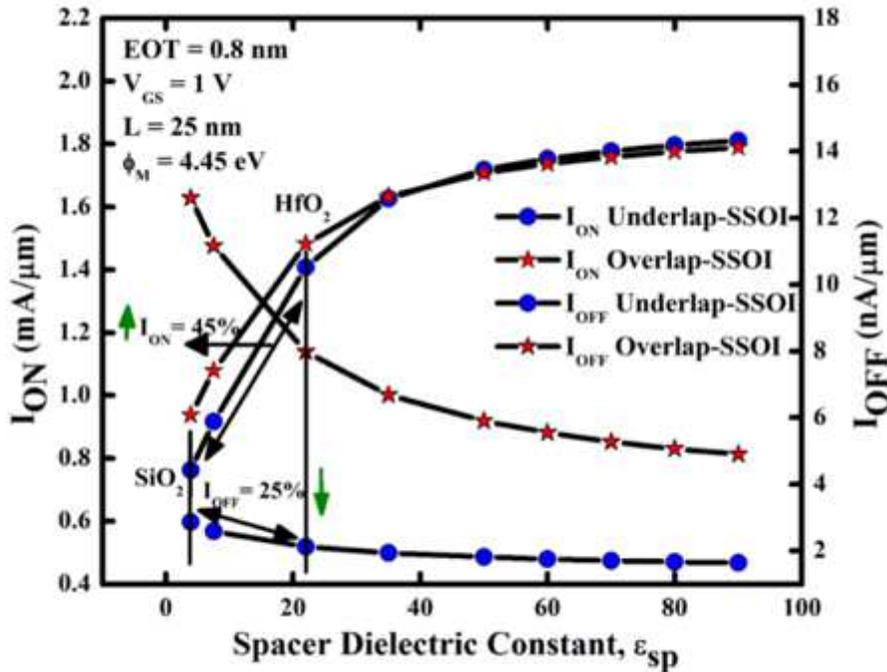


Figure 3

ON and OFF current variation with spacer dielectric constant for underlap-SSOI and overlap-SSOI

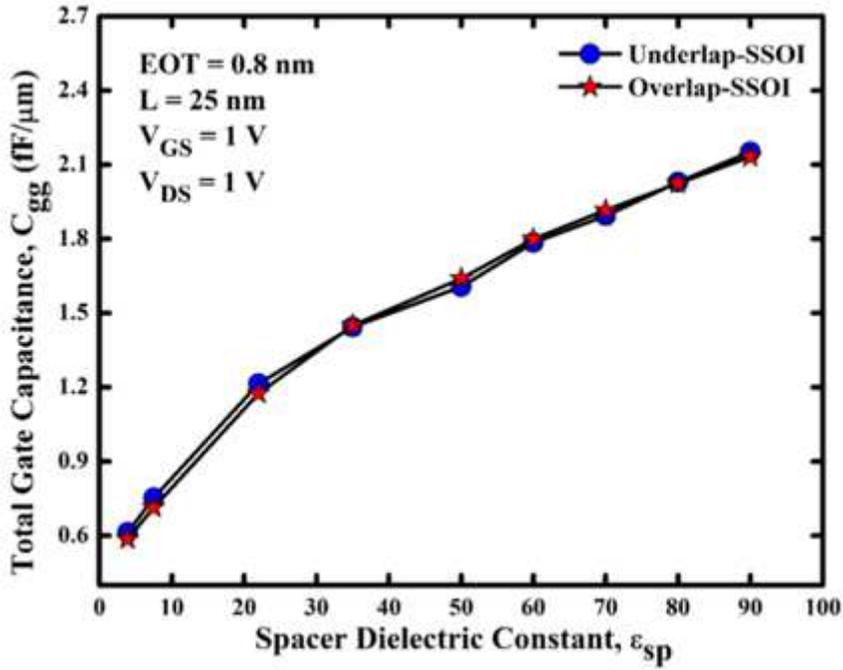


Figure 4

Total gate capacitance dependence on spacer dielectric constant for underlap-SSOI and overlap-SSOI devices

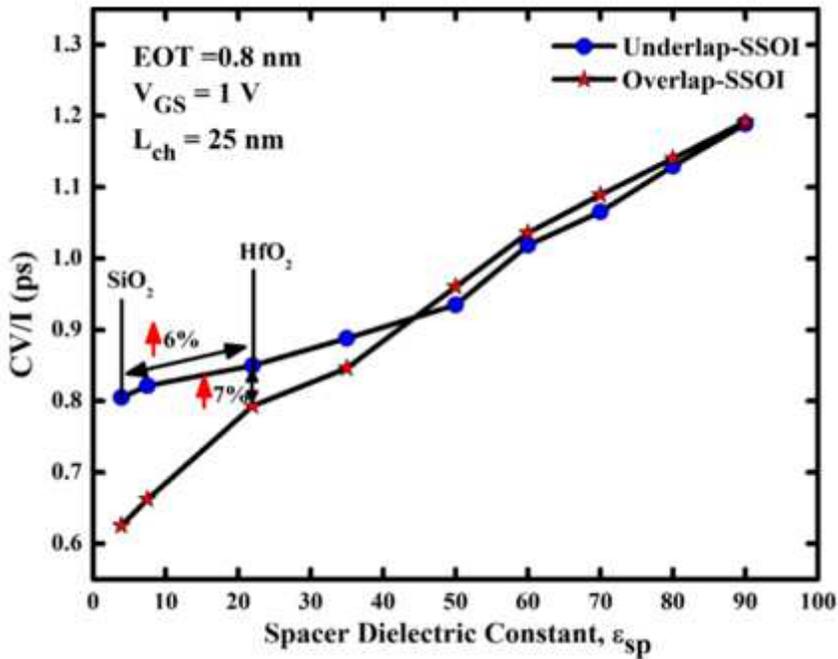


Figure 5

Comparison of underlap-SSOI and overlap-SSOI delay (CV/I) penalty as a function of spacer dielectric constant

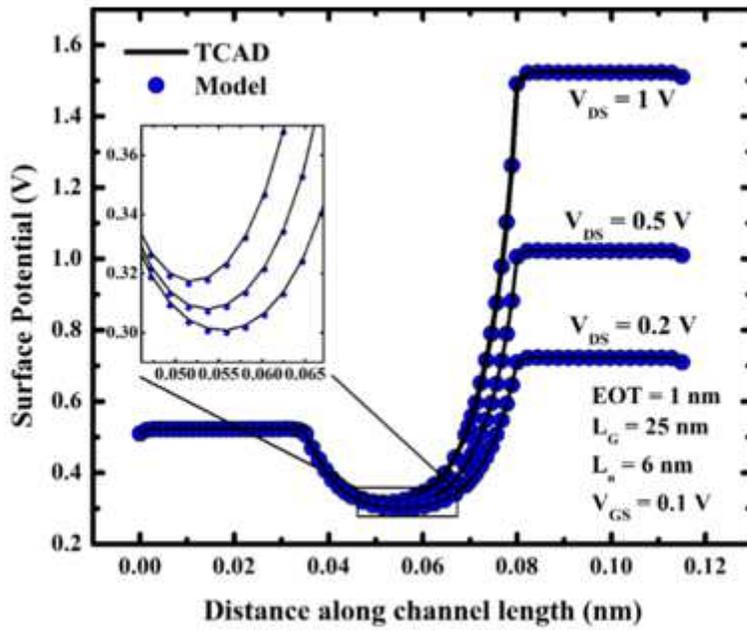


Figure 6

Surface potential distribution along the channel length for underlap-SOI at different drain voltages i.e. $V_{DS} = 0.2\text{ V}, 0.5\text{ V}$ and 1 V

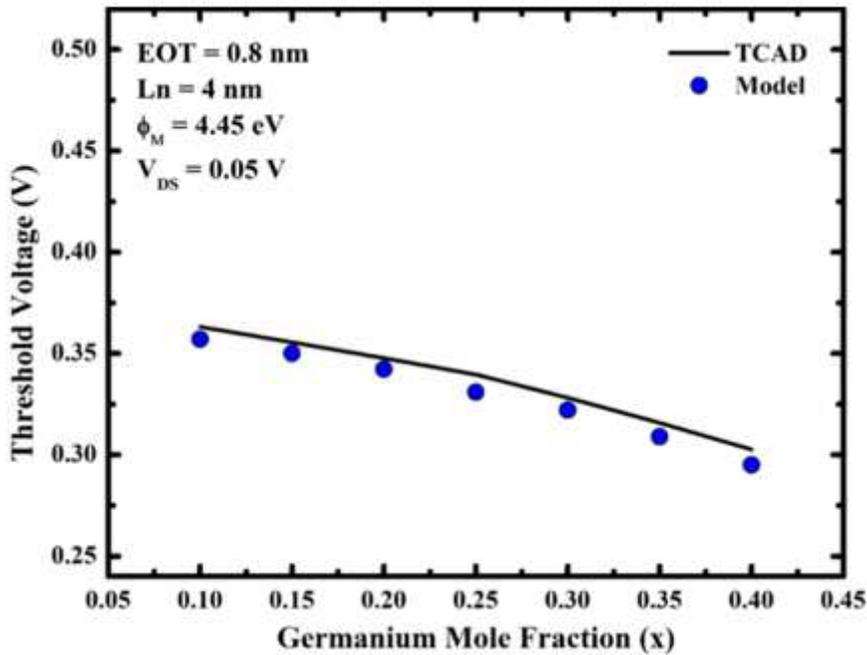


Figure 7

Variation of threshold voltage with Ge mole fraction.

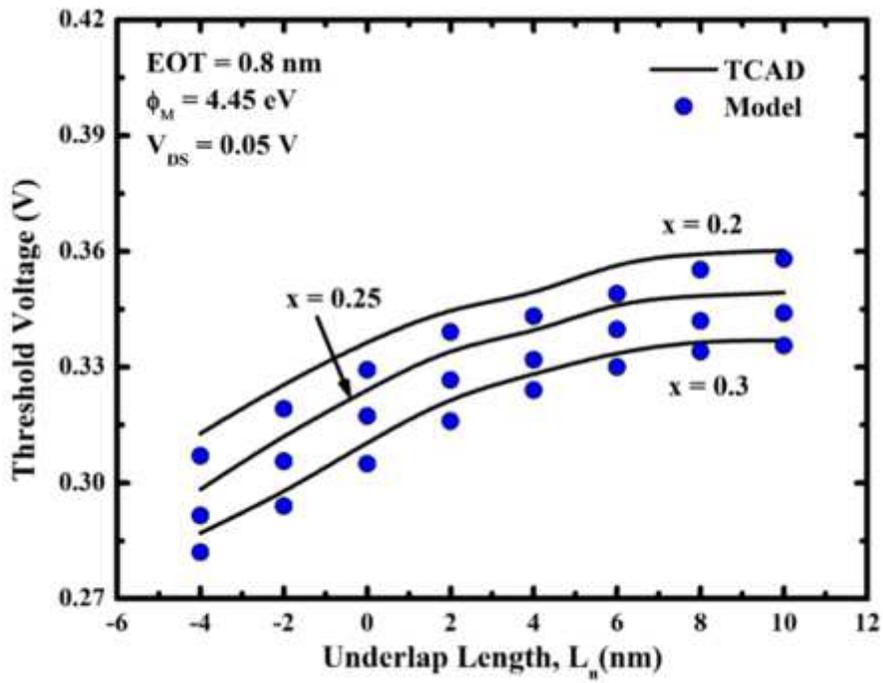


Figure 8

Variation of threshold voltage with underlap length at different mole fraction i.e. $x = 0.2$, $x = 0.25$ and $x = 0.3$

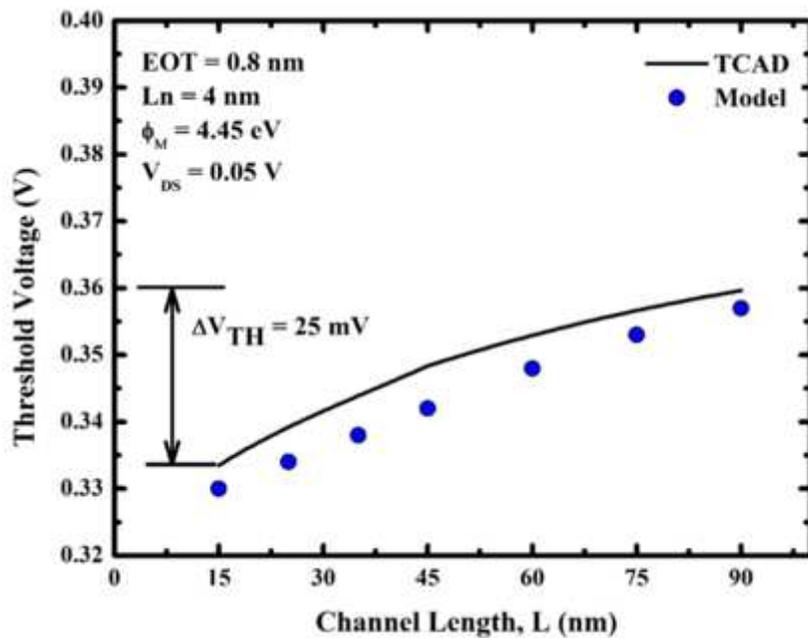


Figure 9

Reduction of threshold voltage with decreasing channel length

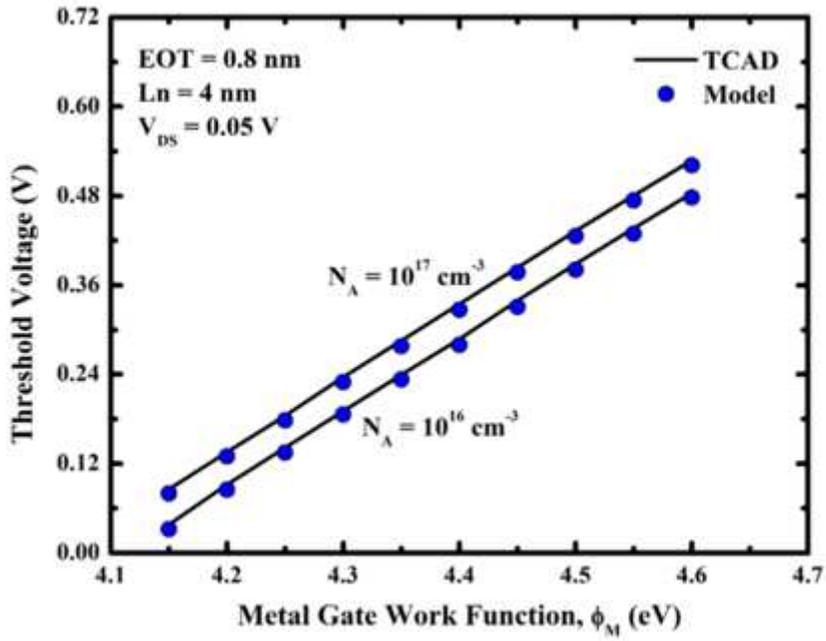


Figure 10

Variation of threshold voltage with gate work function at channel doping concentration $N_A = 10^{17} \text{ cm}^{-3}$ and $N_A = 10^{16} \text{ cm}^{-3}$