A Novel Design and Evaluation of a Low Power Efficient Fault-Tolerant Reversible ALU Using QCA: Applications of Nanoelectronics

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A Novel Design and evaluation of a low power efficient Fault-Tolerant Reversible ALU Using QCA: Applications of Nanoelectronics

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Abstract: Reversible logic based on Quantum-dot Cellular Automata (QCA) is the most requirement for achieving nano-scale architecture that promises significantly high device integration density, high-speed calculation, and low power consumption. The arithmetic logic unit (ALU) is the significant component of a processor for processing and computing. The primary objective of this work is to develop a multi-layer fault-tolerant arithmetic logic unit using reversible logic in QCA technology. Additionally, the reversible ALU has divided into arithmetic (RAU) and a logic unit (RLU). A reversible 2:1 MUX using the Fredkin gate has been implemented to select either the arithmetic or logical operations. Besides, to improve the efficiency of arithmetic operations, a novel QCA reversible full adder is implemented. To build the ALU, fault-tolerant reversible logic gates are used. The proposed reversible multilayer QCA ALU is designed to carry out eight arithmetic and sixteen logical operations with a minimum number of gates, constant inputs, and garbage outputs compared to the existing works. The functional verification and simulation of the presented circuits are assessed by the QCADesigner tool.

Keywords: Quantum-dot cellular automata (QCA), reversible logic, fault tolerance, ALU.

1. Introduction

Following Moore's law, CMOS technology has reached the size of tens of nanometers. The scaling of transistor size results in short-channel effects, leakage power, high power dissipation, low package density, physical and economic challenges. Researchers have proposed quantum-dot cellular automata (QCA) as a substitute for the CMOS VLSI technology. The potential advantages of this technology are ultra-low-power dissipation, less area, high packaging density, fast computing, and high operating frequency when compared to the CMOS technology. In the conventional technologies, the data is carried by passing electric current whereas in QCA by polarization states. According to Landauer, an irreversible operation dissipates the energy of KTln2 Joules due to a transition from input to output where temperature T is measured in Kelvin and K represents Boltzmann's constant [1]. For avoiding energy loss during the signal transition, Benett had introduced reversible circuits made up of reversible gates [2]. The energy dissipation in reversible logic gates avoided by mapping each n bit input to an n bit output. The main factors to be considered while designing circuits using reversible logic gates are quantum cost, the number of garbage outputs, constant inputs, and the number of gates is to be minimum. Researchers have introduced reversible logic gates like Fredkin, FG, F2G, Toffoli, RUG, KMD, PG, MKG, IG, HNG, RM [6-12] to design a reversible logic circuit. But a few gates addressed as in above have fault tolerance property. ALU (Arithmetic Logic Unit) is the base of most quantum computers. Reliability in reversible computation is a big concern .A fault-tolerant system can keep its properties correct in the case of failure also. The purpose of this paper is to integrate fault tolerance with the property in the architecture of ALU using parity preservation gates of reversible logic. It's not only going to minimize hardware overhead, but it also prohibits additional design efforts for designing of a fault-tolerant ALU using parity conservative logic gates. The design

of ALUs suggested so far has to be improved in terms of the performance metrics like quantum cost, number of gates, number of garbage inputs, constant inputs, complexity, area, and number of operations. So, we recommend a high-performance reversible fault tolerant ALU in QCA with more number of functions and less number of gates in this paper. The essential contributions from this work indicated as follows:

- Proposes a cost-effective reversible 2X1 MUX circuit in QCA with a parity preserving gate.
- Addresses a novel reversible fault tolerant full adder circuit in QCA for optimization in designing the ALU circuit.
- Designs a single bit ALU with the suggested QCA full adder and the 2X1 MUX with the improved number of operations, number of gates, garbage inputs, and constant inputs.
- Compares the proposed ALU work with the related existing works.

The remaining of the article is structured as follows. The review of QCA technology and reversible logic is discussed in section 2. The related works are presented in section 3. Section 4 introduces a novel QCA based on a reversible 2:1multiplexer and single-bit full adder circuits. The proposed reversible QCA based ALU is presented in section 5. The simulation results and comparison with similar works are analyzed in section 6. The observations are concluded in section 7.

2. Preliminaries

Basics of QCA technology and reversible logic are discussed in this section.

2.1. QCA basics

The basic cell used in designing QCA circuits is a QCA cell which consists of four quantum dots in a square-shaped nanostructure as can be seen in Figure 1. In a QCA cell, a polarization P is formulated as

$$P = \frac{(e1+e3)-(e2+e4)}{e1+e2+e3+e4} \quad (1)$$

Where ei denotes the electronic charge on dot i. The QCA cell with polarization -1 represents logic '0' and polarization 1 for logic '1'. When a QCA cell is positioned near a carrier cell that has a fixed polarisation, the cell would match its polarisation with its carrier cells. Hence the data interaction between the neighboring QCA cells can be transmitted across a series of cells as shown in Figure 2.

Insert Fig. 1

Insert Fig. 2

The basic logic gates used in QCA are a majority gate and an inverter and their examples are displayed in Figure 3. The basic function of a 3-input majority gate with inputs p,q,r, and output Y is given by

$$Y=M(p,q,r)= pq + qr +rp \quad (2)$$

Insert Fig. 3

An AND gate is constructed by using the majority gate by keeping one of the inputs as logic 0. The expression for an AND gate with two inputs p,q and on output Y is given by

$$Y=M(p,q,0)=pq \quad (3)$$

In the same way, an OR gate is constructed by keeping one of the inputs as logic 1. The 2-input OR gate is given by equation 4.

$$Y=M(p,q,1)=p+q \quad (4)$$

The two-wire crossings available in QCA technology are co-planner and multilayer crossings. Both standard and rotated cells are used by a coplanar crossover. The two kinds of cells do not interfere with one another if they are correctly positioned. Multilayer crossovers are implemented by using more number of layers. It is more reliable compared to the co-planner crossover. QCA circuits operate accurately if they are clocked properly. In QCA, clocking not just to regulates the flow of data, but also acts as the source of electricity. There are four types of clocking available in QCA.They are clocking zone 0,clocking zone 1,clocking zone 2 and clocking zone 3. A typical clocking scheme used in QCA is as shown in Figure 4.

Insert Fig. 4

2.2 Reversible logic

Computers available now are smaller, quicker, and more complicated. All the logical operations in these computers are considered irreversible. Some data erased each time the logic operation has performed in irreversible logic. Due to this, the power consumption has increased. Thus, the implementation of reversible logic circuits that does not delete information is one promising future computing technology to reduce power consumption. A reversible system must be able to work in a reverse direction. That is, the outputs recovered from their inputs. The measurable parameters of reversible circuits are:

Garbage outputs

Garbage outputs are required to make a function reversible. They are not the actual outputs of the system.

Constant inputs

Constant inputs are the inputs with a fixed value that are required to make a function reversible.

Logical calculations

Logical calculations of a reversible circuit give the total number of NOT, AND, and XOR operations needed for realizing a function.

Quantum Cost

The Quantum Cost (QC) of a circuit with reversible logic is the complete number of 2x2 size quantum primitives to frame a proportionate quantum circuit.

The fault-tolerant reversible gates utilized in synthesizing the proposed circuits are described as follows:

1.RUG

RUG is a 3X3 fault tolerant reversible gate. The three inputs (A, B, C) mapped to the three outputs (P, Q, R). The block diagram of the RUG is displayed in Figure 5 and its schematic diagram in Figure 6. The QCA realization of the RUG is as seen in Figure 7. Figure 8 depicts its simulation result.

Insert Fig. 5

Insert Fig. 6

Insert Fig. 7

Insert Fig.8

2.F2G

Double Feynman gate(F2G) is a 3X3 fault tolerant reversible gate. The block diagram of the F2G and its corresponding schematic diagram is as depicted in Figure 9.a & b. The QCA realization of the F2G is as displayed in Figure 9..c. Figure 10 shows the simulation result of the F2G gate.

Insert Fig. 9

Insert Fig.10

3.FRG

Fredkin gate(FRG) is a 3X3 fault tolerant reversible gate. The block diagram of the FRG is as seen in Figure 11 and its corresponding schematic diagram in Figure 12. The QCA realization of the FRG is as presented in Figure 13 and its simulation output in Figure 14.

Insert Fig. 11

Insert Fig. 12

Insert Fig. 13

Insert Fig.14

4.FG

Feynman gate(FG) is a 2X2 reversible gate. The block diagram of the FG and its corresponding schematic diagram is as seen in Figure 15. The QCA realization and simulation result of the FG are displayed in Figures 16 and 17.

Insert Fig. 15

Insert Fig. 16

Insert Fig.17

5.UPPG

Universal parity preserving gate(UPPG) is a 4X4 reversible gate. The structure of the UPPG is as seen in Figure 18 and its corresponding schematic diagram in Figure 19. The QCA realization and simulation result of the UPPG is as presented in Figure 20 and 21 respectively.

Insert Fig. 18

Insert Fig. 19

Insert Fig. 20

Insert Fig.21

3.Related work

Different approaches have been implemented in recent years to enhance the performance of elements of the ALU. There are, however, only a few architectures suggested for designing QCA ALU. The authors have suggested a 4-bit QCA ALU in [3]. This approach uses three layers, 420 QCA cells, latency in three clock zones, and an area of 0.85 μm2. This layout is not using the fault-tolerant reversible gates as well as it is using more number of QCA cells to implement. The authors suggested a method to implement QCA ALU capable of performing 12 logic and arithmetic operations[4]. But, this approach uses 485 QCA cells, an area of 0.79 μm2, and latency of five clock zones. There are many drawbacks to this process, as the absence of reversibility, exclusion of fault tolerance, high consumption of cells, and also high latency. Trailokya Nath Sasamal et al.[5] designed a reversible ALU in QCA using the coplanar crossing. But the proposed design uses more number of QCA cells and performs only 20 ALU operations only. In [13], the authors constructed a reversible QCA ALU using a reversible MUX. However, the design is able to perform only 16 operations with more number of constant inputs and garbage outputs. Sasamal et al.[14] propose a QCA ALU using reversible logic. They considered a 3X3 RUG fault tolerant reversible gate as a fundamental element in synthesizing reversible ALU design. But it can perform only 16 ALU operations only. The authors [15] propose an integrated fault-tolerant QCA ALU using KMD reversible gates. The suggested design can be able to perform only 18 operations with an increased number of constant inputs, gates, and garbage outputs.

4. Reversible MUX and full adder

4.1 Reversible MUX

Using Fredkin's reversible logic gate, a novel 2:1 MUX has been constructed in QCA technology. All the potential benefits with this proposed new multiplexer seem to be reversible logic that is not present in the traditional MUX. One of the crucial characteristics in designing the logic circuit using reversible gates is to reduce the count of reversible gates and garbage outputs. The schematic diagram of the proposed MUX is as shown in Figure 22 and its QCA layout in Figure 23. The designed circuit utilizes only 75 QCA cells, only one gate, and an area of 0.08μm2. Figure 24 depicts the simulation result of the suggested 2:1 MUX.

Insert Fig. 22

Insert Fig. 23

Insert Fig.24

4.2 Full adder

The proposed reversible fault tolerant full adder circuit is designed using RUG and F2G gates. The schematic diagram and QCA layout of the suggested circuit is as shown in Figure 25 and 26 respectively. It utilizes a very less cell count of 107 QCA cells compared to its earlier designs. The circuit is said to be fault-tolerant and less are utilization as it is implemented with the parity preserving reversible gates RUG and F2G. The simulation result of the suggested full adder is depicted in figure 27.

Insert Fig. 25

Insert Fig. 26

Insert Fig.27

5. Proposed fault tolerant reversible ALU

An arithmetic and logic unit is an essential part of several computing systems. With minimal hardware cost, the desired requirement of an ALU should execute the maximum allowable operations. The suggested fault tolerant reversible ALU unit has separated into two sub-components: (1) a reversible arithmetic unit (AU)(2) a logic unit(LU), which is shown in Figure 28. The signals used for this ALU are A, B & Cin(three inputs), constant inputs, and selection lines (S0, S1 & S2). A 2X1 MUX is used to choose an output from any of the two components.

Insert Fig. 28

5.1 Arithmetic Unit

The reversible fault tolerant arithmetic unit (RAU) using the suggested full adder is seen in Figure 29. It incorporates one gate of FG, Fredkin, RUG, and F2G. It performs eight arithmetic operations like transfer, increment, decrement, copy, addition without carrying input, addition with carrying input, and addition with complement as depicted in Table 1. The reversible arithmetic module has five inputs (A, B, Cin, S0 & S1), two actual outputs(sum & Cout), and six garbage outputs (G1, G2, G3, G4, G5 & G6). The expressions for the two outputs sum and Cout are given by the following equations 5 & 6. The synthesized QCA layout of the suggested reversible AU is depicted in Figure 30 .

$$Sum= A \square (B(S_1 \square S_0)+S_0B') \square C_{in} \quad (5)$$

$$C_{out}=A(B(S_1 \square S_0)+S_0B') + B(S_1 \square S_0)+S_0B')C_{in} + AC_{in} \quad (6)$$

Insert Table 1

Insert Fig. 29

Insert Fig. 30

5.2 Logic unit

The reversible fault-tolerant logic unit (RLU) is as seen in Figure 31. It incorporates one gate of F2G and two gates of UPPGG & Fredkin. It performs sixteen logical operations like copy A, AND operation with complement B, XOR operation, OR operation, constant, AND, copy B, AND operation with complement A, NOT, OR operation with complement A and XNOR operation as depicted in Table 2. The reversible logic module has two inputs (A, B), four selection inputs (Cin, S0, S1 & S2), one actual output(Y), and twelve garbage outputs. The expressions for the output Y is given by equation 7. The synthesized QCA layout of the suggested reversible LU is as depicted in Figure 32.

$$Y=S_2 \square S_1A \square S_0B \square C_{in}AB \quad (7)$$

Insert Table 2

Insert Fig. 31

Insert Fig. 32

6.Results and discussion

The characteristics used with QCA Designer-E to generate simulation results of the proposed circuit, along with energy dissipation, are listed. These are all the essential parameters for simulating any QCA circuit with the QCA Designer-E software. The dimension of a single QCA cell is 18 nm. The gaps between the cells from each QCA are 2 nm.The paper introduces a novel multilayer reversible QCA ALU layout which performs both the arithmetic and logical execution operations. Furthermore, a new QCA fault tolerant reversible 2:1 multiplexer is to select the arithmetic and logic unit. The proposed reversible 2:1 multiplexer built with 75 QCA cells, 0.08 μm^2 region, and four clock cycle latency that are lower compared to the best earlier design. Also, an efficient fault-tolerant reversible full adder has suggested minimizing the complexity of the arithmetic unit. Table 3 shows the results of suggested FA has 107 QCA cells and an area of 0.08 μm^2 that are less than the best existing single-layer design.

Insert Table 3

The factors measured for comparing ALU with existing are the number of operations, constant inputs, garbage outputs, number of reversible gates, and the total number of logical calculations.Table 4 discusses the comparison of the suggested ALU with the best earlier works. We may note from Table 5 that our fault-tolerant reversible ALU requires only five constant inputs, ten reversible gates, and eighteen garbage outputs, which are lower than the current works. Also, the suggested ALU performs eight arithmetic and sixteen logical operations. Therefore, regarding two very different parameters area and speed, our proposed structure is more appropriate for implementing the reversible QCA design.

Insert Table 4

Table 5 provides the improvement of the suggested ALU with the previous best works. It shows an improvement of 25% in terms of the number of operations, 29% constant inputs, 18% garbage outputs, and 9 % the number of gates used when compared to the KMD approach 2. The improvement of the proposed ALU with the earlier works is represented in graphical form as seen in Figure 33. The comparison of the performance of n-bit ALU is as seen in table 6.

Insert Table 5

Insert Table 6

Insert Fig. 33

7.Conclusion

This paper introduces a novel multilayer fault-tolerant reversible arithmetic logic unit using QCA technology. The ALU unit has been separated into a reversible arithmetic and logic unit. Moreover, an area-efficient reversible 2:1 multiplexer has proposed to select either the arithmetic or logical operations. The results of the simulation show the suggested 2:1 multiplexer has built-in comparison to the best previous model, with 75 cells, 0.08 μm2 area, four

clock cycle latency, and fault tolerance. Furthermore, an efficient fault-tolerant reversible QCA full adder with parity preserving gates has been proposed to decrease the complexity of the arithmetic operations. The suggested ALU architecture is fault-tolerant as the circuit itself has been designed using parity preserving gates.The results of the comparison demonstrate that the suggested full adder has 107 cells, and 0.08 μm2 area is much less than the best earlier models. The proposed QCA ALU shows an improvement of about 25% in the number of operations, 29% in constant inputs, 18 % in garbage outputs, and 9 % in the number of gates utilized compared to the earlier best design.

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conflicts of interest: The authors have no conflicts of interest to declare that are relevant to the content of this article.

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Figures

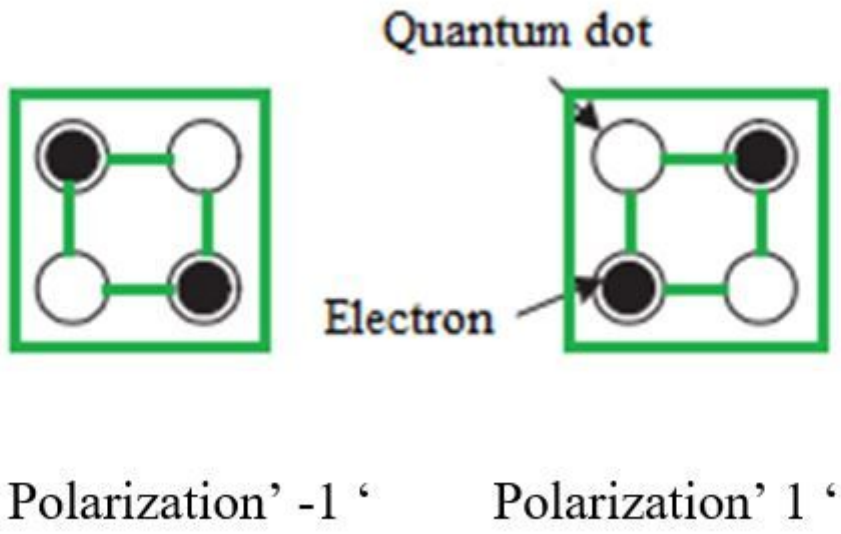

Figure 1

Basic QCA cell

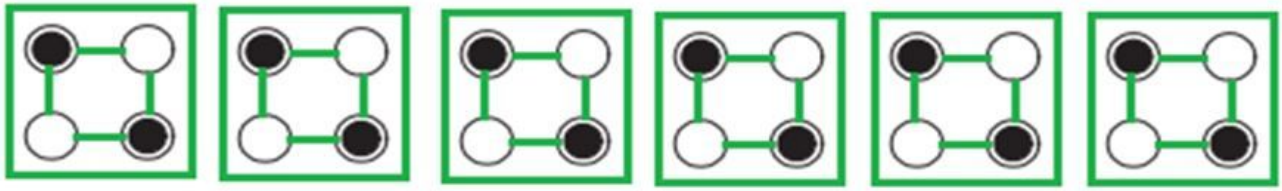

Figure 2

A basic QCA wire

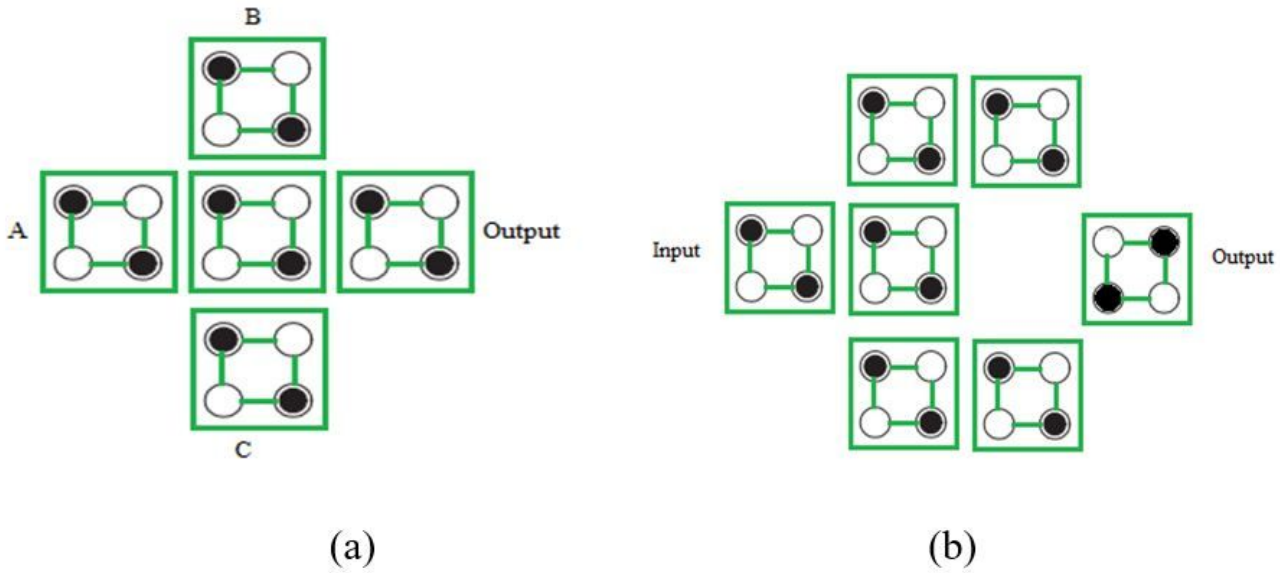

Figure 3

(a) A majority gate (b) An inverter

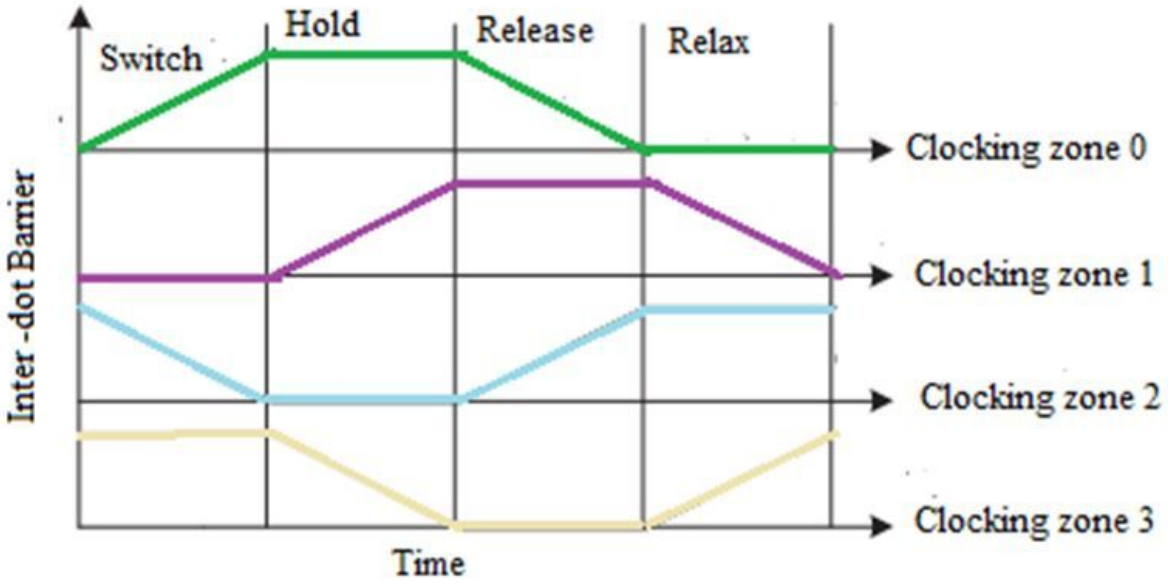

Figure 4

Clocking scheme of QCA

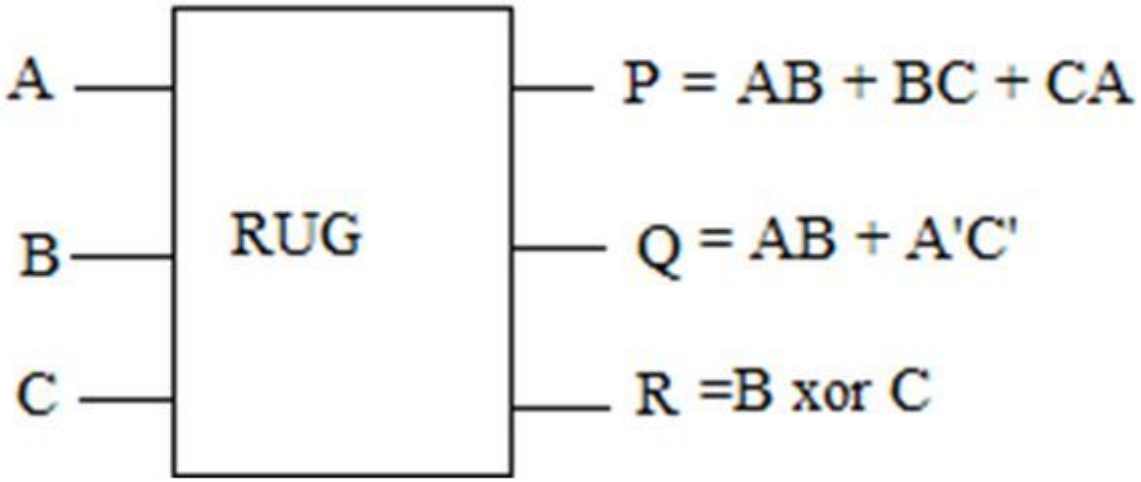

Figure 5

Structure of RUG

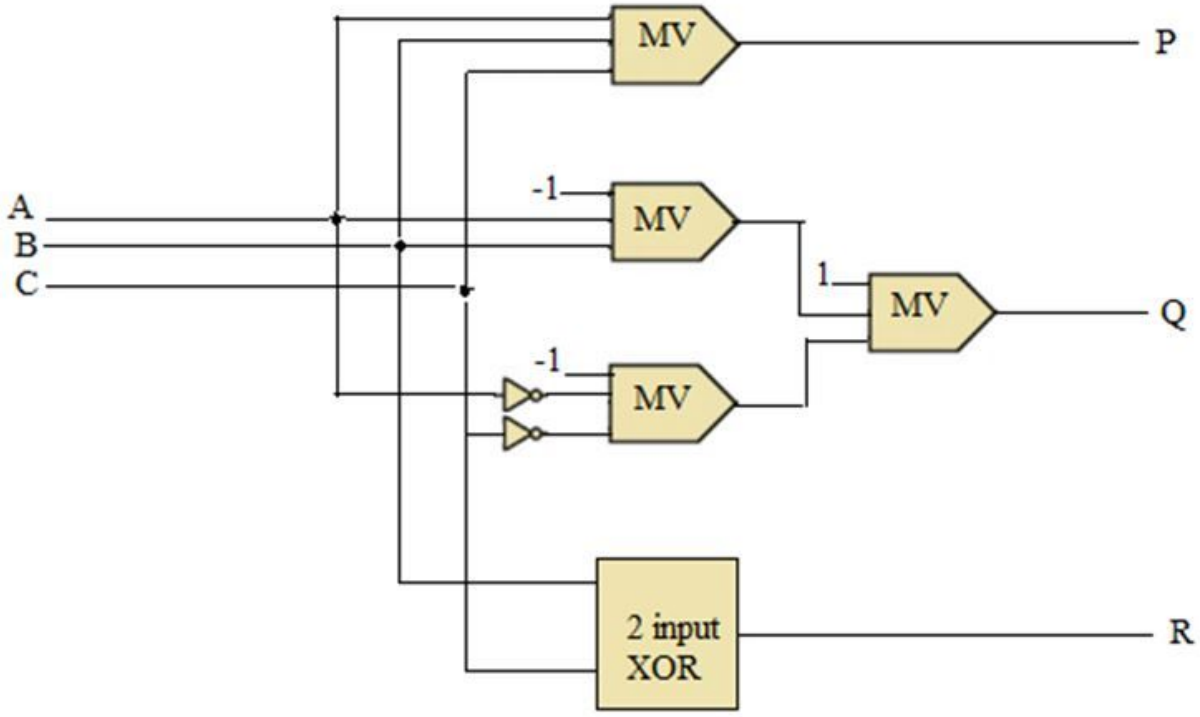

Figure 6

Schematic of RUG

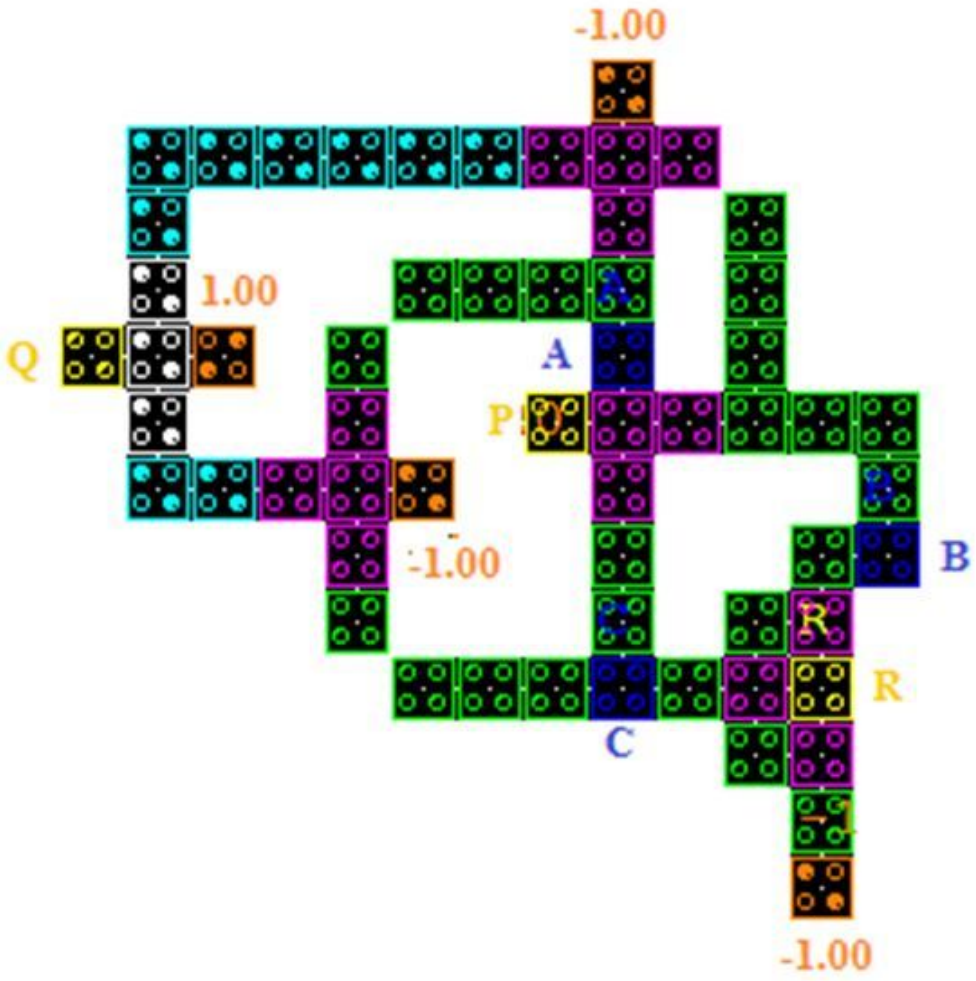

Figure 7

QCA layout of RUG

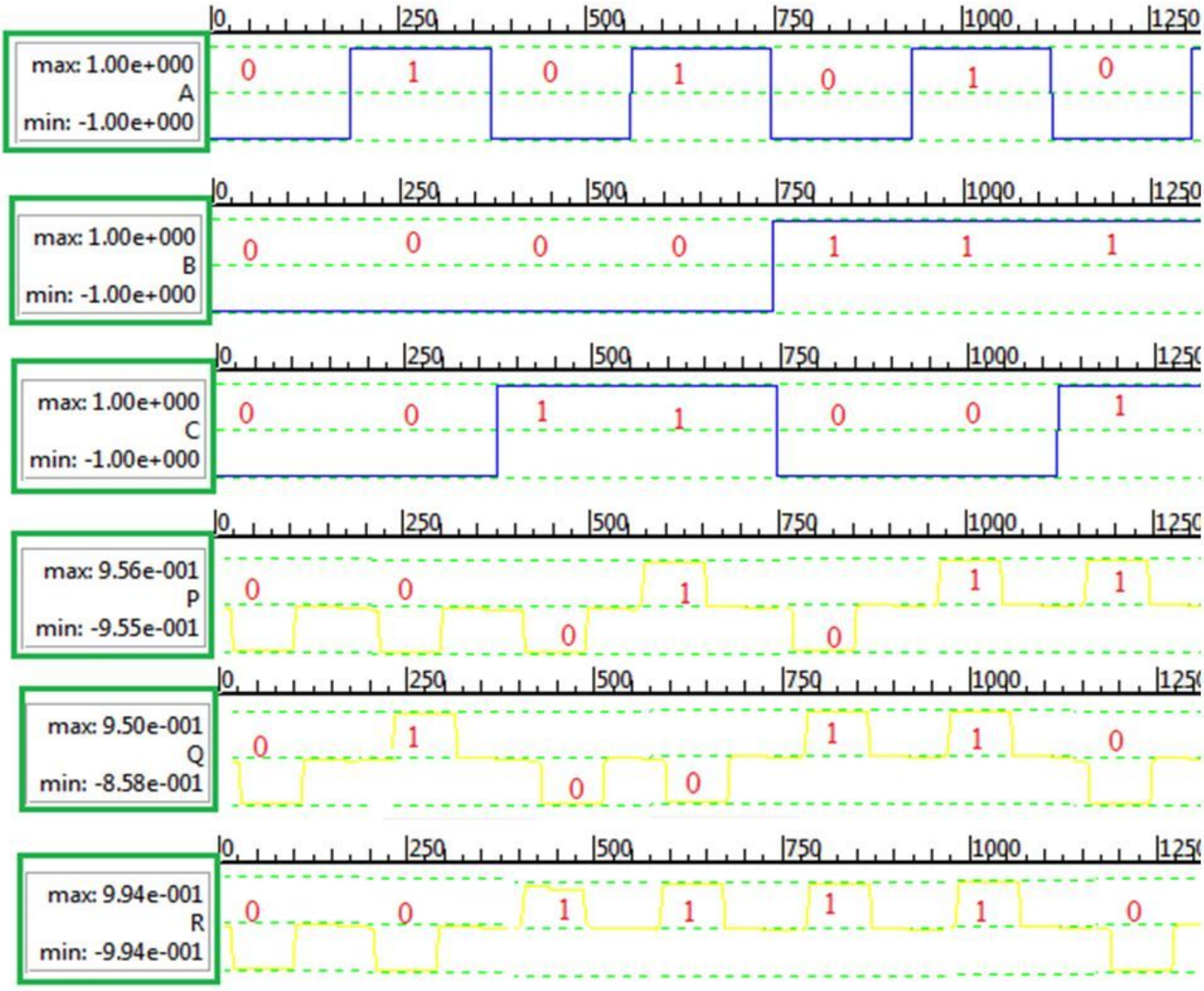

Figure 8

Simulation result of RUG

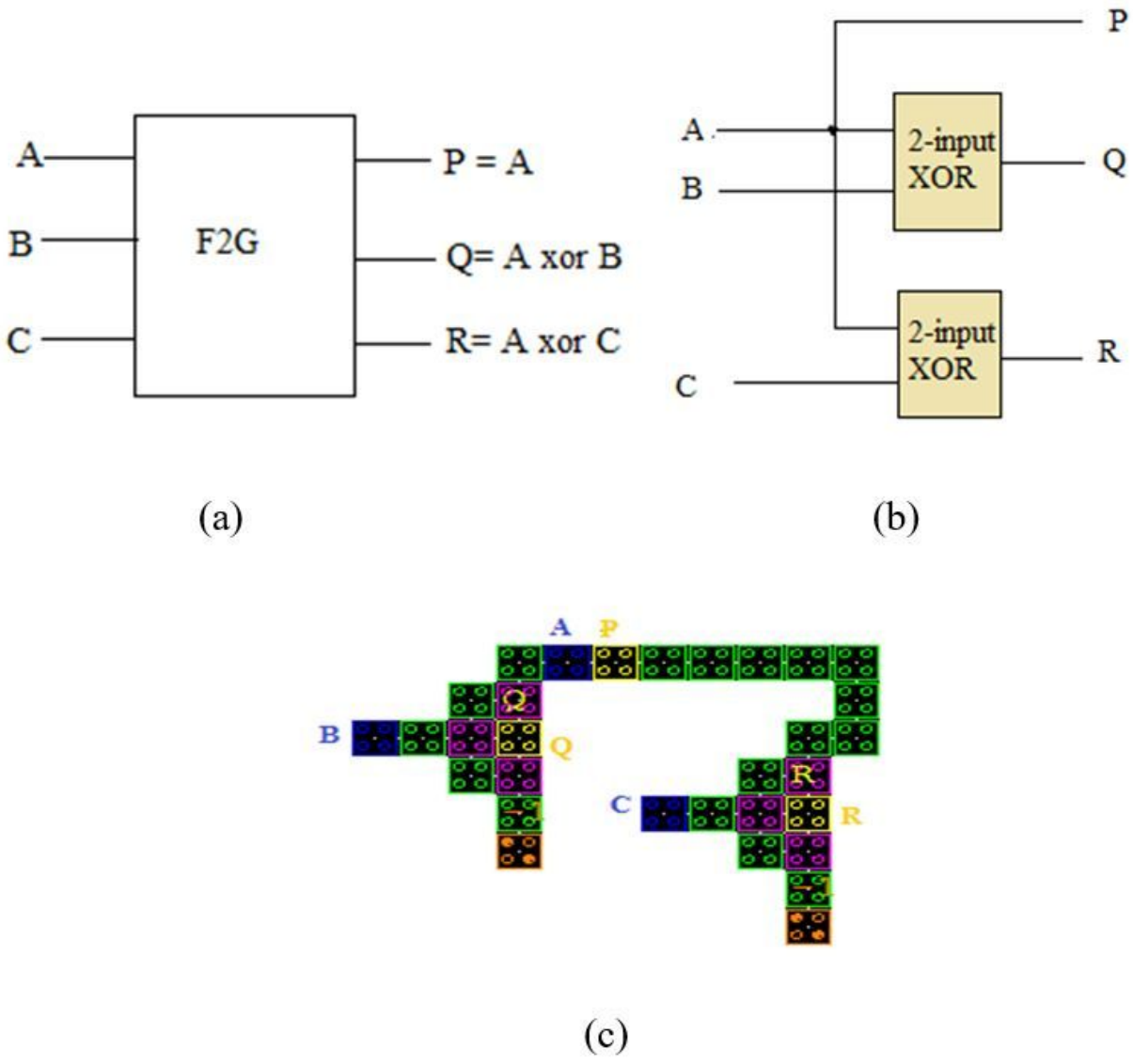

Figure 9

(a) Sturcture of F2G (b) Schematic of F2G (c) QCA layout of F2G

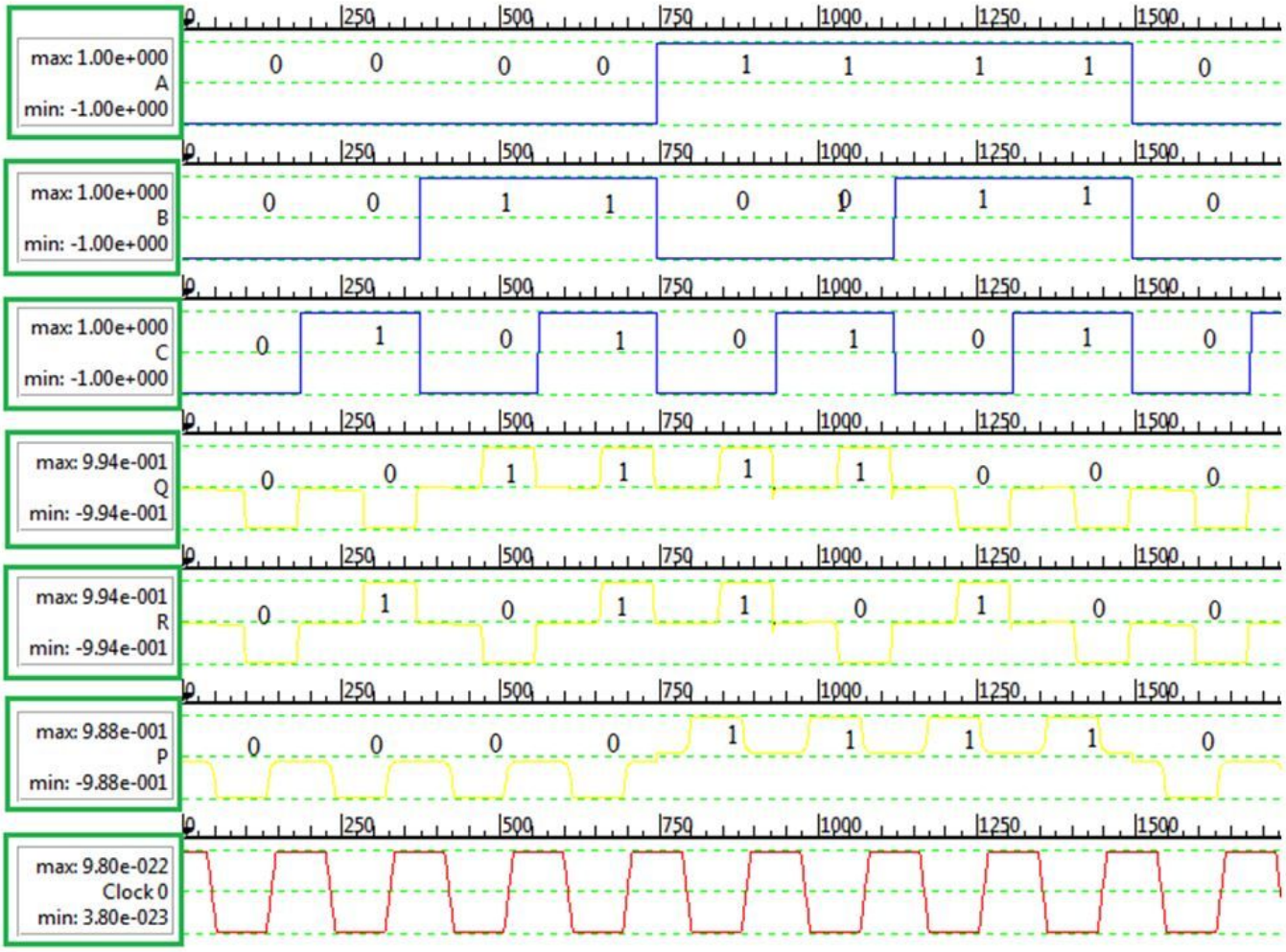

Figure 10

Simulation output of F2G

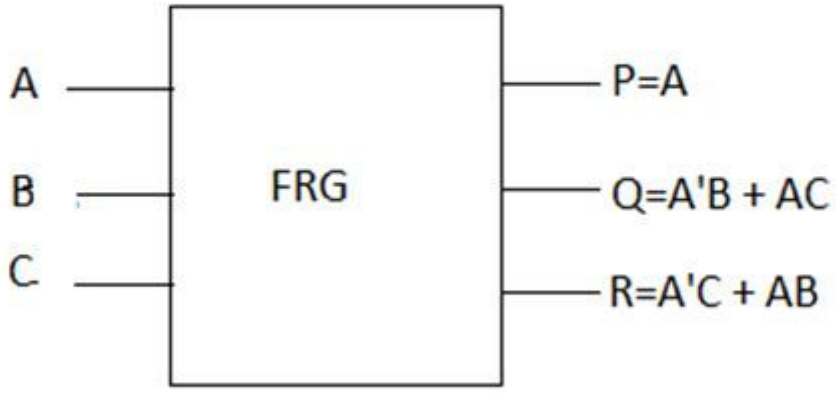

Figure 11

FRG gate block diagram

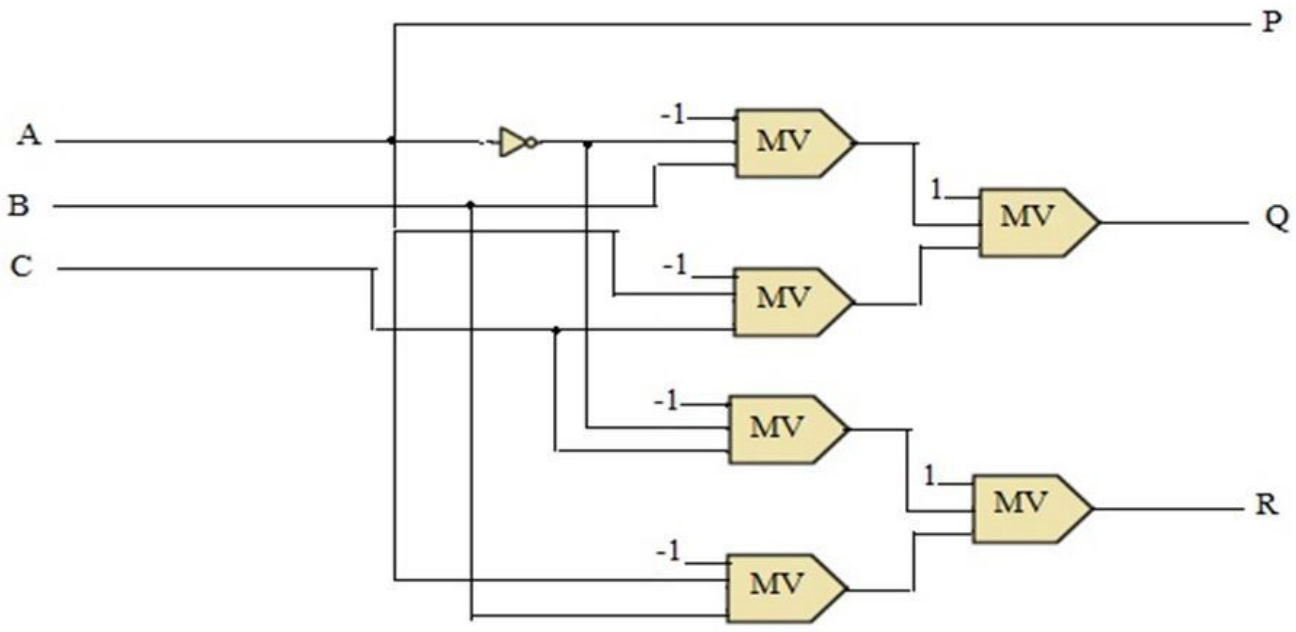

Figure 12

Schematic of FRG

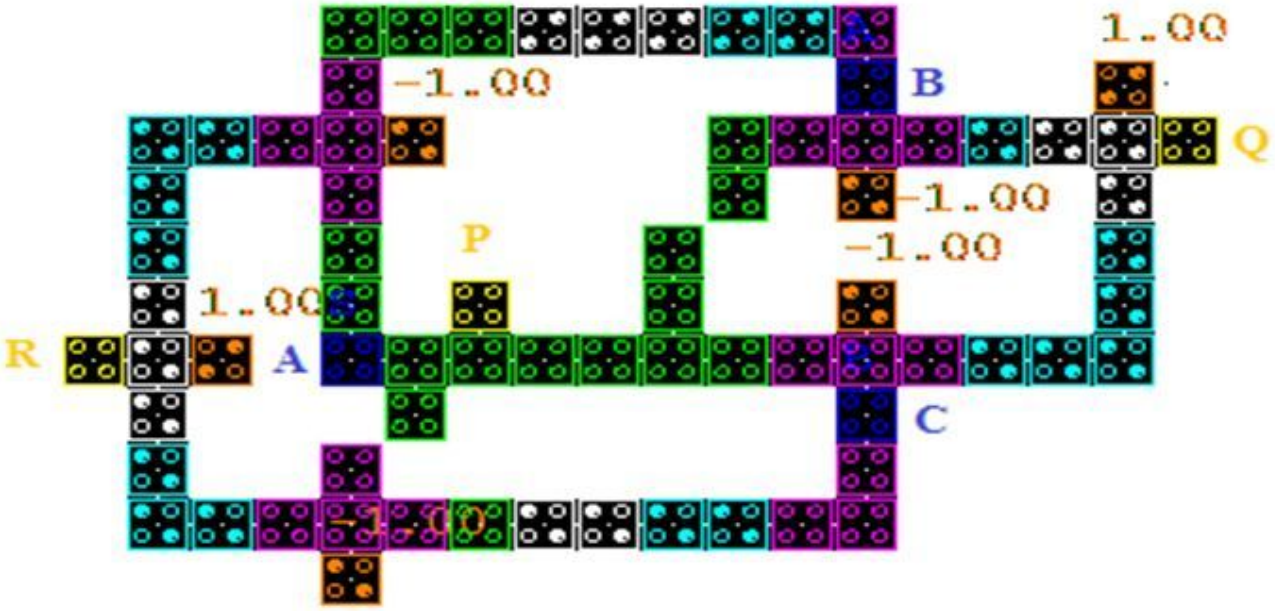

Figure 13

QCA layout of FRG

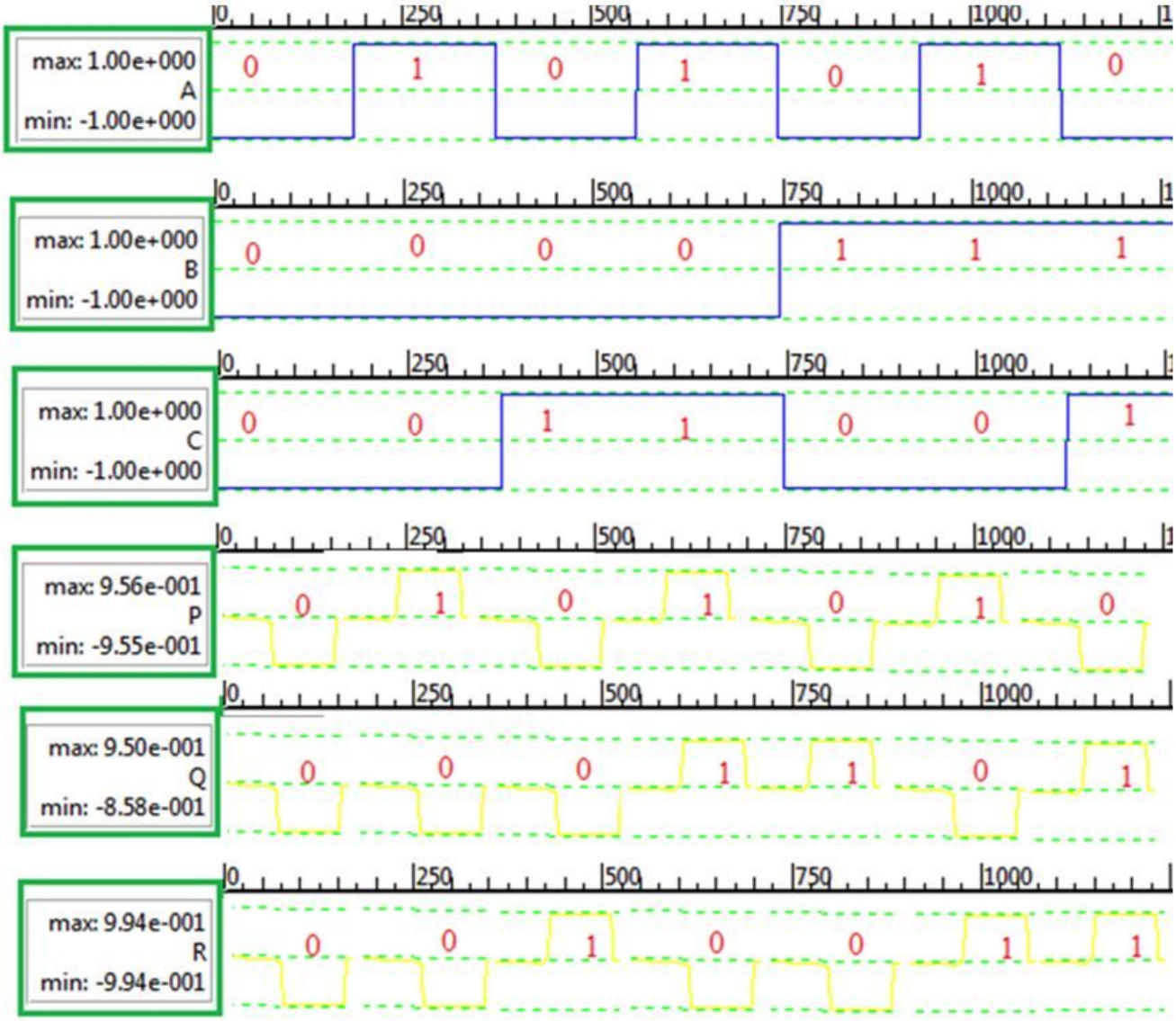

Figure 14

Simulation result of FRG

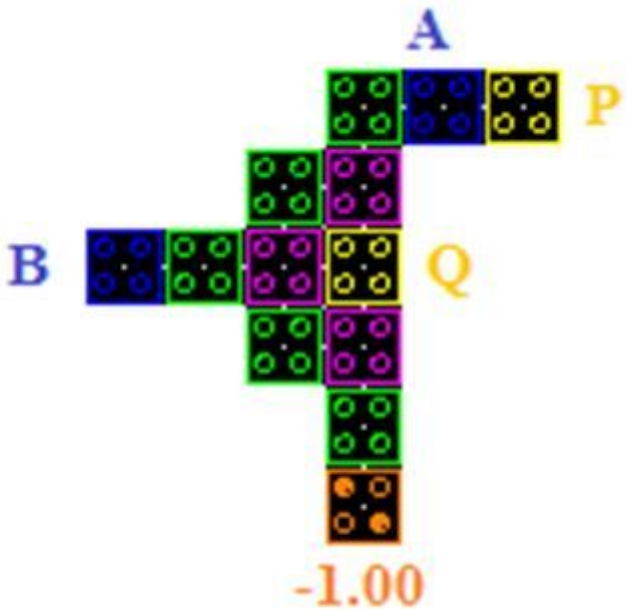

Figure 15

FG gate block diagram

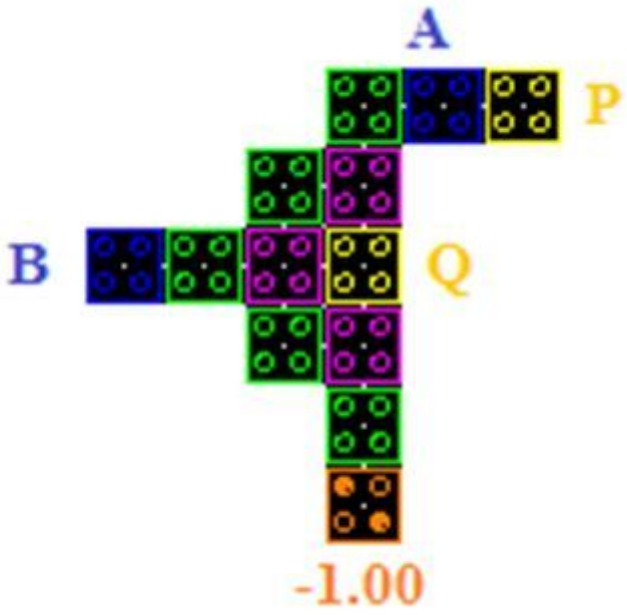

Figure 16

QCA layout of FG

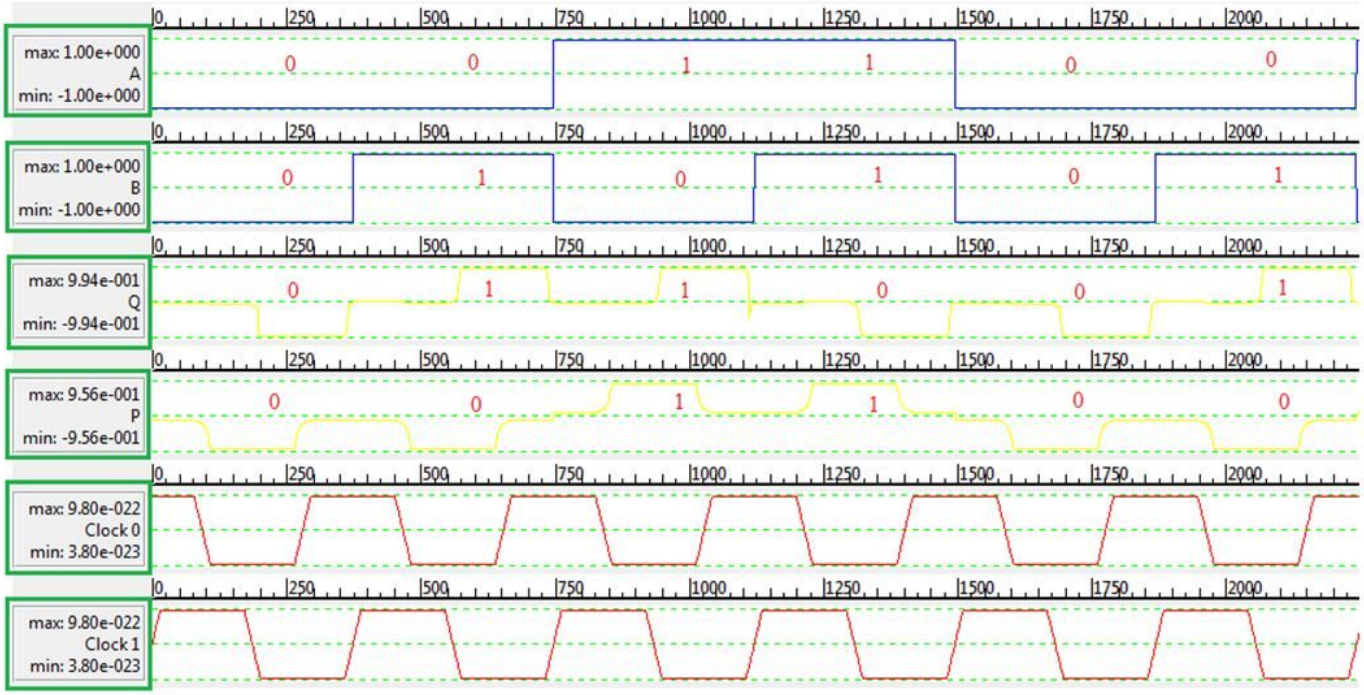

Figure 17

Simulation result of FG

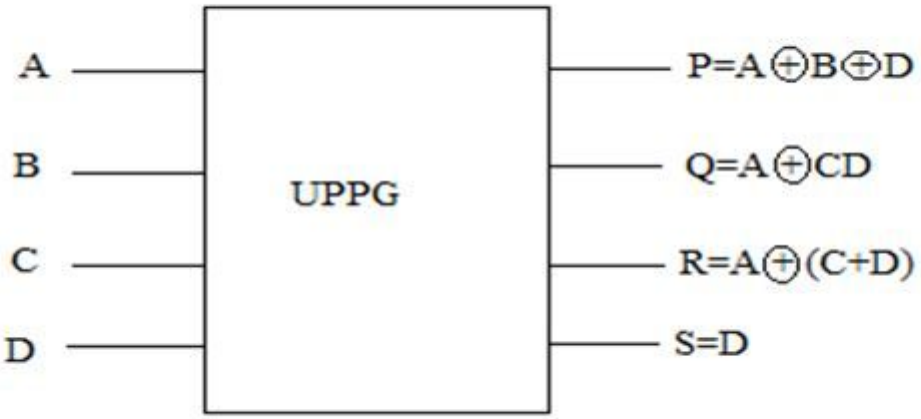

Figure 18

UPPG block diagram

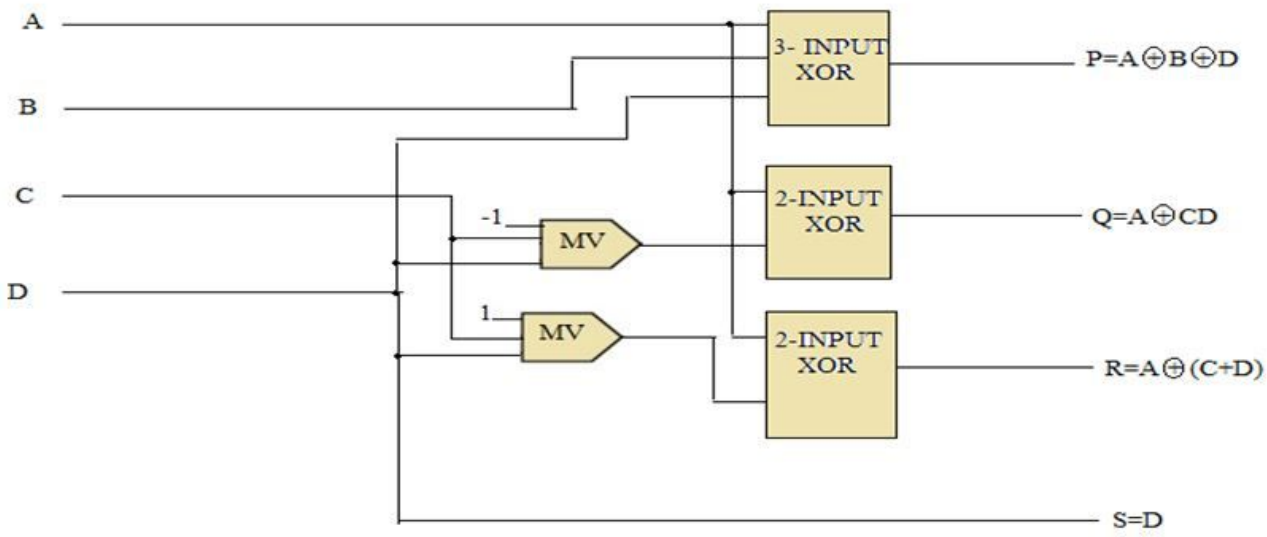

Figure 19

Schematic of UPPG

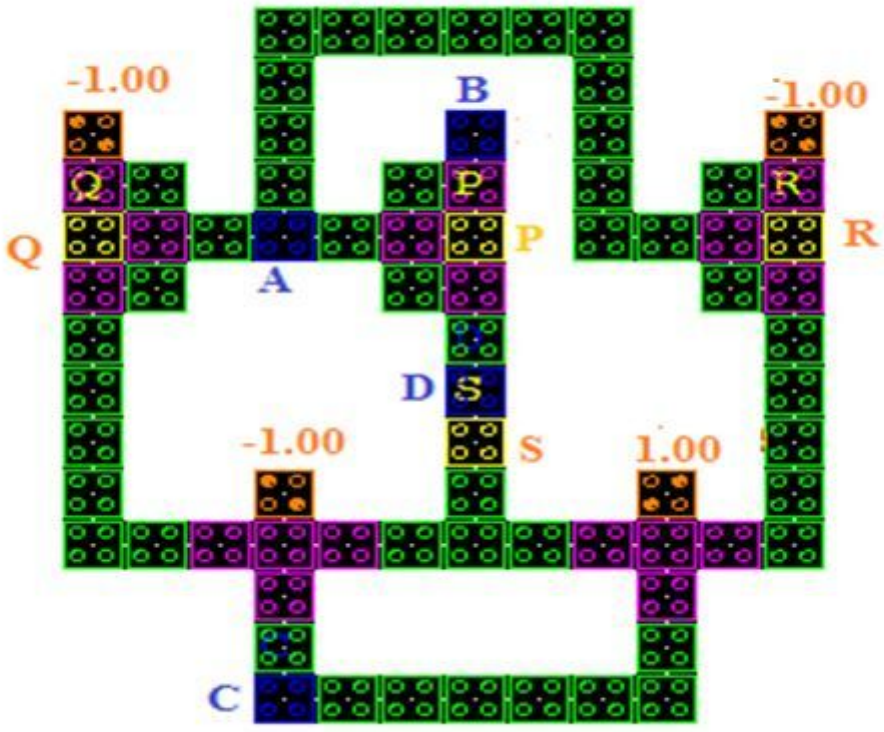

Figure 20

QCA layout of UPPG

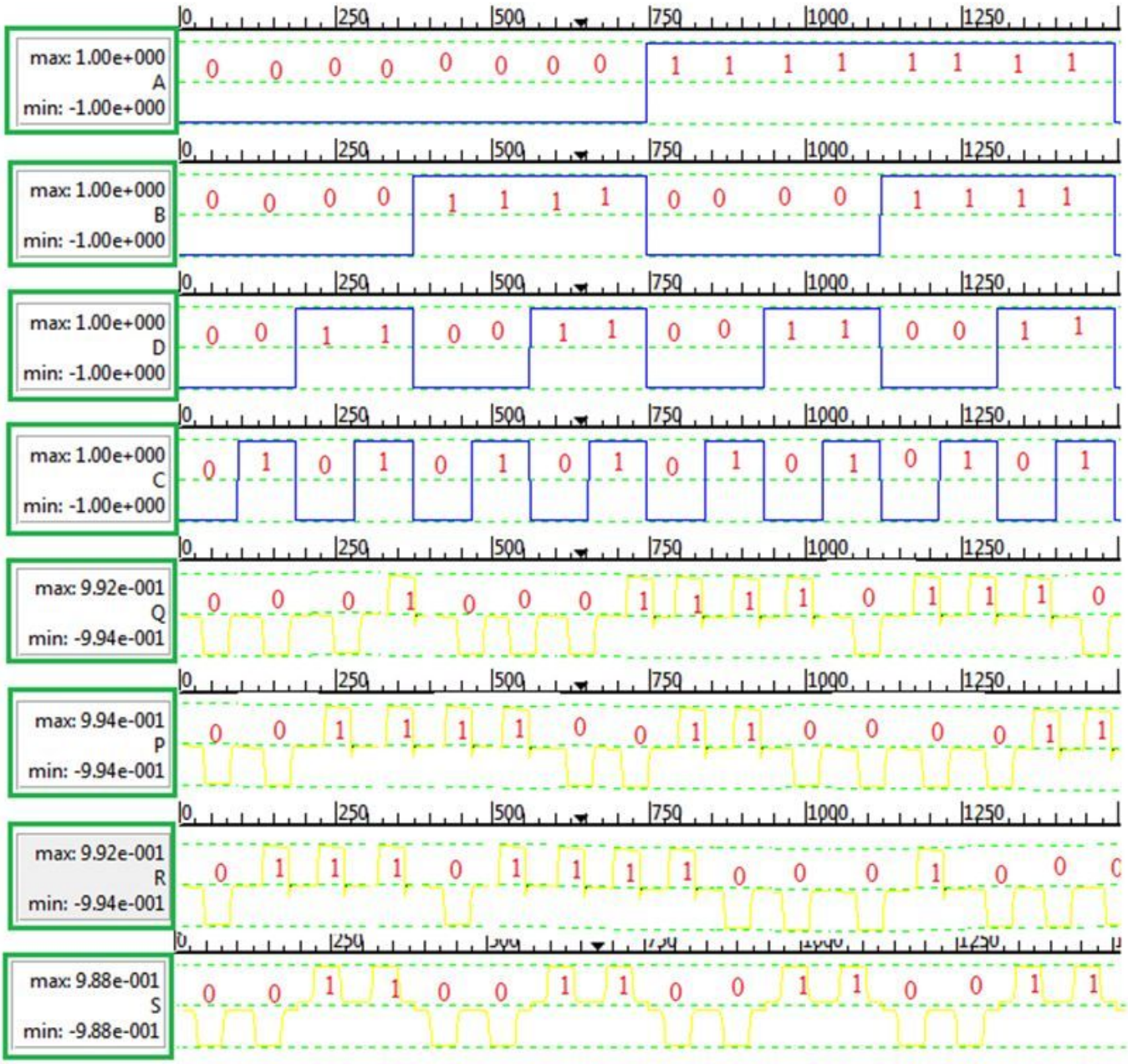

Figure 21

Simulation of UPPG

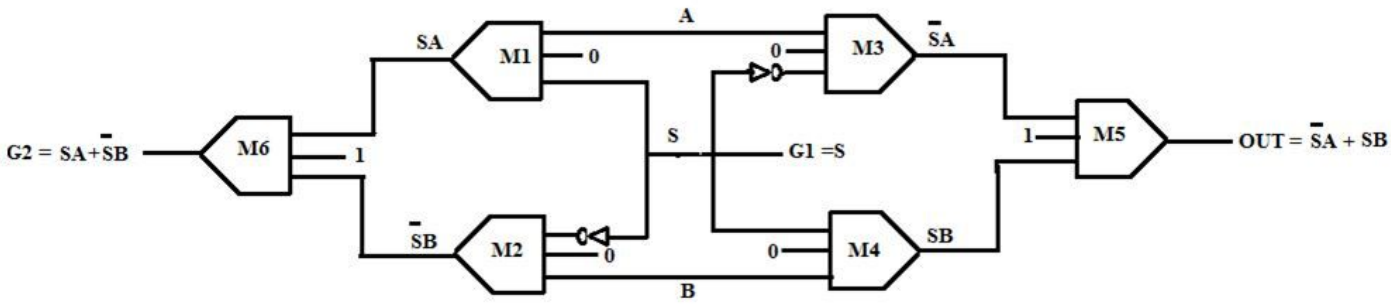

Figure 22

Schematic of 2:1 MUX

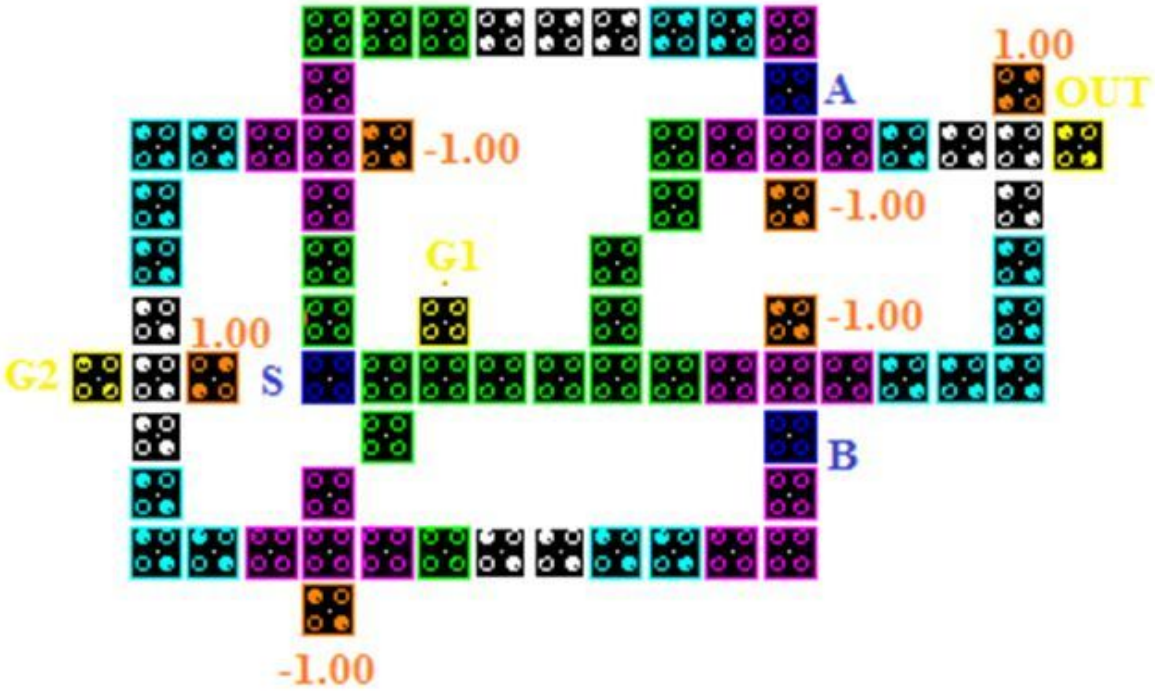

Figure 23

QCA layout of 2:1 MUX

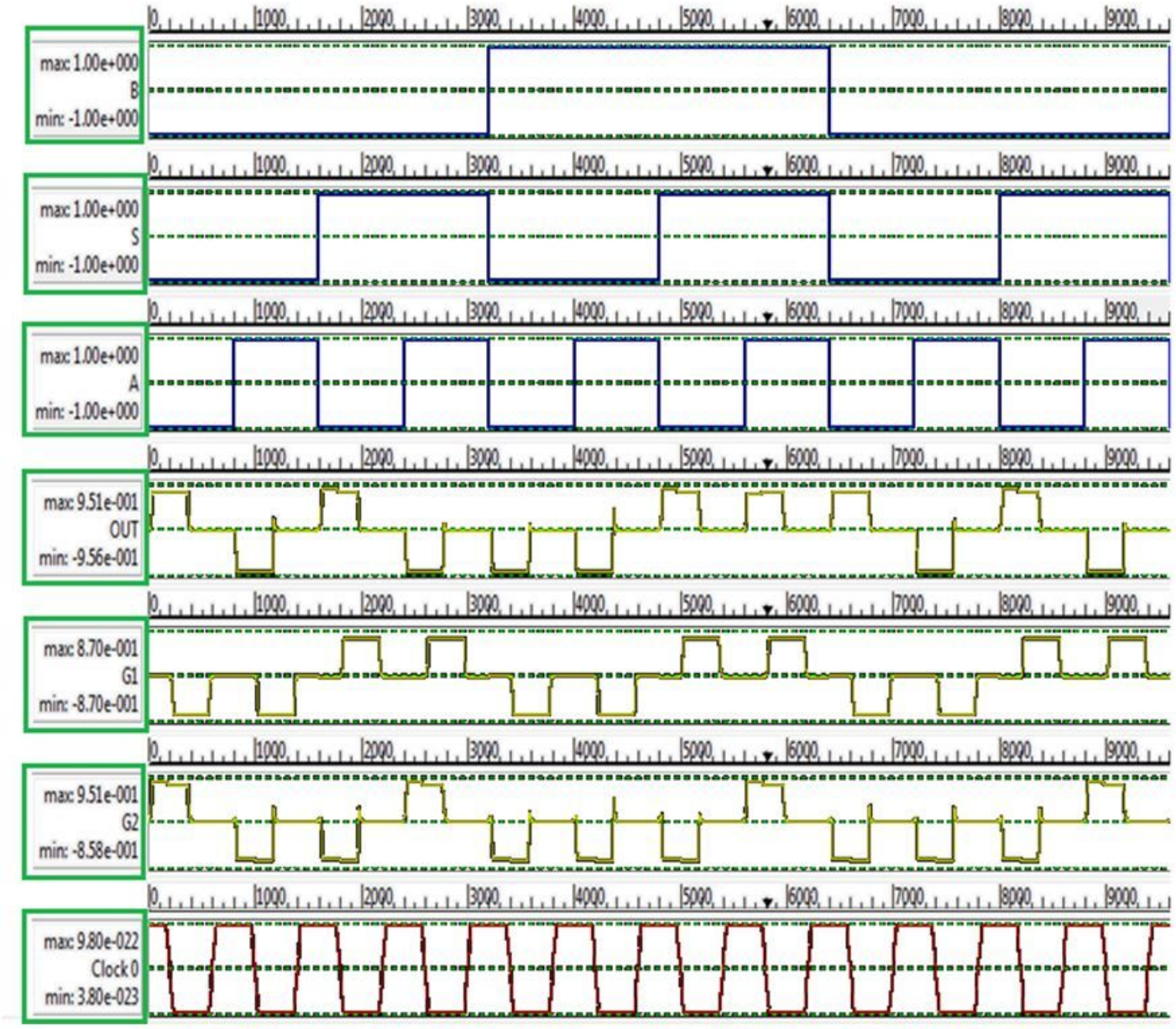

Figure 24

Simulation of 2:1 MUX

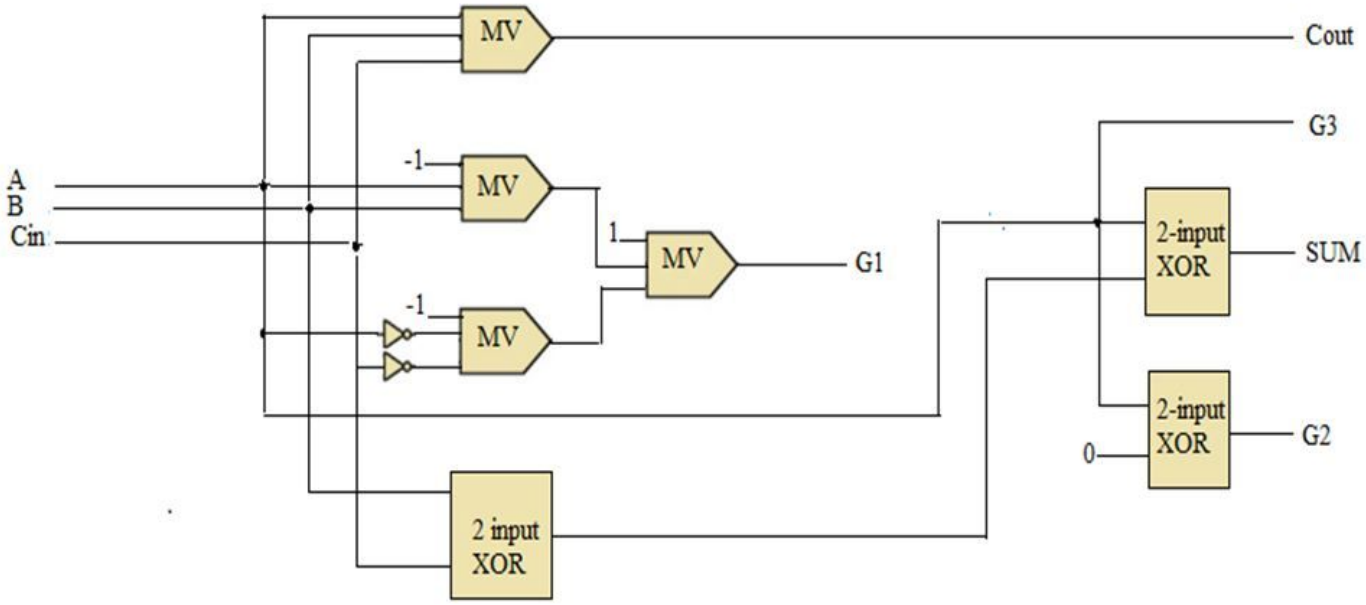

Figure 25

Schematic of proposed full adder

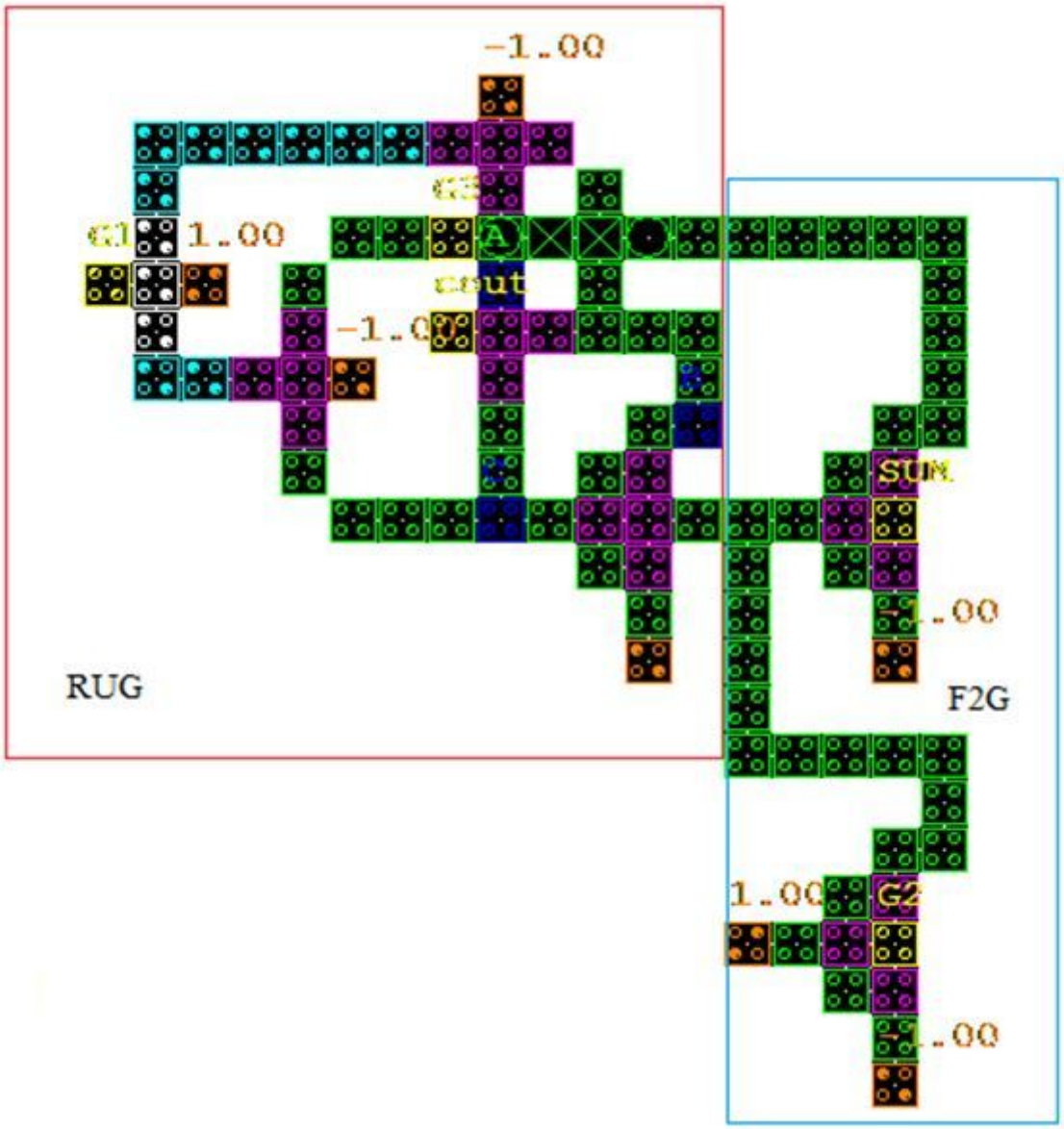

Figure 26

QCA layout of proposed full adder

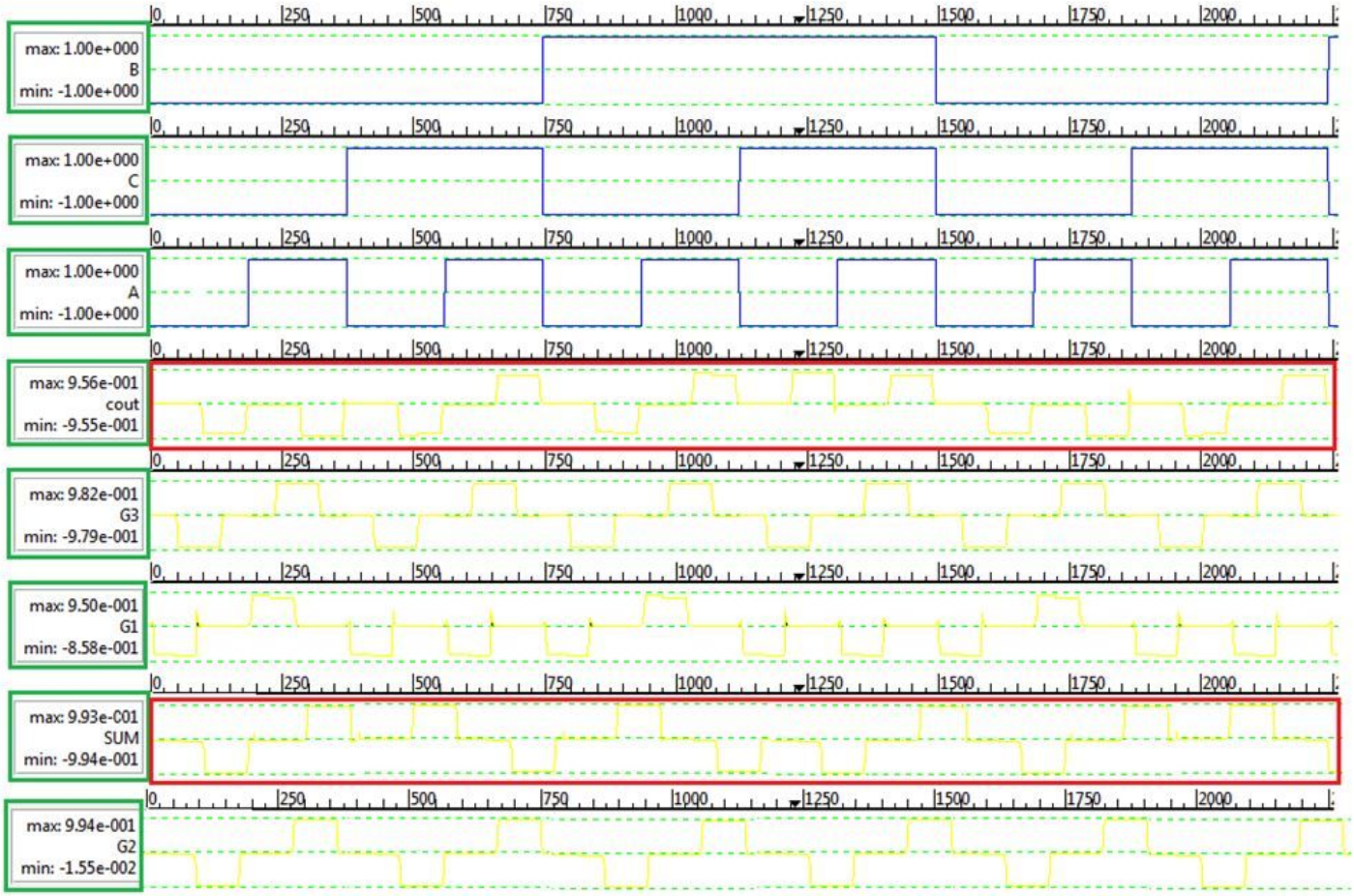

Figure 27

Simulation of the proposed reversible fault-tolerant full adder

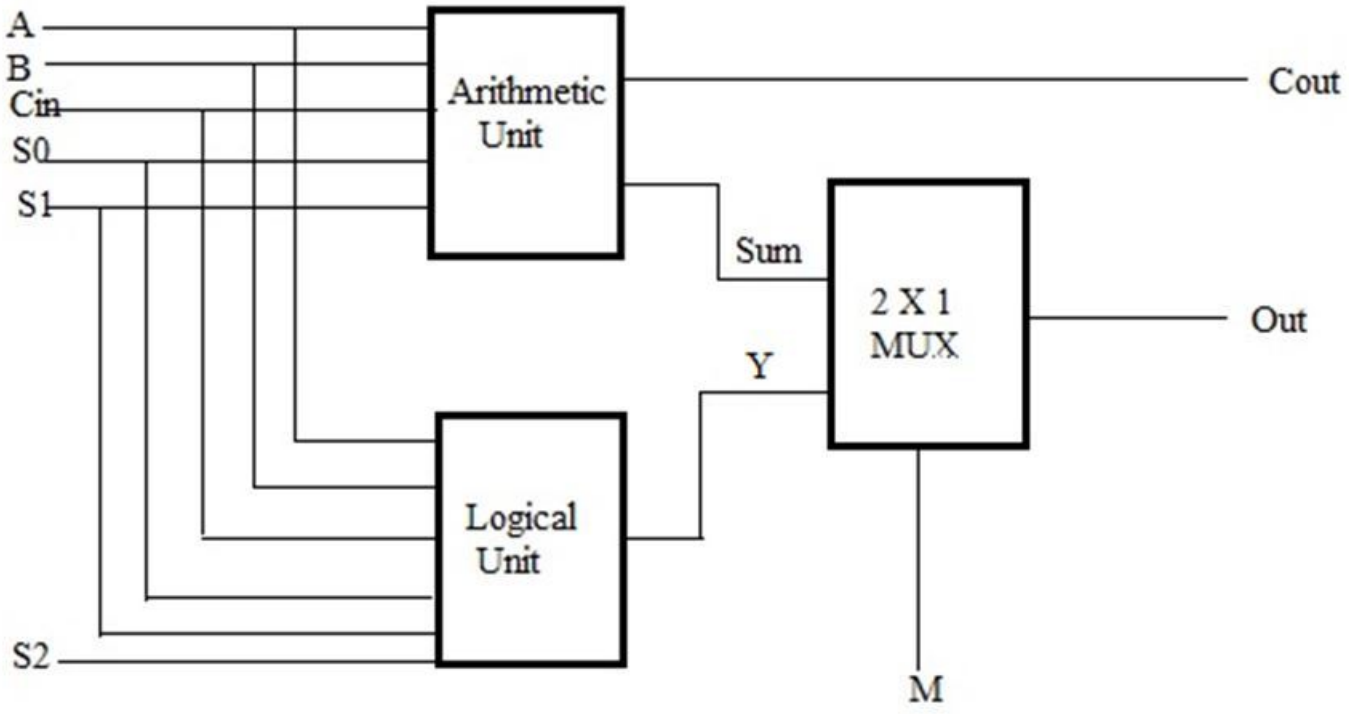

Figure 28

Proposed ALU block diagram

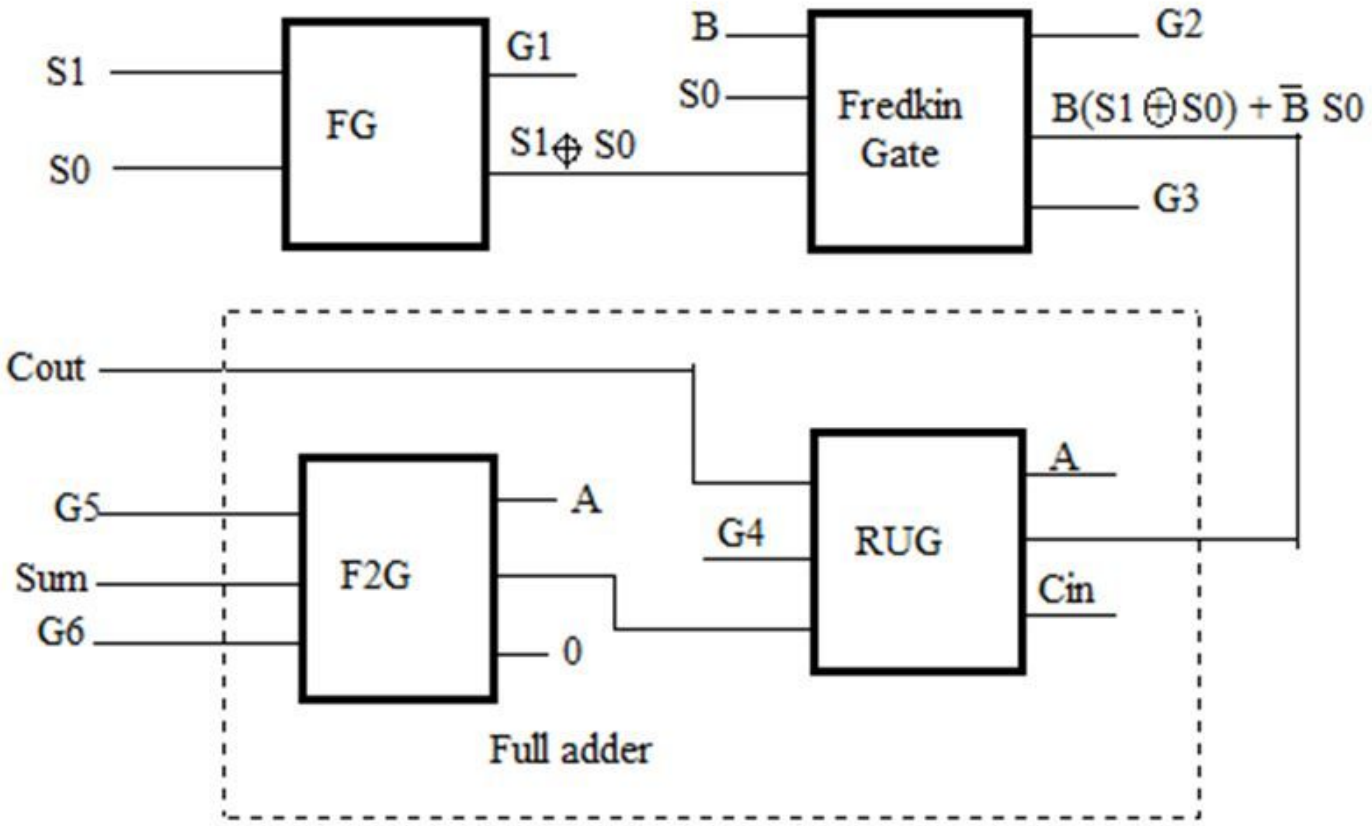

Figure 29

Proposed Arithmetic unit block diagram

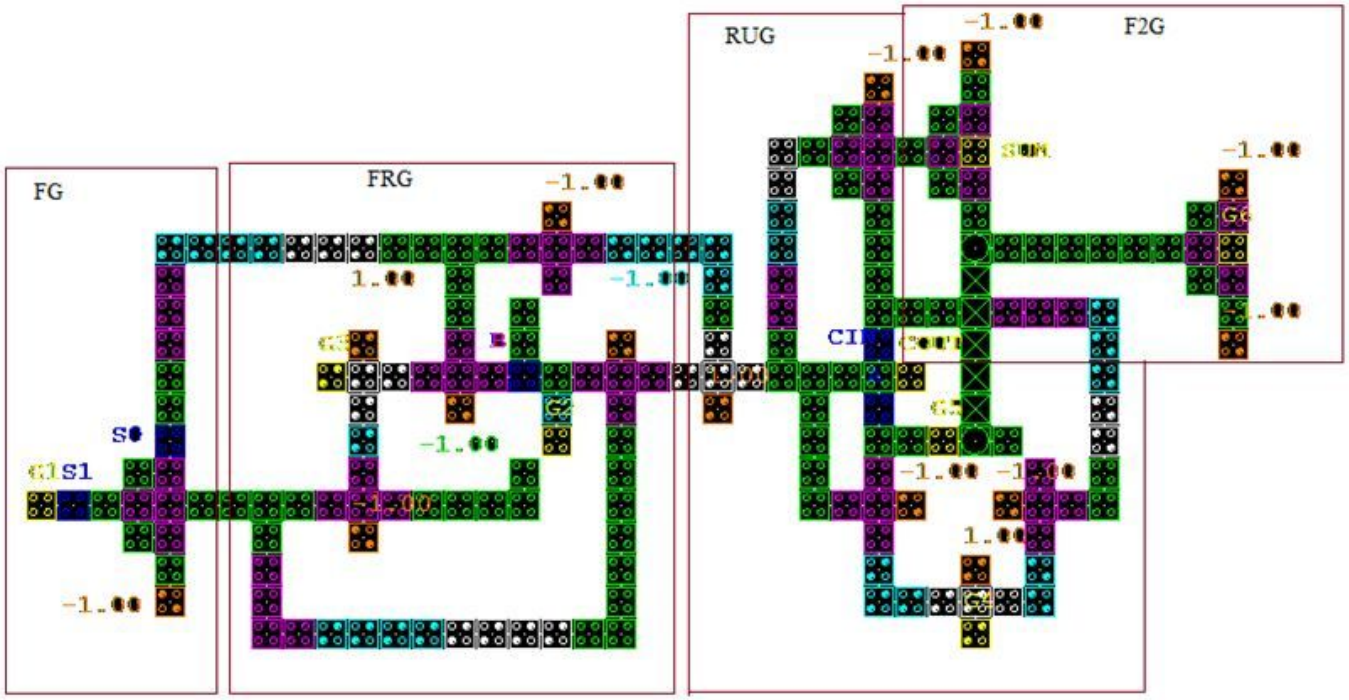

Figure 30

QCA layout of the porposed AU

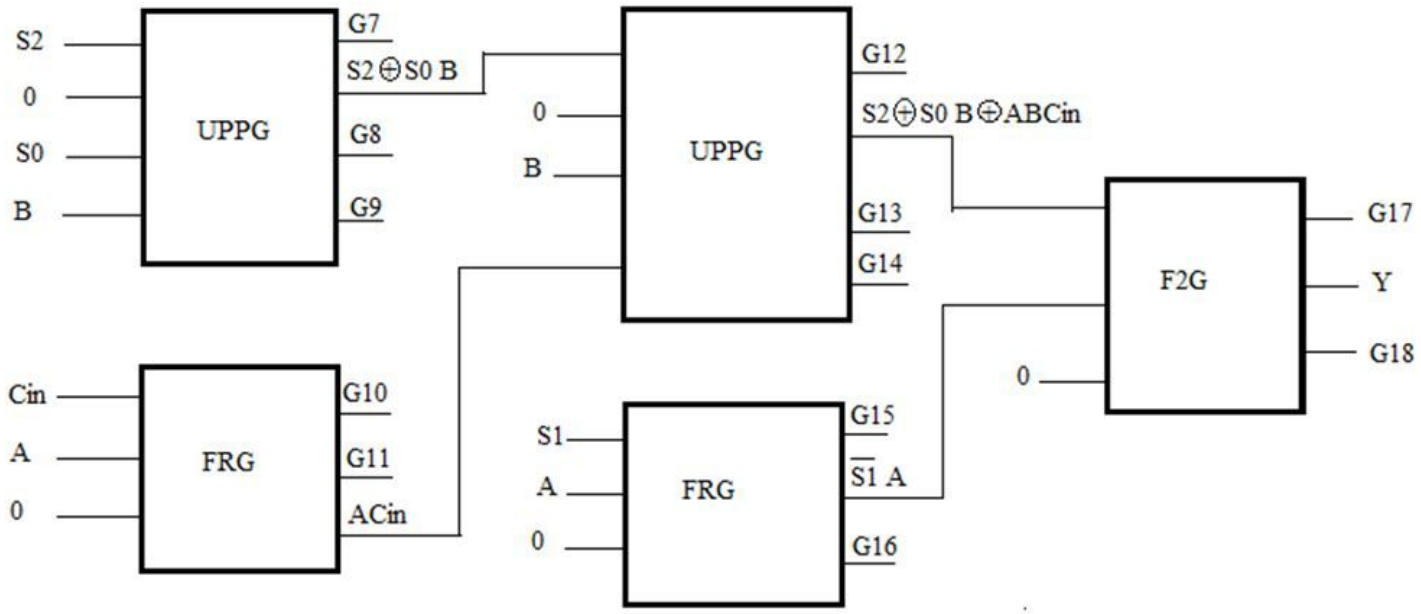

Figure 31

Proposed LU block diagram

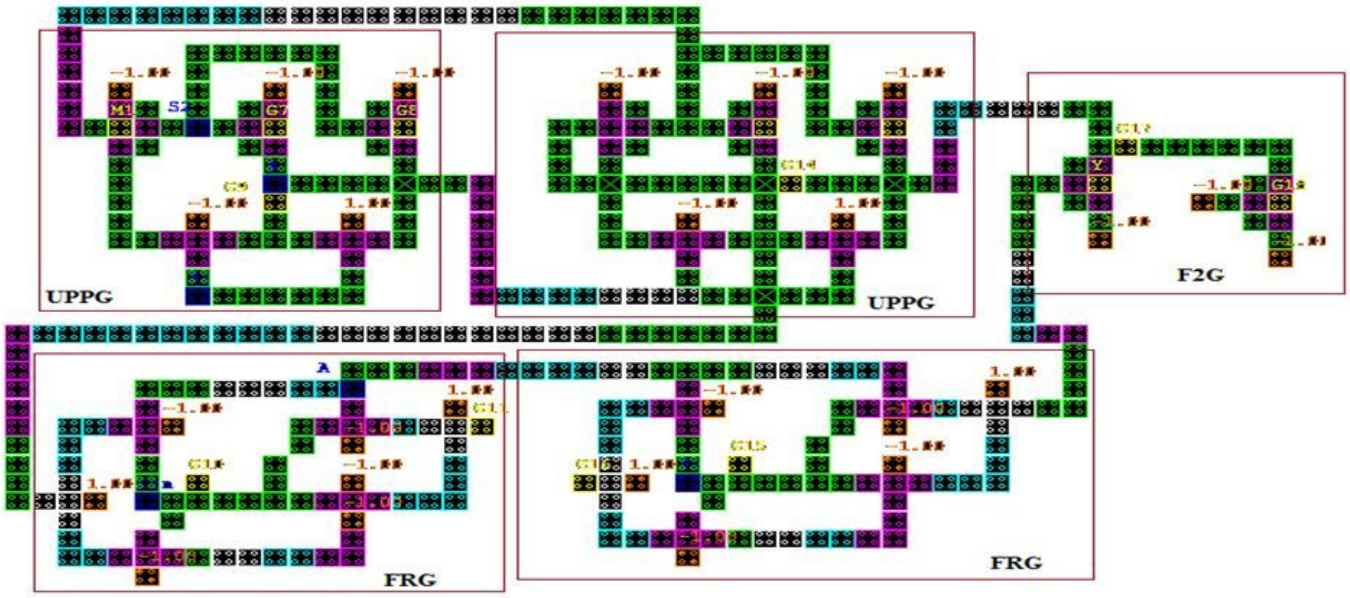

Figure 32

QCA layout of proposed LU