Performance analysis of Tunnel FET based Ring Oscillator using Sentaurus TCAD

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Menka Yadav,

Abstract—A detailed Sentaurus TCAD simulation based study for Silicon Double Gate Tunnel Field Effect Transistor (Si-DG TFET) based Ring Oscillator (RO) is presented in this work. Two different ring oscillator topologies (simple RO and Negative Skewed Delay RO) are presented with two different structures for TFET device. The two structures are different in the source-drain extension regions widths. The extension region width variation effects are studied and presented for inverter and ring oscillator. A TFET based inverter is presented to show the changes in behavior due to variations in the drain extension region widths, which is later used for RO designs. The drain extension region width changes the drain extension region resistances which in turn is responsible for change in the corresponding device properties. RO simulation are used for calculating the delay. To further explore digital and analog applications transfer characteristics and noise margins of inverter are explored with power supplies variations. Better reliability for oscillation frequency is obtained using Negative Skewed Delay ring oscillator (NSD RO) topology. NSD RO is resulting in lesser jitter, more reliable frequency as compared to single-ended ring oscillator topology. By tuning the supply voltage of the device the ring oscillator frequency can be used for RF applications, thus it works like a voltage controlled oscillator (VCO).

Index Terms—Sentaurus TCAD, double gate, tunnel FET, inverter, peak overshoot, ring oscillator, Silicon TFET, NSD RO

I. INTRODUCTION

The conventional device metal-oxide-semiconductor field-effect transistors (MOSFET) is now saturated before further scaling due to its short channel effects, high leakage current etc. Among new devices- tunnel field-effect transistors (TFETs) are promising future benchmark to replace the CMOS [1] due to their potential for very low off current as compared to MOSFET [2], sub-60mV/dec sub-threshold swing [3]–[5] and higher reliability with respect to temperature changes [6], [7], while for MOSFET sub-threshold swing at room temperature is 60mV/dec and it increases with temperature. The reduced swing is an essential requirement for the ultra-low power operation for the next generation of transistors. Researchers are finding Tunnel FET suitable for ultra-low power and energy

harvesting applications [8]–[10] in various domains. The TFET is the most future bench-marking device because of its strong similarity with the MOSFET configuration, which allows significant re-use of the MOSFET expertise and reliable operation at higher temperatures. Although ON current (I_{ON}) for Silicon TFETs is lower as compared to III-V materials and Ge TFET [11]–[13], but still since Silicon is cheaper material, easily available, and fabrication setup already available for Silicon-MOSFET can be reused for TFET rather than designing a new fabrication setup and paying new efforts for different steps in the device formation. This all makes the Silicon TFET research an important topic. Therefore in this paper, **Silicon** is used as the device material. There are different ways to boost up the ON current (I_{ON}) for Silicon TFETs, here high- κ gate dielectric (HfO_2) is used to increase the TFET ON current (I_{ON}) [14] and [15], which can easily be integrated with Silicon interface. The below-mentioned structures are taken for study in this paper **Fig. 1**.

Fig. 1. Different Tunnel FET structures under study with gate length 50nm and channel thickness 10nm.

The device under study is shown in **Fig.1** with channel width-50 nm, source/drain extension length 100 nm, high- κ thickness 3 nm. In this work an inverter is prepared to see the effects of source/drain extension width changes and then it is used for ring oscillator design.

With device miniaturization, there is a huge demand to develop an oscillator which can be fabricated with the chip with low cost and better reliability. Earlier days quartz crystal oscillator and L-C tank oscillators were used which are proving very heavy oscillators now a days. So, research

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is going on towards a low cost solution for frequency generator on the chip and one of such solution is RO, which can be fully fabricated along the chip and the output frequency can be tuned with variations in the supply voltage, thus it works like voltage control oscillator (VCO). There are different topologies used for ring oscillator to make it more reliable and low power consuming oscillator.

Ring oscillators have a wide variety of applications in transmitter and receiver systems of communication, control and feedback systems, as VCO in Phase Locked Loops, and others. Since the TFET ring oscillators are expected to perform reliably even at higher temperatures (virtue of TFETs) [7], so when the device sizes are shrinking and power density is increasing the RO with TFET can give more reliable results as compared to the CMOS technology. Thus in this work, focus is on RO design and analysis with different parameters of the device or the supply voltage, like- the effect of drain extension region widths of Tunnel FET has been studied for the inverter DC, Voltage Transfer Characteristics (VTC), and transient characteristics, and for ring oscillator application as well. The supply voltage variations and its effects on the characteristics of inverter and ring oscillator have also been explored in this work. A NSD-RO is presented to make the ring oscillator frequency more stable, and with less jitter as compared with single-ended ring oscillator topology.

The work done in this paper is as follows: Simulation setup and TFET device calibration are presented in Sec. II, Inverter Analysis in detail is presented in Sec. III, Ring Oscillator is presented in Sec. IV and the last section concludes the work done.

II. SIMULATION SETUP AND TFET DEVICE CALIBRATION

In the whole work, the simulations are performed using TCAD **sdevice** Sentaurus simulator [16]. The models included are - non local tunneling model, Wentzel-Kramers-Brillouin (WKB) is used with Fermi statistics, band-gap narrowing model, *OldSlotboom*, is included without Fermi statistics, high field saturation mobility models, carrier transport model, Shockley Reed Hall (SRH), and Auger carrier recombination, eMLDA, and hMLDA models are included for density correction due to energy quantization. The doping profiles used in the device are abrupt to make more carriers to tunnel during device ON condition. For n-type impurity, phosphorus as a pentavalent impurities is used. The device under study is calibrated against data given in [17], which was already calibrated against experimental data. For calibration, the electron, and hole effective masses have been tuned to match the tunneling current while for recombination current calibration, the carrier life times have

Fig. 2. $I_{ds} - V_{gs}$ Calibration with the previously reported work in [17] (which is already calibrated against the experimental data presented Bhuwalka et al.), for this calibration all physical dimensions are used from [17], DG Tunnel FET with high-k gate oxide with EOT=0.9nm, channel length $L=20$ nm, Silicon thickness $T_{Si} = 10$ nm, $V_{ds} = 1$ V

been tuned. The electron/hole effective masses used in the study are $0.29m_0/0.36m_0$ respectively, where m_0 is the rest mass of the electron, and the carrier life times tuned for electron/hole are $10\mu s/3\mu s$ respectively. The calibrated results are shown in **Fig. 2**. The calibration is done with intention to keep the reported result and TCAD simulation results within an error of $\pm 4\%$. For device calibration the tuning of carrier life times and carrier effective mass has been done [18]–[21]. For n-TFET, Source is p-type with doping concentration $10^{20}/cm^3$, drain is n-type with doping concentration $5 \times 10^{18}/cm^3$ and the channel region is lightly p-type doped with doping concentration $10^{17}/cm^3$, Gate work function used in the simulations is 4.5 eV. Correspondingly for p-TFET doping profiles are same but the material is changed, gate work function is 5.4 eV. The below table lists all related dimensions of Tunnel FET.

III. INVERTER ANALYSIS

Ring oscillator is a chain of odd number of inverters connected one after other, and the last inverter is connected back to the input of first inverter to meet the sustained oscillations criteria as shown in **Fig. 8**. Since inverter is the basic element for RO, so characteristics of Complementary TFET (C-TFET) based inverter are analysed here, which further can be helpful to understand the possible applications of TFET in the digital and/or analog domain. Thus different characteristics are investigated for C-TFET based inverter. The schematics for C-TFET inverter is shown in **Fig. 3**. All simulations are performed using Sentaurus TCAD (sdevice)

TABLE I
DEVICE PARAMETERS FOR SYMMETRIC SILICON DG TFET

	Parameters	Values
1	L-channel length	50nm
2	T_{si} -channel width	10 nm
3	T_{ox} -gate oxide thickness	3 nm
4	HfO_2 -gate dielectric	$22\epsilon_0$
5	T_{ext} -drain/source extension widths	10 nm, 20 nm, 36 nm
6	N_a -channel doping	$10^{17}/cm^3$
7	N_{ap} -source doping	$10^{20}/cm^3$
8	N_{dp} -drain doping	$5 \times 10^{18}/cm^3$
9	ϕ_m -gate metal work-function	4.5 eV (n-type) 5.4 eV (p-type)
10	V_{dd} -supply voltage	1.5 V, 1.8 V 2.0 V
11	Carrier life times electron/hole	$10\mu s/3\mu s$
12	effective mass electron/hole	$0.29m_0/0.36m_0$

with device channel material as Silicon and gate insulator material used as HfO_2 .

A. Static Transfer Characteristics

The static transfer characteristics for both N-channel and P-channel Si DG Tunnel FETs are discussed in this section to understand the characteristics basic C-TFET inverter. To explain the static characteristics, a resistive equivalent circuit of a TFET is taken into account by considering R_S/R_D source/drain extension region resistances respectively which are fixed and independent on the applied gate/drain bias voltages, R_T is the tunnel junction resistance which completely depends on the applied gate, and drain voltages. This tunnel junction barrier decreases with both applied drain, and gate voltage as well. R_C —is the channel resistance. The static transfer characteristics are represented in **Fig. 4**. It is clear from these plots that the drain current of the device (N-channel or P-channel TFET) increases with the extension region width. Here the static voltage transfer characteristics of an inverter are shown in **Fig. 5**.

Since the tunnel FET current is heavily controlled by the tunnel junction resistance R_T and also by R_S , R_D , R_C as well. Here R_T is a function of both gate and drain voltages, thus it will change drastically as V_{gs} or V_{ds} is changed. R_T is very high at lower drain/gate voltages, thus the drain current is very low for lower drain/gate voltages. As soon as the carriers start tunneling at the source/channel junction, the drain current is controlled by R_D and R_C , where drain/source extension region resistances (R_S and R_D) will get reduced with increasing in width of extension region, which in turn increases the drain current of the TFET devices, as shown in **Fig. 5a** and **Fig. 5b**.

B. Voltage Transfer Characteristics

For digital systems/circuit applications, the voltage transfer characteristics (VTC) for C-TFET inverter plays significant role while the inverter gain plots are useful for

Fig. 3. Inverter schematics under study

analog domain applications such as sensors, amplifiers etc. The VTC for C-TFET inverter for different power supplies ranging from $V_{dd}=1.5V$ to $2.0V$ are shown in **Fig. 5a**. A very small change in the VTCs with variations in extension region width (T_{ext}) have been observed for C-TFET inverter, therefore, VTCs for different extension region widths are not shown separately. $T_{ext}=10$ nm have been used for VTCs.

Different noise margins are observed for different power supplies. The noise margins for all power supplies are listed in **Table II**. Here the lower noise margins (NM_L) are lesser than higher noise margins (NM_H), which indicates that the pull-up transistors (P-channel TFETs) are stronger than the pull-down transistors (N-channel TFETs). The lower noise margins vary from 40% to 41% while the higher noise margins are in a range of 42% to 43.5% of the power supply.

From the above discussion, it can be concluded that there is a sharper transition from high to low and vice versa ($<20\%$ of V_{dd}) for these inverters. The inverter gain, which is very much useful for analog applications is shown in **Fig. 5b**. It is seen that the inverter gain is better for higher power supplies as in the case of MOSFETs [22]. Better inverter gain makes it suitable for amplifier applications. One such application Operational Trans-conductance Amplifier (OTA) has been presented in [23].

C. Transient Characteristics

Inverter's transient characteristics are useful for analysis related to timing, overshoot, undershoot etc. The transient characteristics for both of TFET structures given in **Fig. 1** are presented in **Fig. 6**, a very minute difference between

(a) I-V characteristics for NTFET

(b) I-V characteristics for PTFET

Fig. 4. I_{ds} - V_{gs} characteristics for N-TFET and P-TFET for different extension region TFET widths at applied drain voltage, $V_{ds} = 1V$

the two transient waveform of output voltages V_{out} , for both the structures have been observed, but still there is a difference in terms of the peak undershoot, overshoot, and inverter's delay. Inverter delay will be discussed in the next section IV, with RO. The peak overshoot, and undershoot occurs because of Miller capacitance, which is more for TFETs as compared with MOSFETs [24], [25] which makes the undershoots and overshoots higher for TFET as compared to MOSFET as shown in **Fig. 6** and **Fig. 7**, for CMOS the simulation has been done online for $0.35\mu m$ gate length (aim is just to shown that there is no overshoot and undershoot in case of CMOS) using NGSPICE online simulator, even if the CMOS inverter

TABLE II
INVERTER NOISE MARGINS FOR SOURCE/DRAIN EXTENSION REGION WIDTHS $T_{ext} = 10nm$ AND POWER SUPPLY $V_{dd} = 1.5V, 1.8V$ AND $2.0V$

$V_{dd}(V)$	$NM_H(V)$	$NM_L(V)$
1.5	0.63	0.62
1.8	0.765	0.74
2.0	0.87	0.80

simulations are done for higher V_{dd} (up to 3V for this technology node) the undershoot and overshoot are observed much far lesser than TFET.

For both of TFET structures, the fringe capacitance is different. The fringe capacitance is given as shown in Eq. (1). Since the Miller capacitance is the sum of fringe capacitance (C_{fringe}) and the gate-drain capacitance (C_{gd}) Eq. (2), thus the fringe capacitance has its own effect on the transient characteristics.

$$C_{fringe} = \frac{\epsilon_{fringe}}{T_{fringe}} \quad (1)$$

$$C_{Miller} = C_{fringe} + C_{gd} \quad (2)$$

Since the average fringe width T_{fringe} gets reduced as the extension region width T_{ext} increases, this will cause the fringe capacitance in Eq. (1) to increase while the extension region resistances R_S , and R_D to decrease. The combined effect of both of these will decide the peak overshoot, undershoot, and low-to-high (T_{plh}), and high-to-low (T_{phl}) inverter delay. The average propagation delay (T_d) of inverter is estimated by Eq. (3)

$$T_d = \frac{(T_{plh} + T_{phl})}{2} \quad (3)$$

The transient characteristics for $V_{dd}=1.5V$ are shown in **Fig. 6a**, and the undershoot, overshoot are shown in **Fig. 6b** for extension region width 10 nm and 36 nm. Although the study is carried out for intermediate extension region widths as well, but in order to avoid complexities in diagrams, only 10 nm, and 36 nm results are presented. It is clear that at higher T_{ext} , a higher value of the peak overshoot, and undershoot potentials are obtained, which is because of increased fringe capacitance, while T_{phl} and T_{plh} will get reduced with the increased T_{ext} due to reduced extension region resistances.

Here Fig. 7, SPICE simulated graph is included just to show that the overshoot and undershoot in CMOS based inverter is negligible as compared to CTFET inverter at the same power supply, (here technology node is different because for TFET higher supply voltage is needed as compared to MOSFETs).

(a) Voltage Transfer Characteristics for different extension region TFET inverter widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

(b) TFET inverter gain for different extension region widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

Fig. 5. Voltage Transfer Characteristics for different extension region TFET inverter widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

IV. RING OSCILLATOR APPLICATION

Ring oscillator can be fabricated along the chip which contains odd number of inverters connected back to back in order to meet Barkhausen criteria for self sustained oscillations i.e. it must provide a phase shift of 2π and have unity close loop gain. The frequency of the oscillations can be controlled by supply voltage variations thus it can be referred as VCO.

In an n -stage ring oscillator the phase shift of π/n is provided by each inverter stage, the rest π phase shift is provided by the static inversion. The frequency (f) of

(a) Full transient characteristics of C-TFET inverter for applied supply voltage $V_{dd} = 1.5V$

(b) Overshoot and undershoot transient characteristics of C-TFET inverter for applied supply voltage $V_{dd} = 1.5V$

Fig. 6. Transient characteristics of C-TFET inverter for applied power supply $V_{dd} = 1.5V$, the 'red color solid circle -o-' represents data for $T_{ext} = 10nm$ and the 'blue color solid triangle -△-' symbol represents the data for $T_{ext} = 36nm$

ring oscillator is given by Eq. (4). It can be seen here the frequency of oscillation is inversely proportional to the number of stages (n) used in the ring oscillator. Thus larger the number of stages, lesser the frequency of operation (if the single inverter stage delay T_d is constant).

$$f_{RO} = \frac{1}{2 * n * T_d} \quad (4)$$

Ring Oscillator time period $T_{RO} = 2 * n * T_d$.

To investigate the effect of drain extension width (T_{ext}) and supply voltage (V_{dd}) variations -on RO frequency, a simulation based study is performed for various parametric variations. A three stage ring oscillator is presented in Fig. 8, which is the minimum possible number of stages in RO. The RO is most widely used in PPLs, VCOs, clock generation, communication, multi-phase outputs etc.

Fig. 7. Transient characteristics of CMOS inverter with $V_{dd} = 1.5V$, showing negligibly small overshoot and undershoots as compared to TFET inverter

Fig. 8. Three stage single ended ring oscillator under study

A three stage ring oscillator is simulated with $V_{dd} = 1.5V$ and the output self sustained oscillations are represented in **Fig. 9**. Here the oscillations exceed the power supply voltage level because of higher Miller capacitance in TFETs as compared to CMOS RO, where the oscillations are within 0 to V_{dd} range and overshoot/undershoot voltages are very small as compared to the TFET based inverter as shown in **Fig. 10**.

The oscillation does not start immediately but it starts after certain time period **Fig. 9a**, this time period is known as oscillator's warm-up time. During this time period all inverter stages have constant and same in magnitude and phase outputs which are equal to $V_{dd}/2$. After the warm-

Fig. 9. Ring Oscillator output characteristics for power supply $V_{dd} = 1.5V$, for three stage single ended topology

up phase the oscillator starts oscillations which will attain a fix frequency after a small time duration. Now the outputs of the different stages will be $\frac{\pi}{n}$ out of phase but same in magnitude and ΔT jitter induced by each RO inverter stage.

The simulations are performed using three stages of inverters for **Table III** and **Table IV**. In **Table III**, a fixed $T_{ext} = 10$ nm is taken and power supply voltage is varied from 1.5 V to 2.0 V. and various T_{ext} from 10 nm to 36 nm. It is clear from **Table III** and **Fig. 11**, as the power supply is increased f_{RO} also increases as in case of CMOS based inverters [22] and the overshoot of the inverters is also increased. There is a distorted waveform for oscillations which can be improved by using increasing the number of inverter stages but it will also cause lower frequency output. The speed of operation i.e. frequency of C-TFET ring oscillator is lesser as compared with CMOS RO at the same power supply (**Table III**), while the peak overshoot is much higher as compared with CMOS because of increased

Fig. 10. CMOS based three stage ring oscillator with $V_{dd} = 1.5V$

Miller capacitance in TFETs [24], [25].

TABLE III
OSCILLATION TIME AND FREQUENCY FOR DIFFERENT POWER SUPPLIES
FOR SIMPLE SINGLE ENDED TFET- THREE STAGE RO WITH
 $T_{ext} = 10nm$

$V_{dd}(V)$	$T_{RO}(ns)$	Freq. (f_{RO})	$T_d(ps)$	$V_{Peak}(V)$
1.5(CMOS)	1.6	0.625GHz	266.66	1.5
1.5	2.2715	0.440 GHz	378.58	1.702
1.8	1.1789	0.848 GHz	196.48	2.021
2.0	0.8077	1.238 GHz	134.62	2.246

TABLE IV
OSCILLATION TIME AND FREQUENCY FOR DIFFERENT DRAIN REGION
WIDTH FOR THREE STAGE RO WITH $V_{dd} = 2V$

T_{ext}	$T_{RO}(ns)$	Freq. (f_{RO})	$T_d(ps)$	$V_{Peak}(V)$
10nm	0.80769	1.2381 GHz	134.615	2.246
26nm	0.76934	1.2998 GHz	128.223	2.294
36nm	0.76188	1.3125 GHz	126.98	2.302

Here V_{peak} is the peak overshoot voltage of ring oscillator, T_{RO} is the time period of each output of RO, $f_{RO}=1/T_{RO}$ is the frequency of oscillation for RO, $T_d=T_{RO}/(2*n)$ is single inverter delay calculated from RO.

To see the effect of T_{ext} on the ring oscillator, the T_{ext} is varied from 10 nm to 36 nm in structure of RO with $V_{dd}=2.0V$, as shown in **Table IV** and **Fig. 11**. Here the speed of operation increases at the cost of increased overshoot and undershoot. As the drain extension region width T_{ext} is increased the Miller capacitance will also get increased as shown in Eq. (2), and Eq. (1). This enhanced Miller

capacitance increases the peak overshoot and undershoots. Although the Miller capacitance has been increased but a reduction in the extension region resistance R_d is seen due to width increase. The combined effect of R_d and C_{Miller} will increase the speed of operation as shown in **Table IV**. The effect of T_{ext} and V_{dd} on the frequency of RO is also presented in **Fig. 11**. Further, as the number of stages is increased from three to five the frequency will decrease according to Eq. (4), the same can be compared from **Table III** and **Table V**.

Fig. 11. Variations in RO frequency with supply voltage and extension region width 'red' line is supply versus f_{RO} and 'black' line is for T_{ext} versus f_{RO}

TABLE V
OSCILLATION TIME AND FREQUENCY FOR SIMPLE AND SKEWED DELAY
FOR FIVE STAGE RO WITH $V_{dd} = 1.8V$ AND $T_{ext} = 10nm$

RO Topology	$T_{RO}(ns)$	$f_{RO}(GHz)$	$T_d(ps)$	Jitter	V_{Peak}
Simple RO	2.5784	0.388GHz	257.84	2.04ps	2.38V
Skewed delay	0.7054	1.418GHz	70.54	0.008ps	1.33V

The single ended topology of ring oscillator is the simplest form of oscillator, but the frequency of this oscillator is not fix, it suffers from higher jitter (ΔT) - a time delay is induced in the next cycle. To overcome the effect of jitter and to make the oscillator a bit faster **NSD** ring oscillator topology is proposed in [26]. To see details and the circuit-level diagram of simple (single ended inverter based RO) and NSD ring oscillator topology are shown in **Fig. 8** and **Fig. 12** respectively. In NSD ring oscillator topology the nTFETs are having connected in the same manner while the pTFETs are fed inputs from $(n-2)^{th}$ stage in order to reduce the jitter and make the oscillator faster. The simple topology can have even three stages also but the NSD ring oscillator topology can minimum have five stages. The NSD ring oscillator topology is faster because its oscillation has

Fig. 12. Five stage negative skewed delay ring oscillator topology

much smaller magnitude as compared to the single ended inverter topology of ring oscillators as presented in **Table V**, thus lesser time is required to switch in either states. Comparison of frequency of operation at $V_{dd} = 1.8V$ is presented in **Table V**. It is found that the frequency of operation in case of NSD RO is 3.65X times of the simple single ended RO, this happens because the amplitude of sinusoidal wave generated by NSD RO is 60% of its power supply as shown in **Fig 13b** while in case of simple RO it is 150% of the power supply.

Further the jitter has also reduced as compared with simple RO. Here it can be seen that because of larger overshoot in case of TFET the amplitude of the sinusoidal wave generated is much more than the conventional MOS-FET device RO [26]. Further, as the number of stages are increased in the RO, the operation speed will get reduced because the inverters used are of same size. The comparison can be understood from **Table III** and **V**. At $V_{dd}=1.8V$ and with $n=3$, RO is operating with $f_{RO}=0.848$ GHz while for $n=5$ the RO's operating frequency is $f_{RO}=0.388$ GHz.

The RO overshoot, peak to peak voltage, and frequency also depend on the technology used in inverter device. For CMOS based RO the full swing 0 to V_{dd} is obtained in oscillations and the frequency is higher than TFET. There are distortions in the outputs of RO which can be reduced either by increasing the number of stages or using DTMOS like techniques for TFETs also.

RF and mobile Applications

The range of Radio Frequencies (RF) is from 300 KHz to 300 GHz. It can be seen from **Table III** and **IV**, a wide range of frequencies can be tuned with the help of power supply by end user by taking the advantage of late saturation of TFET devices. This tuning can be done by the end user but if it is desired to design an integrated RO

(a) Ring oscillator outputs for 5 stage single ended inverter chain

(b) Ring oscillator outputs for 5 stage negative skewed delay topology as mentioned in [26]

Fig. 13. Simple single ended and negative skewed delay Ring Oscillator outputs for showing faster operation and lesser jitter for power supply $V_{dd} = 1.8V$

for a particular application e.g. frequency of operation 900 MHz for mobile communication. In such case the frequency tuning with T_{ext} can also play a vital role for RO, as for double gate devices the drain extension resistance is going to become a big problem.

Comparative study of **Table III** and **IV** or **Fig. 11** shows that increasing V_{dd} or T_{ext} although increases the frequency of operation but it also increases the signal swing ($V_{Peak}-V_{min}$) and simple RO waveform is much distorted as compared to NSD RO topology. Therefore, its better to use NSD RO as it give 60% of V_{dd} waveform swing, **Fig. 13**, which in turn is responsible for lesser power dissipation, and multiple times (3.6X in this case) frequency of operation with less wave distortions. Depending on the application the tuning can be done from few hundred KHz to few GHz range.

V. CONCLUSIONS

Tunnel FET based ring oscillator (RO) study is presented with drain extension region width and power supply variations (works like Voltage Controlled Oscillator-VCO) of Si-DG TFET. The effects of drain extension region resistance on the Tunnel FET inverter (hence on RO) has been explained with its impact on device characteristics and applied to RO. As the drain extension region width is increased the propagation delay of RO decreases that in turn makes the device faster while the peak overshoot and undershoot increases. Thus, a trade off must be maintained in order to get best results in terms of frequency, and switching power dissipation ($C * V^2 * f$). Ring oscillators frequency can be tuned by the end user by tuning the power supply as well. RO faces the problem of jitter introduced in subsequent stages, to remove this jitter and make the oscillator more reliable a previously reported negative skewed delay ring oscillator (NSD RO) is designed, and simulated for comparative study with single ended simple RO. It is found on the basis of observations that the NSD RO have lesser jitter, faster speed for its single ended RO topology counterpart. It is also found that the larger the extension drain/source width, frequency will be more for the device. The comparison also includes the variations in drain extension region and its impact on the inverter, and therefore, on RO characteristics. The possible application in RF frequency range tuning with adjusting power supply by the end user, and drain extension width at the manufacturer is also discussed.

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Figures

(a) Tunnel FET structure without widening the extension regions

Figure 1

Different Tunnel FET structures under study with gate length 50nm and channel thickness 10nm.

Figure 2

I_{ds} – V_{gs} Calibration with the previously reported work in [17] (which is already calibrated against the experimental data presented Bhuwalka et al.), for this calibration all physical dimensions are used from [17], DG Tunnel FET with high-k gate oxide with $EOT=0.9\text{nm}$, channel length $L=20\text{ nm}$, Silicon thickness $TSi = 10\text{nm}$, $V_{ds} = 1\text{V}$

Figure 3

Inverter schematics under study

(a) I-V characteristics for NTFET

(b) I-V characteristics for PTFET

Figure 4

I_{ds} - V_{gs} characteristics for N-TFET and P-TFET for different extension region TFET widths at applied drain voltage, $V_{ds} = 1V$

(a) Voltage Transfer Characteristics for different extension region TFET inverter widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

(b) TFET inverter gain for different extension region widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

Figure 5

Voltage Transfer Characteristics for different extension region TFET inverter widths with voltage supply $V_{dd} = 1.5V, 1.8V$ and $2.0V$

(a) Full transient characteristics of C-TFET inverter for applied supply voltage $V_{dd} = 1.5V$

(b) Overshoot and undershoot transient characteristics of C-TFET inverter for applied supply voltage $V_{dd} = 1.5V$

Figure 6

Transient characteristics of C-TFET inverter for applied power supply $V_{dd} = 1.5V$, the 'red color solid circle -●-' represents data for $T_{ext} = 10\text{nm}$ and the 'blue color solid triangle -▲-' symbol represents the data for $T_{ext} = 36\text{nm}$

Figure 7

Transient characteristics of CMOS inverter with $V_{dd} = 1.5V$, showing negligibly small overshoot and undershoots as compared to TFET inverter

Figure 8

Three stage single ended ring oscillator under study

(a) Complete output waveform

(b) Zoom of Fig. (a)

Figure 9

Ring Oscillator output characteristics for power supply $V_{dd} = 1.5V$, for three stage single ended topology

Figure 10

CMOS based three stage ring oscillator with $V_{dd} = 1.5V$

Figure 11

Variations in RO frequency with supply voltage and extension region width 'red' line is supply versus f_{RO} and 'black' line is for Text versus f_{RO}

Figure 12

Five stage negative skewed delay ring oscillator topology

(a) Ring oscillator outputs for 5 stage single ended inverter chain

(b) Ring oscillator outputs for 5 stage negative skewed delay topology as mentioned in [26]

Figure 13

Simple single ended and negative skewed delay Ring Oscillator outputs for showing faster operation and lesser jitter for power supply $V_{dd} = 1.8V$