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Savio Jay Sengupta (✉ saviojsengupta@gmail.com)

Jadavpur University <https://orcid.org/0000-0002-5504-0662>

Bijoy Goswami

Jadavpur University Faculty of Engineering and Technology

Pritam Das

Jadavpur University Faculty of Engineering and Technology

Subir Kumar Sarkar

Jadavpur University Faculty of Engineering and Technology

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A Noise Immune Double Suspended Gate MOSFET for Ultra Low-Power Applications

Savio Jay Sengupta^{1*}, Bijoy Goswami¹, Pritam Das¹, Subir Kumar Sarkar¹

¹ Department of Electronics and Telecommunications, Jadavpur University, Kolkata-700032, India

*saviojsengupta@gmail.com

Abstract:

Purpose - The purpose of this paper is to develop the design and analytical modelling of a noise immune double suspended gate MOSFET (DSG-MOSFET) for ultra-low power applications. Also, Important performance parameters of the proposed structure such as pull-in and pull-out voltages have been thoroughly investigated with respect to the valuable structural parameters.

Methods- The design methodology used is EKV based analytical approach to calculate the pull-in and pull-out voltages with ingeniously developed boundary conditions which helps achieving reasonably accurate result. Also, the I-V characteristics has been modelled to justify accuracy.

Results- The experimental result shows that the pull-in and pull-out voltages are in millivolts and microvolts range and hence it can be used in ultra-low power applications. As the ratio between the pull-out and the pull-in voltage is $10^{(+3)}$ range, justifies that the proposed structure is noise immune. The I_D - V_{GS} characteristic has hysteresis and this sharp transition in pull-in and pull-out voltage indicates that it can be used as an ideal switch with infinite sub-threshold slope.

Conclusion- This paper presents a compact EKV based analytical modelling of pull-in and pull-out voltages for a DSG-MOSFET which predict the device characteristics reasonably similar to simulated results. Also, for the first time the noise immunity for a DSGMOSFET has been analyzed.

Keywords: Double suspended gate MOSFET (DSGMOSFET), Microelectromechanical system (MEMS), Noise immunity, Data encryption, Mechanical Hysteresis, COMSOL.

Author Declarations:

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1. Introduction

One of the main disadvantages of CMOS architecture is the scalability of the device. Up to some range the dimension of MOSFET can be reduced and with that the other parameters such as supply voltage, threshold voltage etc. without any adverse effect on the performance of the device. However, it can be seen that when the threshold voltage (V_{th}) is scaled below or equal to 150mV, it results in huge off current [1] due to the subthreshold slope (SS) constraint in case of this architecture. However, this limitation can be overcome by suspended gate field effect transistor (SGFET). SGFETs are overpowering the CMOS architecture in terms of standby power consumption which is very low in the previous one [2]. Hence, the switching characteristics for SGFETs are almost ideal, therefore these can be used as sleeping transistors which leads to efficient power management. The power management characteristics of SGFETs, make the device an advantageous one over CMOS architecture for low power applications.

More than 52 years ago, the idea of combining a mechanical switch, which is electrostatically actuated, with a MOSFET was introduced [3]. The motivation behind this innovative idea was to get a more stable structure which can operate more properly at high frequency [2]. This MEMS/FET hybrid structures had been implemented as gas as well pressure sensors with some eye-catching results [4,5]. SGFETs can have a SS below 60mV/dec was first time proposed in 2002 [6]. After that, multiple research articles have investigated the opportunity for SGFETs to be implemented as resonators, memory and most importantly as switches [5-11]. Another advantage of SGFETs is that the fabrication of these devices is CMOS compatible and the evaluated characteristics supports the theoretical prediction of having SS lower than 60mV/dec [5-12]. Also, accumulation mode SGFETs are reported in [13].

Gate to channel modelling [6] of SGFETs based on EKV (Enz-Krummenacher-Vittoz) [14] has been reported previously. This model is also valid for all operational regimes. However, some shortcoming of this model, such as huge time consumption as it is an iterative method, was also reported in [2]. Hence, to overcome this limitation, a static model for SGFET has been developed by considering only the operational region of interest [2]. However, this mathematical model was for a single suspended gate FET. For first time, the mathematical model for a double suspended gate MOSFET has been reported in this acritical. This model gives the inside knowledge of DSGMOSFETs performance as well as the basic design rules. This article also reports the mathematical modelling for the compared structure which is depicted in figure 1(e).

The article is organized as follows: the operation of DSGMOSFET and the respected mathematical modelling for both a) proposed as well as b) compared structures is given in section II. Section III includes the performance comparison between the proposed as well the compared structure. In, Section IV, the proposed structure is analysed in depth and section V includes the conclusion.

2. WORKING PRINCIPLE AND ANALYTICAL MODELLING

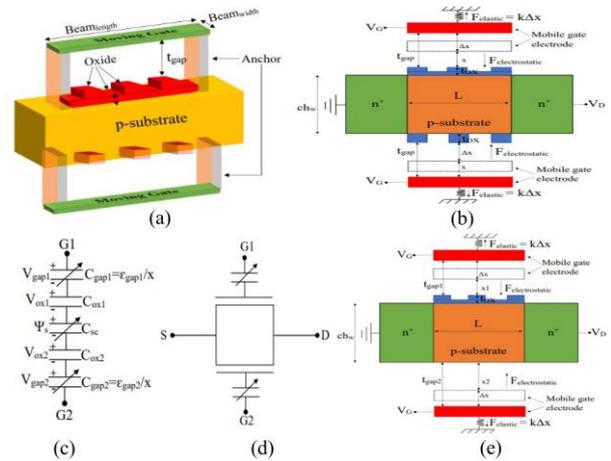


Fig 1 (a) 3D representation of DSGMOSFET, (b) Cross-section of the proposed Structure, (c) Corresponding capacitor circuit (d) Symbol representation of DSGMOSFET, (e) Compared Structure

The 3-D as well as cross section version of the proposed DSGMOSFET is showed in Fig 1(a) and Fig 1(b). Fig 1(c) depicts the equivalent capacitor circuit of DSGMOSFET and Fig 1(d) shows the symbol representation of n-channel DSGMOSFET. The compared structure, without the lower gate oxide, has been given in Fig 1(e).

DSGMOSFET is a hybrid combination of an inversion MOSFET and electrostatically actuated mechanical NEMS switch (Fig 1). The main difference of DSGMOSFETs from a MOSFET is that there is the presence of air between the gate oxides and the double gates which has been supported by anchors as show in Fig 1(a). In case of fabrication of any SGFET structure, can be done by using sacrificial etching of the respected material which can be place on the gate oxide before the completion of gate [7],[12],[15]. However, by this

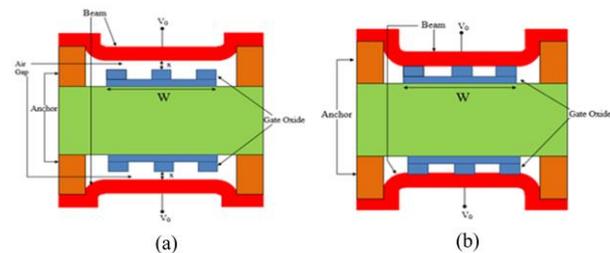


Fig 2 (a) Before the bending of DSGMOSFET, (b) After double gates collapsed on the gate oxides

technique the archived air gap is in the range of few hundred nanometers [5],[7],[12] which in turn will make the structure huge in size and also makes the device potentially unavailable to be used in ultra-low power applications. But, by using atomic layer deposition, an air gap of 10nm has been achieved [16] and it has been used in biosensing applications as well [17]. However, the main constraint is the width of the suspended gate [17]. If the width is too large then it will affect the bending of the gate hence the pull in and pull-out voltages will increase, hence power dissipation will also increase. Due

to increments in both pull-in and pull-out voltages, the noise immunity will be affected the most. By considering all the above reasons, beam widths of 1nm for both the gates has been considered for the proposed structure with a t_{gap} of 10nm and t_{ox} of 2nm. For the compared structure, all the parameters are same except the fact that there is no lower gate oxide present in the compared structure. AlSi [12] or polysilicon [15] can be used as gate materials, polysilicon has been chosen for the both proposed and compared structure.

The working principle of the proposed DSGMOSFETs can be explained in the following way: both the gates are shorted and a gate voltage of V_G has been applied. When gate voltage (V_G) is equal to the flatband voltage (V_{FB}), then the air gaps for both the case is $t_{gap} = x$ [Fig 1(b)] as there is no charge accumulation in both the electrode and in the semiconductor, 'x' represents the initial distance between gate insulator and the moving gate. As V_G start to increase, positive charges start to accumulate in both the moving gates and also equivalent negative charges accumulate in the silicon substrate which results in $x < t_{gap}$. Now below the pull in voltage, there will be no bending in both the moving gates as the electrostatic force is balanced by the elastic forces which are acting on the both gates [Fig 1(a)]. Therefore, when V_G exceeds or become equal to pull in voltage V_{pi} , then the electrostatic forces in both the gates over powered the elastic forces, hence both the gates collapsed (pulled in) on both gate oxides [Fig 2 (b)] due to which the threshold voltage abruptly reduced which leads to a sudden drain current increase [6].

For compared structure [Fig 1(e)], the working principle will remain almost same but the absent of the lower gate oxide will play an essential role in the device operation. It can be observed from Fig 1(b) and Fig 1(e) that the compared structure has two different distances from two gates i.e. x_1 and x_2 . It also has two different air gap values i.e. t_{gap1} and t_{gap} . Hence, two different pull in and pull-out voltages will be obtained for the compared structure and discussed in analytical modelling section. Another important difference between these two structures that the first one [Fig 1(b)] (the proposed structure) will be working perfectly as MOSFETs for both the gates, however in case of compared structure [Fig 1(e)], the lower gate oxide is absent and hence, for the upper gate the device will work as a MOSFET but for lower gate it will work as a metal-metal switch. Both structures have significant improvements over [2], but the proposed one is more advantageous in terms of power dissipation and noise immunity which is discussed in later.

2.1. Pull-in modelling

The electrostatic force, applied between the channel and the gate, that governs the beam displacement is given by the force stiffness relationship. The total energy between two conductive plates is considered for the electro-mechanical analysis and given by

$$U_{tot} = U_{elec} - U_{mech} \\ = \frac{1}{2} C_{gap} V_{gap}^2 - \frac{1}{2} kx^2 \quad (1)$$

At equilibrium these two forces balance each other and hence,

$$\frac{1}{2} \frac{\epsilon_{gap} WL V_{gap}^2}{x^2} = k(t_{gap0} - x) \quad (2)$$

Where, W =beam width, L =channel length, t_{gap0} =initial height of the beam from the oxide, ϵ_{gap} =permittivity of air,

V_{gap} =voltage drop across the air gap, x =actual height of the beam from the oxide

k is the spring constant and given as-

$$k = \frac{32ELh^3}{W^3} \quad (3)$$

E is the Young modulus of the moving gate material.

Now V_{gap} can be demonstrated as a function of x and the semiconductor charge density Q_{sc} as

$$V_{gap} = - \frac{Q_{sc}}{\epsilon_{gap} x} \quad (4)$$

Putting the value of eq (3) into eq (2) we get,

$$x = t_{gap0} - \frac{1}{2} \frac{WLQ_{sc}^2}{\epsilon_{gap}} \quad (5)$$

The restoring force linearly depends on displacement and the electrostatic force is inverse quadratic function, hence the stable point can be achieved only when,

$$x_{pi} \leq \frac{2}{3} t_{gap0} \quad (6)$$

Due to the series connection between C_f and C_{gap} , x_{pi} is reduced to

$$x_{pi} \leq \frac{2 - \frac{C_{gap0}}{C_f}}{3} t_{gap0} \quad (7)$$

Where $C_{gap0} = \epsilon_{gap} / t_{gap0}$ is the minimum gap capacitance.

In this case C_f is the series equivalent of C_{ox} with C_{sc} . By considering depletion approximation, the depletion charge can be expressed as a function of the surface potential as

$$Q_d(\psi_s) = -\sqrt{2\epsilon_{si}} \sqrt{qN_A \psi_s} \quad (8)$$

Where,

ϵ_{si} =permittivity of silicon, q = elementary charge, N_A

= substrate doping concentration, ψ_s = surface potential

Putting eq(8) into eq(5) the gate position is expressed as a function of surface potential as

$$x \psi_s = t_{gap0} - \frac{WLE_{si}qN_A}{\epsilon_{gap}k} \psi_s \quad (9)$$

The well-known formulation of V_{pi} for a suspended gate MOS capacitor is

$$V_{pi} = \sqrt{\frac{8k(t_{gap0} + t_{ox} / \epsilon_r)^3}{27\epsilon_{gap}WL}} \quad (10)$$

In second case of our proposed structure the lower oxide is removed, in this case the pull-in voltage will become as the metal-metal NEMS switch as

$$V_{pi} = \sqrt{\frac{8kt_{gap0}^3}{27\epsilon_{gap}WL}} \quad (11)$$

2.2. Pull-out modelling

In this section the pull-out voltage has been discussed, starting from the force acting on the gate while the gate is pulled in. The opposing electrostatic force, restoring elastic force and adhesion force has been considered.

The gate capacitance increases abruptly immediately after the gate is pulled in, and so do the charge density and the surface potential. For $V_G > V_{pi}$ the DSGFET will behave as a conventional DG MOSFET. When V_G swept back from higher value of pull in voltage, the pull-out does not occur at $V_G = V_{pi}$ because the higher charge density causes higher electrostatic force than those at the onset of pull in. The adhesion force between beam electrode and the oxide surface is another cause of this. As a result, the pull-out voltage V_{po} becomes less than V_{pi} which gives a hysteresis in SGFET characteristics.

The force balance equation just before the pull out can be approximated as

$$\frac{WL\epsilon_{ox}V_{ox}^2}{2t_{ox}^2} + F_a = kt_{gap0} \quad (12)$$

The first term of the left-hand side of the above equation represent the electrostatic force whereas the right-hand side is the elastic force. F_a is the surface adhesion force. F_a can be approximated as

$$F_a \cong 2WL \frac{\Gamma}{D_0} \quad (13)$$

From eq(12) the pull-out voltage can be calculated as

$$V_{po} = \sqrt{\frac{2kt_{gap0}t_{ox}^2}{\epsilon_{ox}WL}} \quad (14)$$

For the second structure the pull out voltage becomes

$$V_{po} = \sqrt{\frac{2kt_{gap0}t_{gap}^2}{\epsilon_{gap}WL}} \quad (15)$$

2.3. I_D - V_G characteristics

In strong inversion region the total inversion charge is the summation of the charges induced by both the gates.

$$\text{i.e. } Q_{inv} = Q_{finv} + Q_{binv}$$

$$\text{but } |Q_{finv}| = |Q_{binv}|$$

$$\text{so, } Q_{inv} = 2Q_{finv}$$

Now when the gate voltage increases the intrinsic gate voltage, $V_{g\text{int}}$ becomes

$$V_{g\text{int}} = \frac{V_G}{1 + \frac{C_{gc\text{int}}}{C_{gap}}} \quad (16)$$

Where $C_{gc\text{int}}$ = intrinsic gate to channel capacitance

And C_{gap} = gap capacitance

C_{gc} is given by,

$$C_{gc} = \frac{C_{ox}C_{inv}}{C_{ox} + C_{inv} + C_d} \quad (17)$$

$$= \frac{(\beta-1)/\beta\sqrt{2}\exp[(V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f)/\beta V_{th}]C_{ox}}{(\beta-1)/\beta\sqrt{2}\exp[(V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f)/\beta V_{th}]+1} \quad (18)$$

$$\text{Where, } \beta = 1 + \frac{C_d}{C_{ox}}$$

$$V_{th} = \text{thermal voltage}$$

Now,

$$Q_{inv} = 2 \int_{-\infty}^{V_{g\text{int}}} C_{gc}(V_{g\text{int}})dV_{g\text{int}} \quad (19)$$

or,

$$\begin{aligned} Q_{inv} &= 2 \int_{-\infty}^{V_{g\text{int}}} \frac{(\beta-1)/\beta\sqrt{2}\exp[(V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f)/\beta V_{th}]C_{ox}}{(\beta-1)/\beta\sqrt{2}\exp[(V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f)/\beta V_{th}]+1} dV_{g\text{int}} \\ &= 2\beta C_{ox} V_{th} \ln\left\{\sqrt{2}(\beta-1)/\beta \exp\left[\frac{V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f}{\beta V_{th}}\right]+1\right\} \end{aligned} \quad (20)$$

The drain current, I_D can be written as

$$I_D = -\frac{Q_{inv}WL}{t_r}$$

Where t_r is the transit time of electron from source to drain.

So,

$$\begin{aligned} I_D &= -\frac{\mu Q_{inv}WV_{DS}}{L} \\ &= 2\frac{\mu WV_{DS}}{L} \beta C_{ox} V_{th} \ln\left\{\sqrt{2}(\beta-1)/\beta \exp\left[\frac{V_{g\text{int}}(V_g)-V_{fb}-2\beta\phi_f}{\beta V_{th}}\right]+1\right\} \end{aligned} \quad (21)$$

This is the approximate relationship of drain current vs gate voltage characteristics for our first device structure.

3. COMPARISON BETWEEN TWO STRUCTURES

In this section, the comparison between two structures (proposed & compared) in terms of pull-in and pull-out voltages with respect to the structural parameters has been analyzed. Channel width (T_{si}), air gap (t_{gap}), Young's modulus (E) and the beam thickness (h) of the gates have been considered as major structural parameters. All the parameters for the both the structures are considered as same such as, channel length (L), T_{si} , t_{gap} , oxide thickness (t_{ox}) double suspended beam thickness is taken as 30nm, 50nm, 10nm, 2nm and 1nm. The doping concentration N_A is $10^{18}/\text{cm}^3$ for both the structures. The travel range is a function of doping concentration and with larger doping concentration, it gets minimized which improves the device performance [2]. L and T_{si} are chosen in such a way so that it falls under the small geometry devices. However, at such small geometry short channel effects may occur. Hence, Double gate structure has been considered.

The t_{ox} is considered as 2nm due to the fact that below 2nm, van der Waal forces [2] and Casimir effects [18] will have significant influences on the device performance. The suspended beams will only get mechanically released if the

electrostatic forces become smaller than the restoring elastic forces. However, for $t_{ox} < 2\text{nm}$, the van der Waal force will not remain weak and hence the pull-out voltage will increase which in turn makes the hysteresis window width smaller [2]. Also, from equation (11) it can be observed that the adhesion force is directly proportional to interfacial adhesion energy per unit area and inversely proportional to surface roughness. Due to air presence between the gate oxides and suspended gates, the surface roughness is already very small. However, for the both the structures, a unique finger like oxides (of 2nm) has been considered [Fig 1(b)] so that the surface roughness can get more smaller but also keeping the van der Waal constraint. Hence, F_a is considered negligible in pull-out voltage modelling [equation (14,15)].

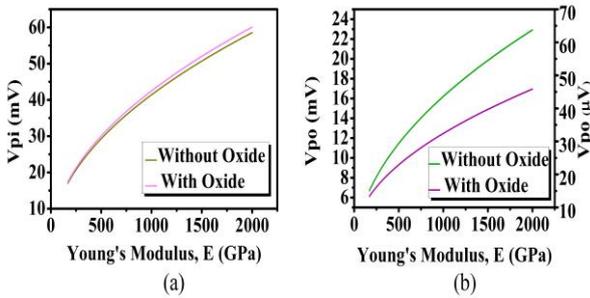


Fig 3. Pull-in (a) and Pull-out (b) voltage variations with respect to Young's modulus for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $t_{gap} = 10\text{nm}$, $t_{beam} = 1\text{nm}$ with the said device parameters.

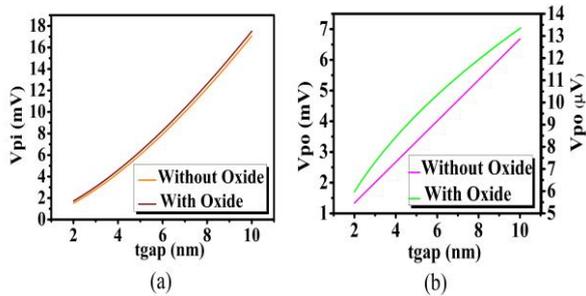


Fig 4. Pull-in (a) and Pull-out (b) voltage variations with respect to t_{gap} for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{beam} = 1\text{nm}$ with the said device parameters.

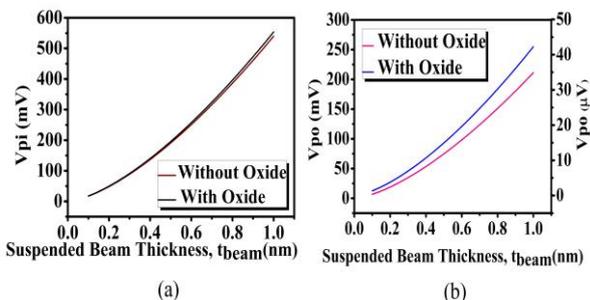


Fig 5. Pull-in (a) and Pull-out (b) voltage variations with respect to t_{beam} for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{gap} = 10\text{nm}$ with the said device parameters.

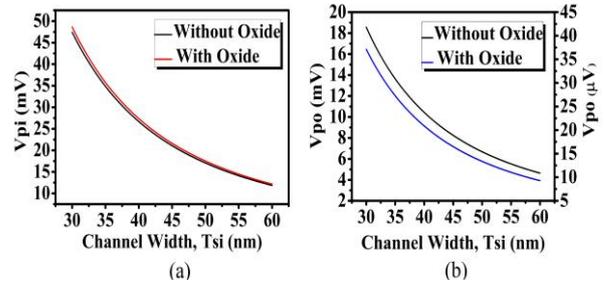


Fig 6. Pull-in (a) and Pull-out (b) voltage variations with respect to T_{si} for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{gap} = 10\text{nm}$, $t_{beam} = 1\text{nm}$ with the said device parameters.

Fig 3,4,5 and 6 depicts the V_{pi} and V_{po} characteristics for varying E , t_{gap} , suspended beam thickness (t_{beam}) and channel width (T_{si}). For both the voltages it can be observed that V_{pi} and V_{po} increase with increase in E , t_{gap} and t_{beam} but decrease with T_{si} . There is a negligible change in V_{pi} for both the structures. Equation (10) and (11) shows the V_{pi} for proposed and compared structure and it is clear that as the oxide thickness is in addition with t_{gap} for equation (10), hence it will not affect the V_{pi} significantly even when t_{ox} is absent [equation (11)] and also t_{gap} , E and t_{beam} are in direct proportional with V_{pi} whereas T_{si} is inversely proportional. However, there is a significant change in V_{po} for the both the structures. Equation (14) and (15) shows the V_{po} for both the structures. As the lower gate oxide is absent in case of compared structure, hence t_{ox} and ϵ_{ox} of equation (14) is replaced by t_{gap} and ϵ_{gap} in equation (15) and hence significant change can be observed. Fig 3(b) also shows that V_{po} is in millivolt range for without lower gate oxide structure (compared) and is in micro volt range for with lower gate oxide structure (proposed). Hence, the proposed structure shown in Fig 1(b) is the preferred structure due to lower power consumption.

4. ANALYSIS OF THE PROPOSED STRUCTURE IN DEPTH

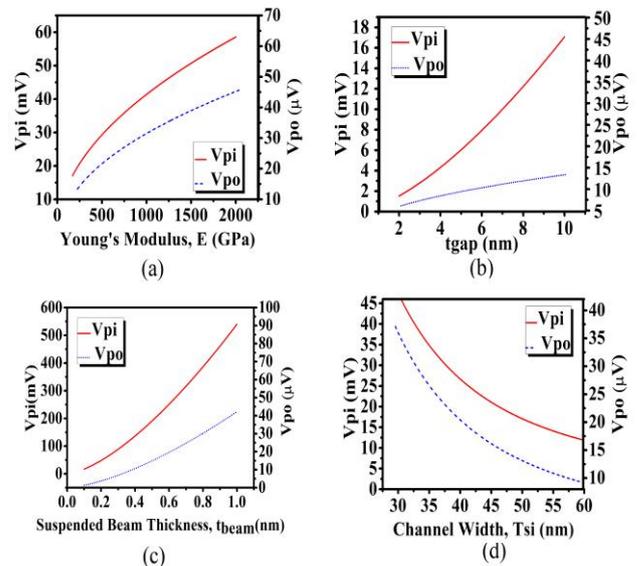


Fig 7. Pull-in and Pull-out voltage variations with respect to (a) Young's modulus of gate material (E) (b) t_{gap} (c) t_{beam} (d) T_{si} for the proposed structure.

Figures 7(a)-(d) depicts the variation of pull-in and pull-out voltages with respect to several structural constraints. The Young modulus is varied from 170Gpa to 2000Gpa. As the young modulus is increasing the beam gets stiffer and as a result the pull-in and pull-out voltage increase. The air gap t_{gap} is varied from 2nm to 10 nm. As it increases, the V_{pi} and V_{po} also increase due to the fact that with increasing the air gap the electrostatic force also increases which in turn makes the two voltages high. The same analysis can be done for the suspended beam thickness, t_{beam} which is varied from 0.1nm to 1nm. But in case of channel width T_{si} , which is varied from 30nm to 60 nm the pull-in and also the pull-out voltage decrease with increasing the channel width. It has been noted that excessive increasing the channel width or excessive lowering the E , t_{gap} , t_{beam} there is a sticking chance of the beam on the oxide as the elastic force become no longer strong as the adhesion force, $F_a < k t_{gap}$.

The on to off capacitance ratio is an important parameter for a RF switch which should be larger than 100. Typical DSGMOSFET switching capacitance characteristics is shown in Fig 8.

As per the analyzed result, the proposed structure has a on capacitance to off capacitance ratio, $c_{on}/c_{off} = 265.39$ which can be considered as a better result. Here the value of $t_{ox} = 2nm$. The threshold voltage of the device is set as $V_{th} = V_{pi}$. The modulation of the threshold voltage can be done by changing the pull-in voltage

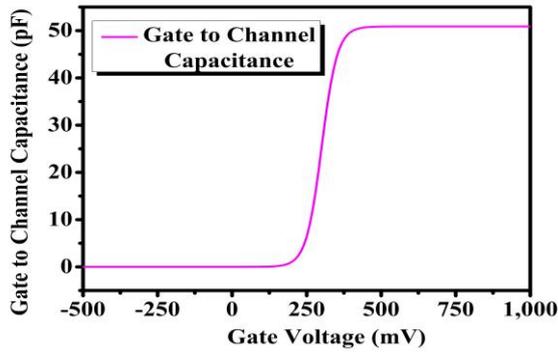


Fig 8. Gate to channel capacitance vs Gate Voltage

It is also found that when $t_{ox} > 2nm$, it does not have any adverse effect on the pull-in voltage [6] which can be confirmed by Fig 9 and also confirmed the reason behind taking $t_{ox} = 2nm$

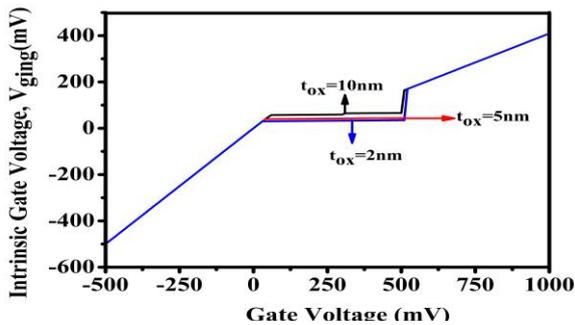


Fig 9. Intrinsic gate voltage vs extrinsic gate voltage, t_{ox} as parameter

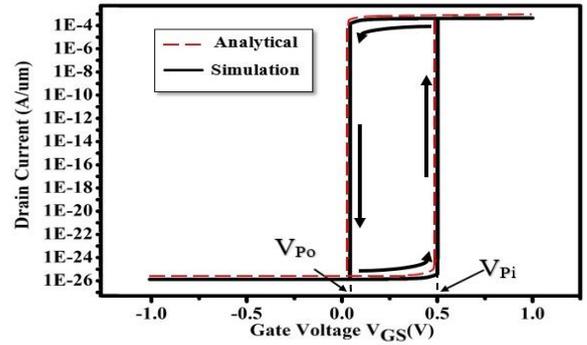


Fig 10. Drain current – Gate voltage characteristics

Fig 10 describes the nature of I_D vs V_G characteristics of the proposed structure of the DSGFET. As it is a short-channel device, the influence of V_D on V_{pi} and V_{po} can be noticed, but which can be minimized by increasing the substrate doping [2]. As L is smaller, the electrostatic force and the fringing fields applied to the double suspended gates by the source and drain regions become an important factor also. The I_D - V_{GS} characteristic has hysteresis, that means the pull-out voltage is lower than the pull-in voltage. An improvement to be noticed on the I_{ON}/I_{OFF} ratio than the conventional single gate SGFET [2]. The sharp transition in V_{pi} and V_{po} indicates that it can be used as an ideal switch with infinite sub-threshold slope [2].

Noise Immunity:

As per the detailed analysis and the graphs (Fig 5 & 6), it can be observed that V_{pi} and V_{po} , for the proposed structure, are in millivolt and microvolt range. However, for the second structure (compared) both the V_{pi} and V_{po} are in millivolt range. Hence, for the proposed structure there is a difference of 1000 times between V_{pi} and V_{po} . Now in any digital circuit, if noise arrives then there is a chance that the voltage level may get changed or shifted from lower level to higher level or vice versa. Due to which the stored data in the system will get changed and it will provide erroneous data as outputs. So, system performance is highly dependent on noise. However, as there is a huge difference between V_{pi} and V_{po} of the proposed structure, if any noise arrives then the probability of that noise to change the voltage levels of the data is very low. Hence, the stored data of the system will remain safely encrypted which makes this structure noise immune. But this can't be said for the second (compared) structure although in terms of power consumption it is providing better performance than [2]. But with respect to the proposed structure, it will consume more power as both V_{pi} and V_{po} are in millivolt range. Also, there is no huge difference between those two voltages, hence in terms of noise immunity, the compared structure is not noise immune like the proposed structure. Hence, the structure depicted in Fig 1(b) is considered as the proposed structure over the structure depicted in Fig 1(e) in terms of both noise immunity and low power consumption, which enable the proposed structure to be used in ultra-low power applications.

5. Conclusion

Two different double suspended gate structures have been designed and also performance of those structures has

been analysed with respect to the several structural dimensional parameters. Based on lower power consumption and noise immunity, the first structure [Fig 1(b)] performs better than the second structure [Fig 1(e)]. Hence, the first structure has been considered as the proposed structure. Also, the proposed structure possessed a better I_{ON}/I_{OFF} ratio over single suspended gate MOSFETs. Analytical modelling of the proposed DSGMOSFETs as well as the compared structure has been developed. The proposed structure can be used in any ultra-low power applications as the V_{pi} and V_{po} are in millivolts and microvolts range.

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Figures

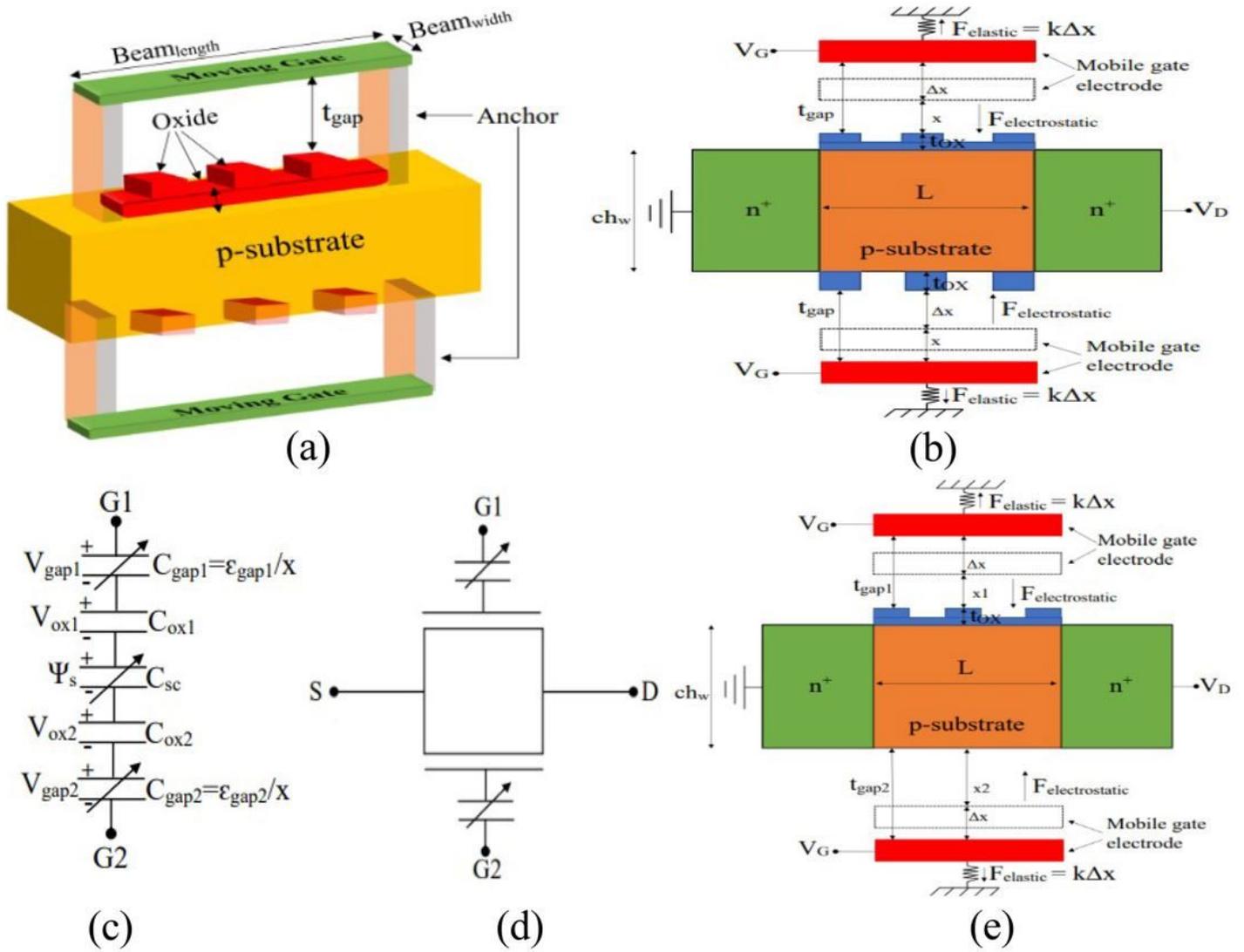


Figure 1

(a) 3D representation of DSGMOSFET, (b) Cross-section of the proposed Structure, (c) Corresponding capacitor circuit (d) Symbol representation of DSGMOSFET, (e) Compared Structure

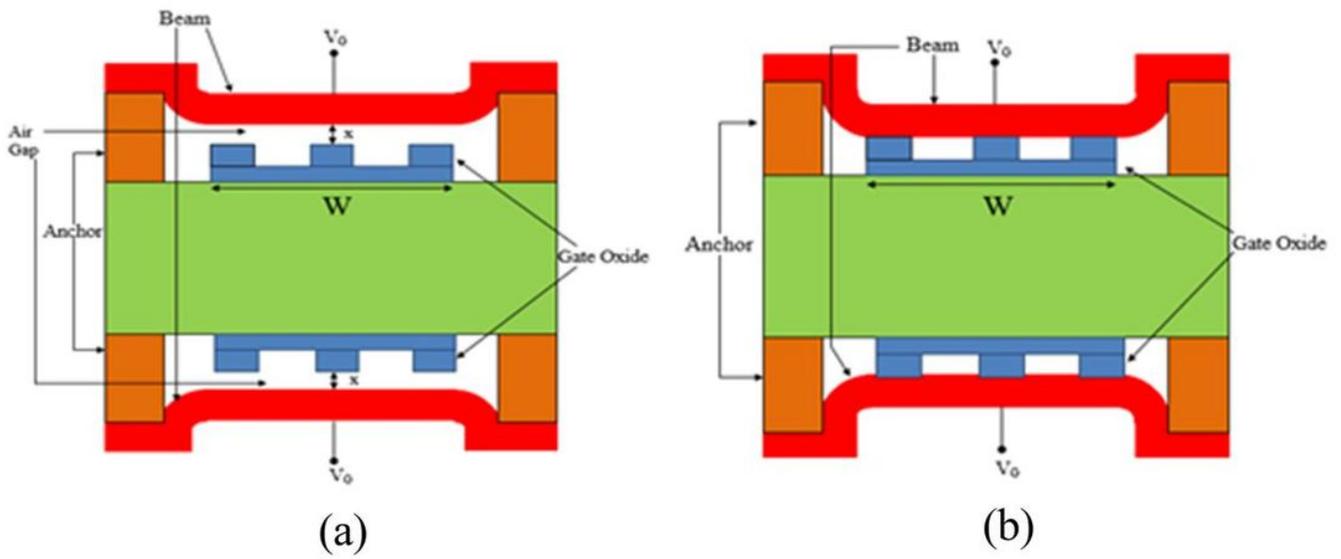


Figure 2

(a) Before the bending of DSGMOSFET, (b) After double gates collapsed on the gate oxides

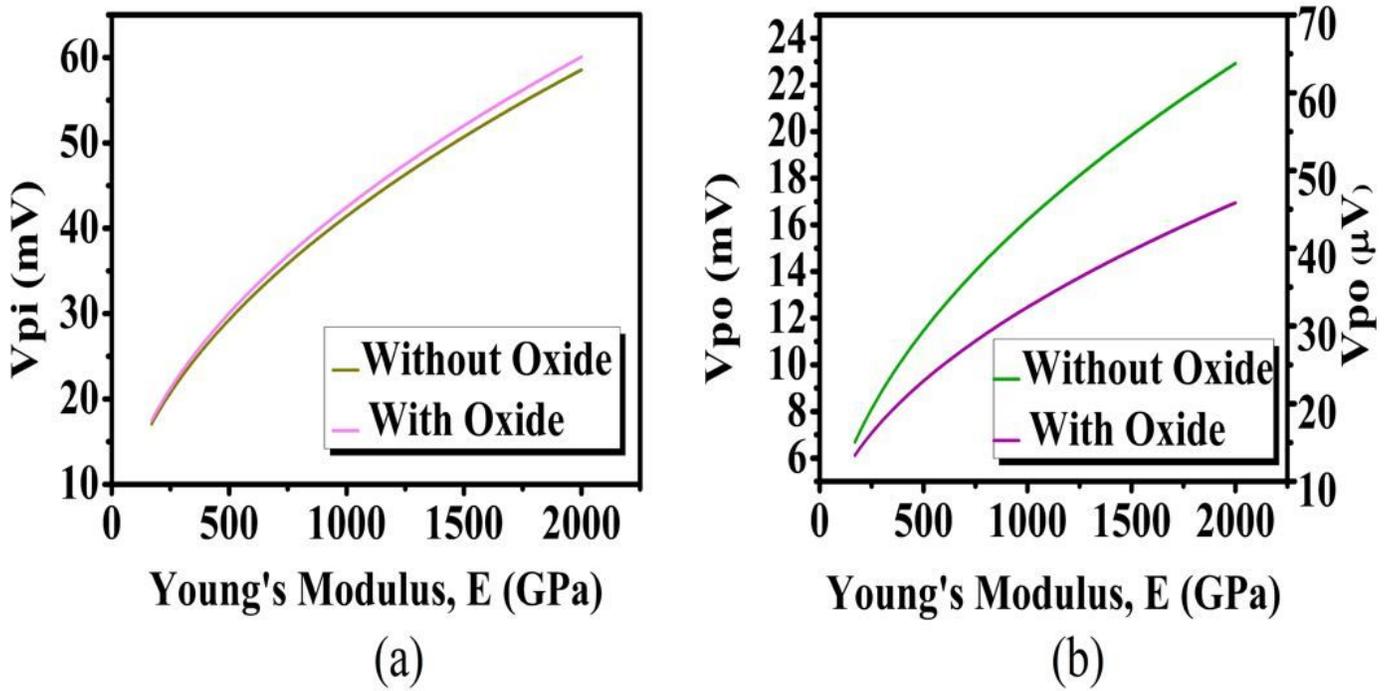


Figure 3

Pull-in (a) and Pull-out (b) voltage variations with respect to Young's modulus for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $t_{\text{gap}} = 10\text{nm}$, $t_{\text{beam}} = 1\text{nm}$ with the said device parameters.

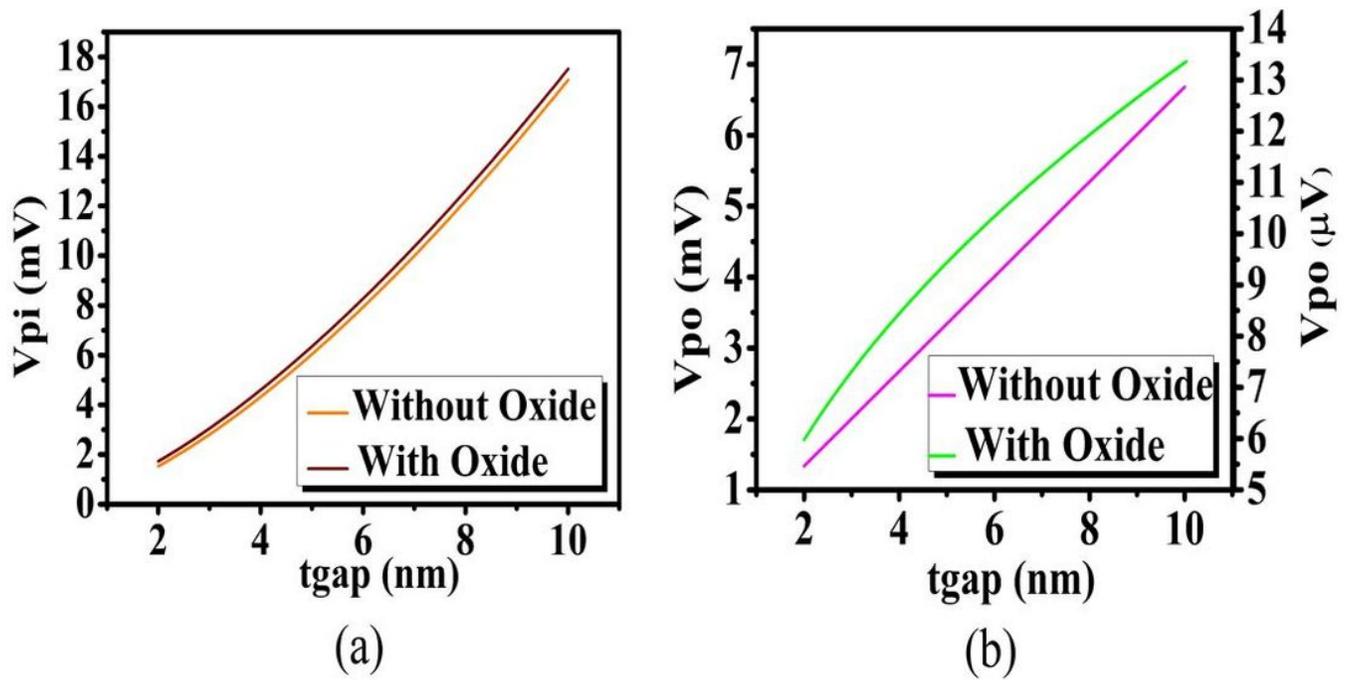


Figure 4

Pull-in (a) and Pull-out (b) voltage variations with respect to t_{gap} for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{beam} = 1\text{nm}$ with the said device parameters.

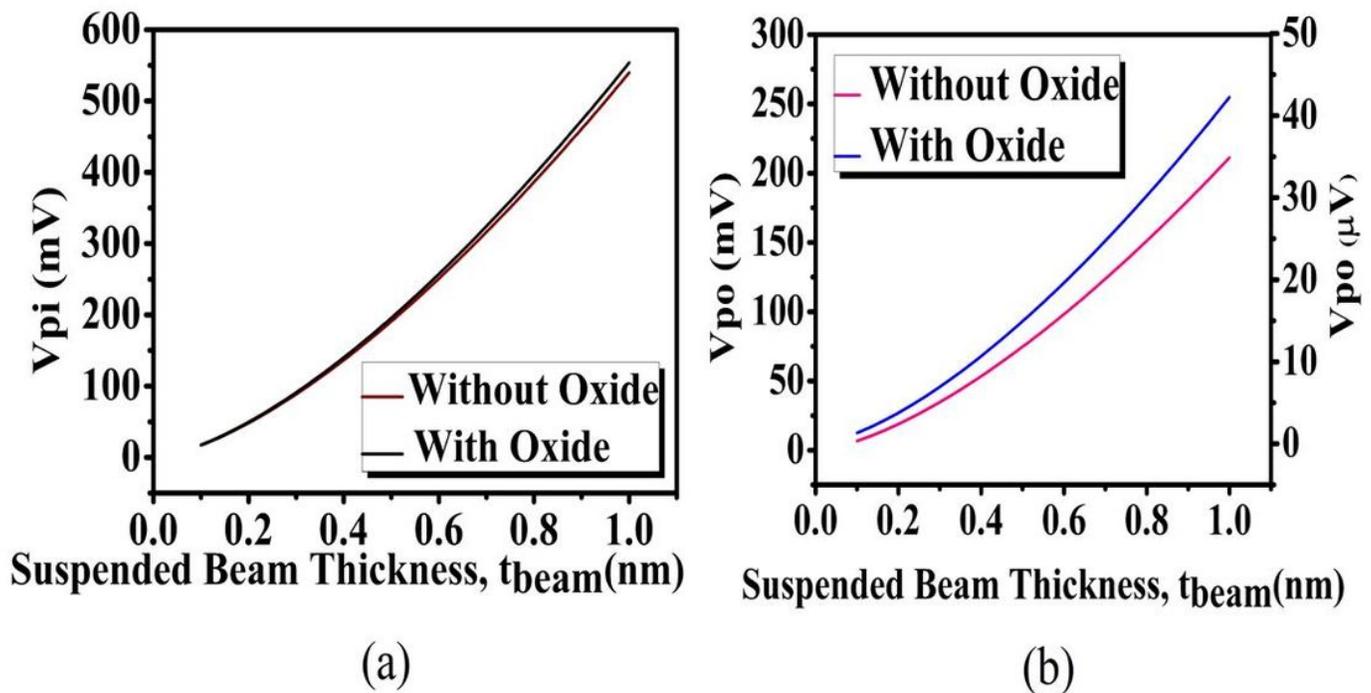


Figure 5

Pull-in (a) and Pull-out (b) voltage variations with respect to tbeam for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{\text{gap}} = 10\text{nm}$ with the said device parameters.

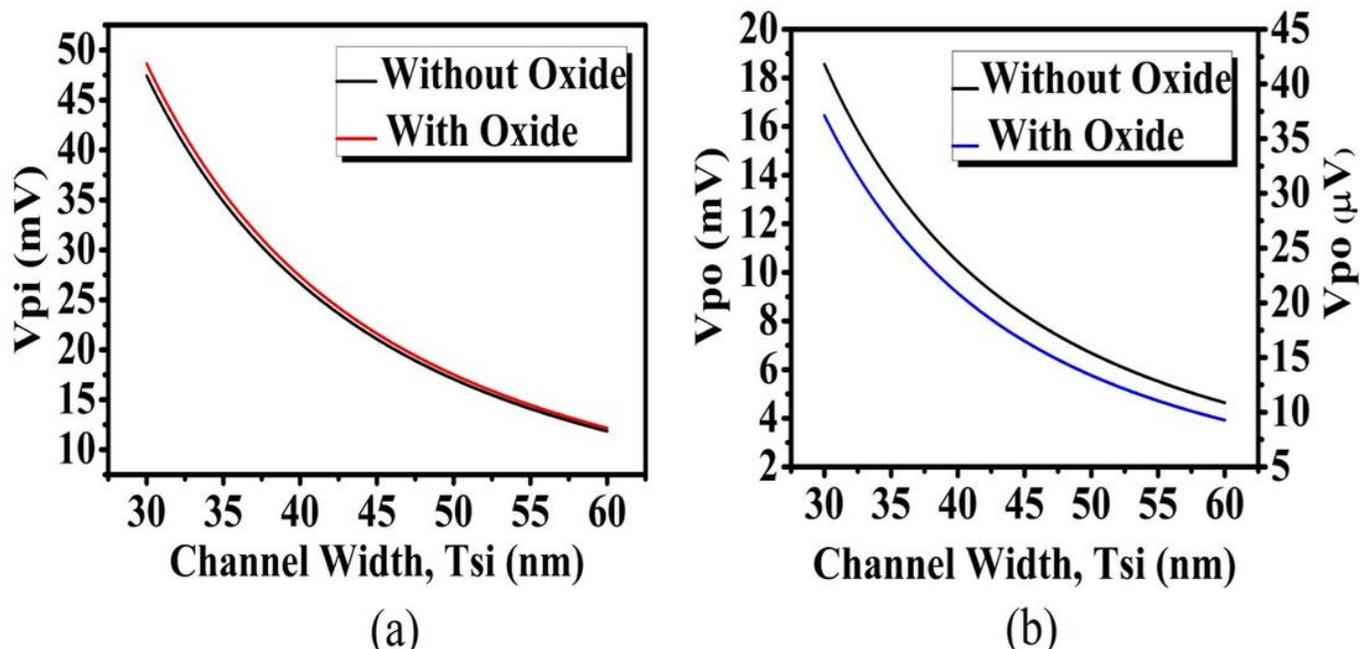
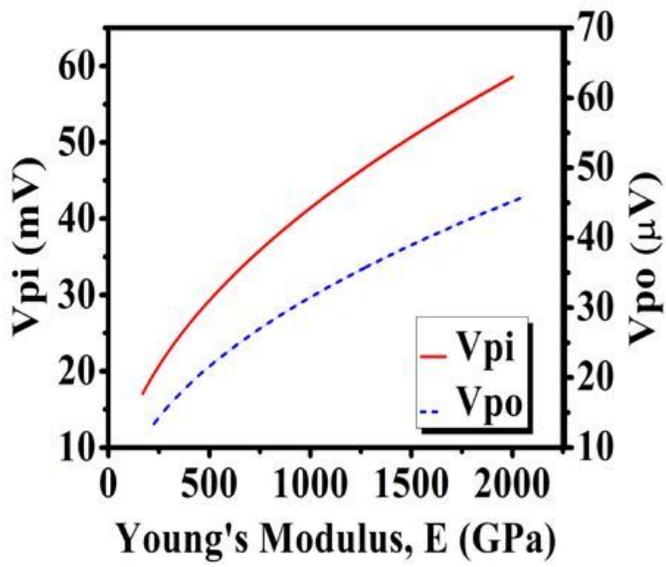
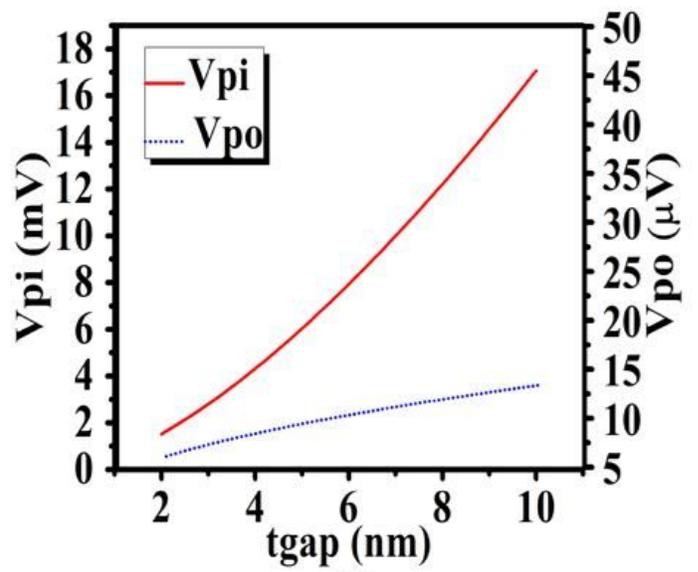


Figure 6

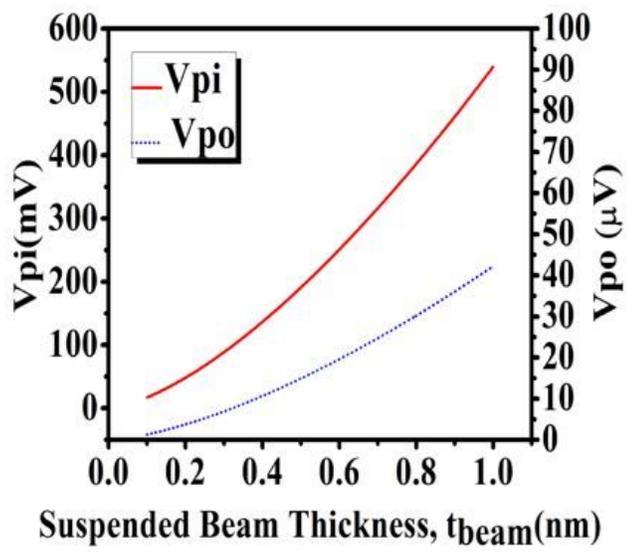
Pull-in (a) and Pull-out (b) voltage variations with respect to Tsi for both proposed and compared structures for $V_{FB} = 0.13\text{mV}$, $\Gamma = 20\mu\text{J}/\text{m}^2$, $D_0 = 0.2\text{nm}$, $E = 170\text{GPa}$, $t_{\text{gap}} = 10\text{nm}$, $t_{\text{beam}} = 1\text{nm}$ with the said device parameters.



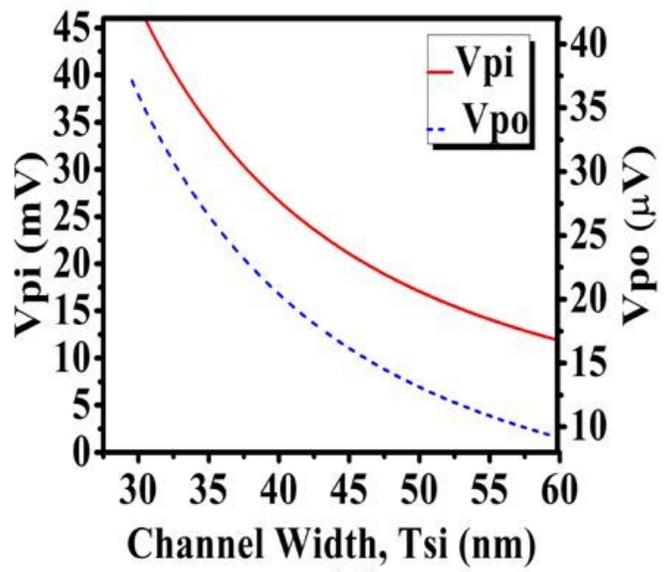
(a)



(b)



(c)



(d)

Figure 7

Pull-in and Pull-out voltage variations with respect to (a) Young's modulus of gate material (E) (b) t_{gap} (c) t_{beam} (d) T_{si} for the proposed structure.

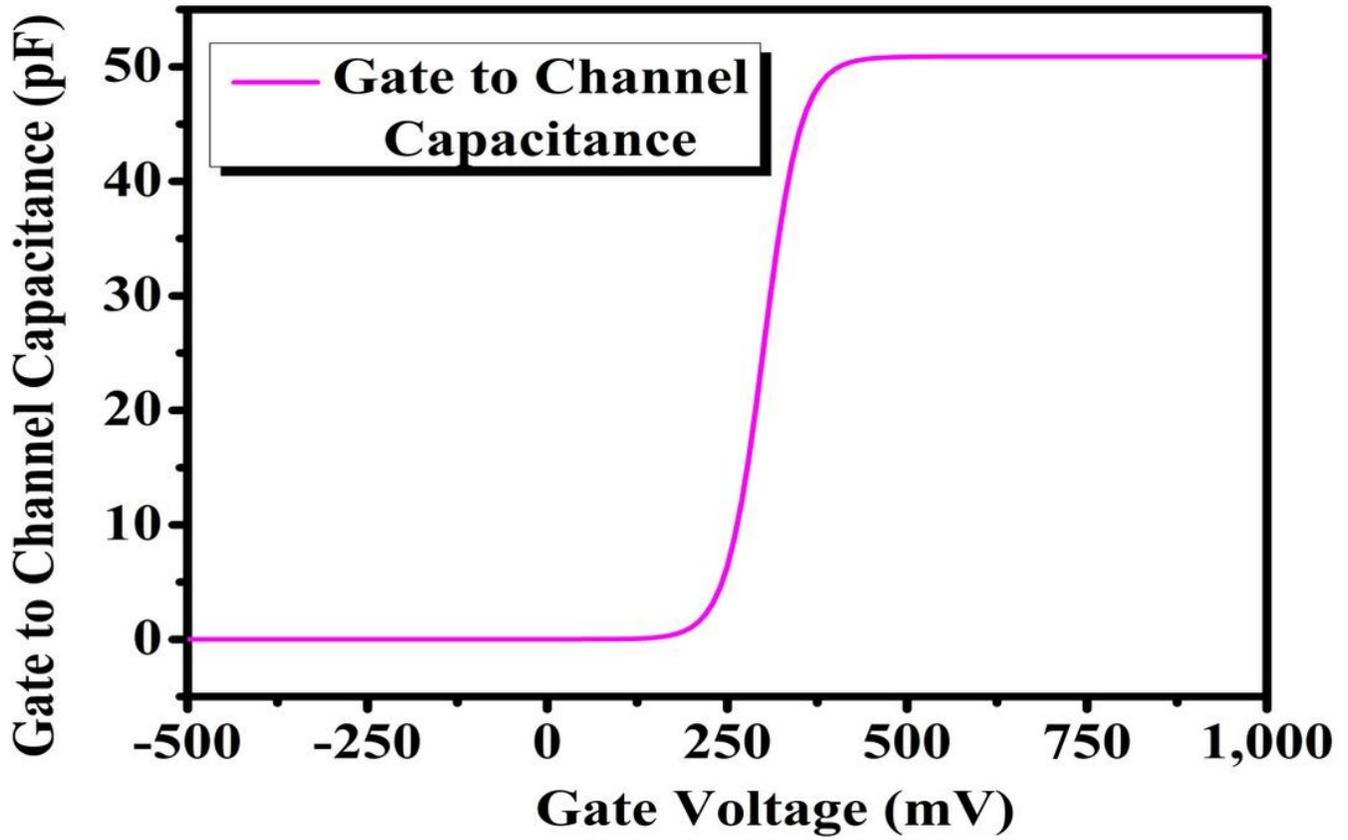


Figure 8

Gate to channel capacitance vs Gate Voltage It is also found that when $t_{ox} > 2\text{nm}$, it does not have any adverse effect on the pull-in voltage [6] which can be confirmed by Fig 9 and also confirmed the reason behind taking $t_{ox} = 2\text{nm}$

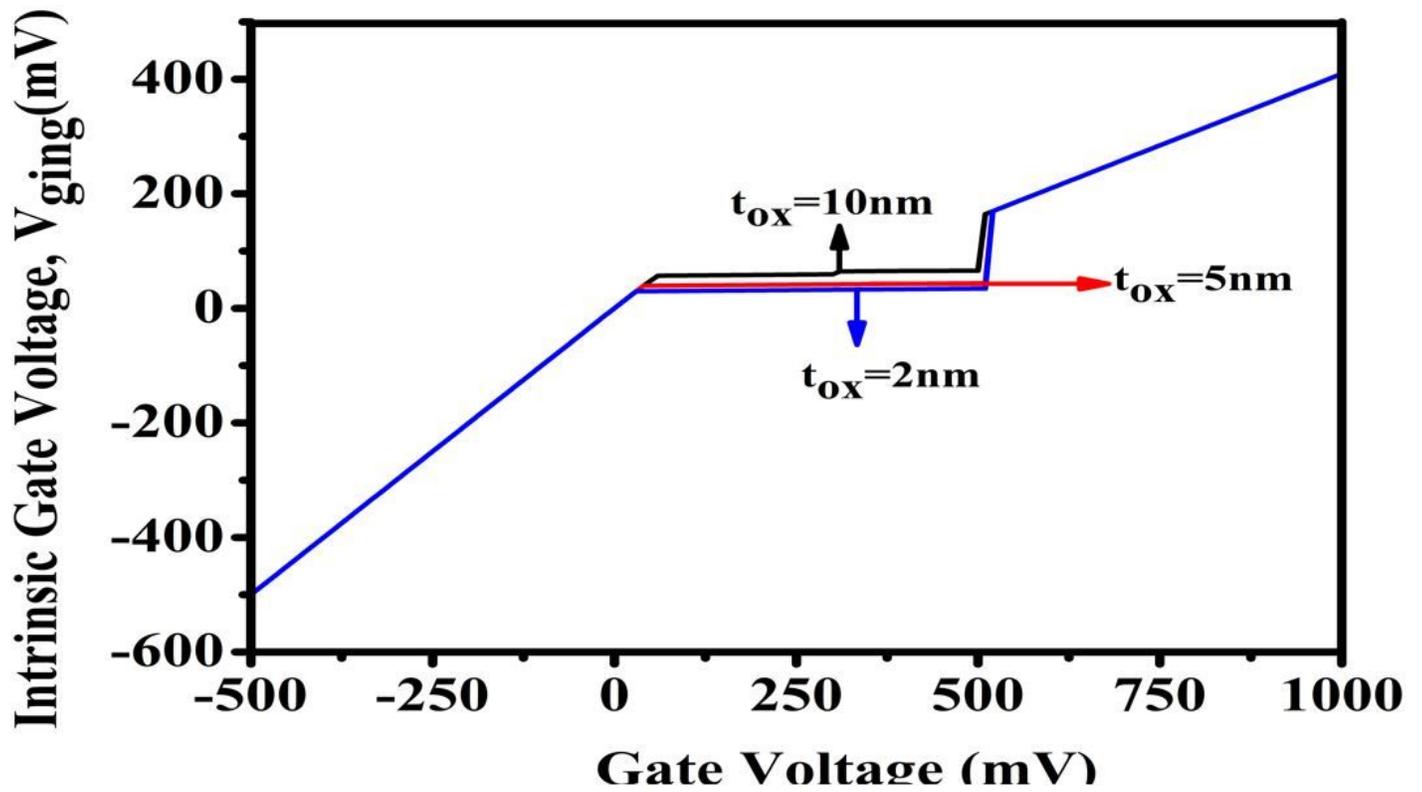


Figure 9

Intrinsic gate voltage vs extrinsic gate voltage, t_{ox} as parameter

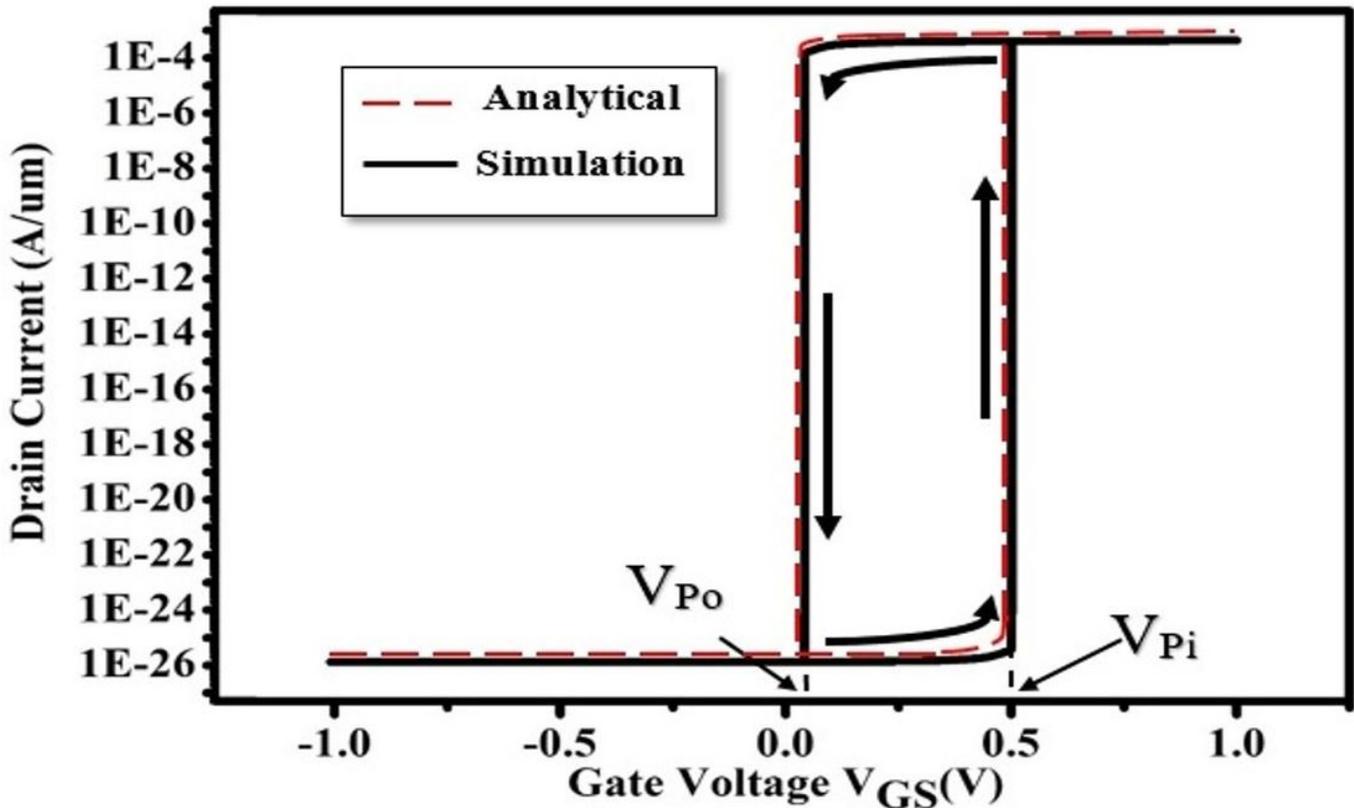


Figure 10

Drain current – Gate voltage characteristics